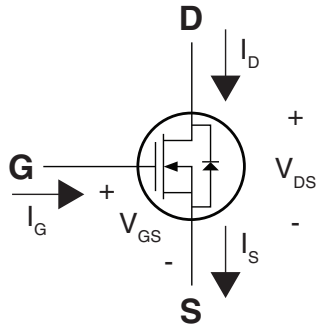
Depletion-Mode Power MOSFETs and Applications

1 Introduction

Applications like constant current sources, solid state relays, and high voltage DC lines in power systems require N-channel depletion-mode power MOSFETs that operate as normally-on switches when the gate-to-source voltage is zero (V_{GS}=0V). This paper will describe IXYS IC Division's latest N-channel, depletion-mode, power MOSFETs and their application advantages to help designers to select these devices in many industrial applications.

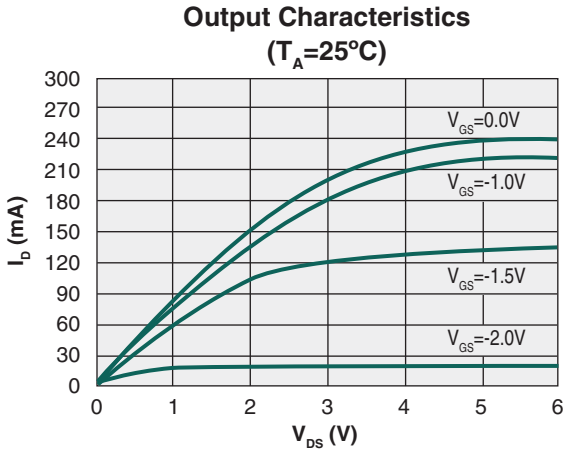
Figure 1 N-Channel Depletion-Mode MOSFET



A circuit symbol for an N-channel depletion-mode power MOSFET is given in Figure 1. The terminals are labeled as G (gate), S (source) and D (drain). IXYS IC Division depletion-mode power MOSFETs are built with a structure called vertical double-diffused MOSFET, or DMOSFET, and have better performance characteristics when compared to other depletion-mode power MOSFETs on the market such as high VDSX, high current, and high forward biased safe operating area (FBSOA).

Figure 2 shows a typical drain current characteristic, I_D, versus the drain-to-source voltage, V_{DS}, which is called the output characteristic. It's a similar plot to that of an N-channel enhancement mode power MOSFET except that it has current lines at V_{GS} equal to -2V, -1.5V, -1V, and 0V.

Figure 2 CPC3710 - MOSFET Output Characteristics



The on-state drain current, I_{DSS}, a parameter defined in the datasheet, is the current that flows between the drain and the source at a particular drain-to-source voltage (V_{DS}), when the gate-to-source voltage (V_{GS}) is zero (or short-circuited). By applying positive gate-to-source (V_{GS}) voltage, the device increases the current conduction level. On the other hand, negative gate-to-source (V_{GS}) voltage reduces the drain current. The CPC3710 stops conducting drain current at V_{GS}= -3.9V. This -3.9V is called the gate-to-source cutoff voltage or threshold voltage ($V_{GS(off)}$) of the device. In order to ensure proper turn-on, the applied gate-to-source (V_{GS}) voltage should be close

to 0V, and to properly turn off, a more negative V_{GS} voltage than the cutoff voltage ($V_{GS(off)}$) should be applied. Theoretically, the on-state drain current, $I_{D(on)}$, can be defined as:

$$I_D = I_{DSS} \bullet \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad \text{Equation (1)}$$

Note that Equation (1) is a theoretical formula that, in most cases, would not yield an accurate value of the drain current. $V_{GS(off)}$ has a range of -3.9V to -0.8V and $I_{D(on)}$ depends both on $V_{GS(off)}$ and the temperature.

A list of IXYS IC Division N-channel discrete depletion-mode power MOSFETs is given in Table 1. The table shows the device's four main parameters: the drain-to-source breakdown voltage (BV_{DSX}), the on-state resistance ($R_{DS(on)}$), the minimum and maximum gate-to-source cutoff voltage ($V_{GS(off)}$), and the on-state drain current (I_{DSS}) along with standard discrete package options such as SOT-89 and SOT-223.

Table 1: IXYS IC Division N-Channel Depletion-Mode MOSFETs

Part No.	BV_{DSX} (V)	$R_{DS(on)}$ (Ω)	$V_{GS(off)}$ Min V	$V_{GS(off)}$ Max V	I_{DSS} Min mA	Package
CPC3701	60	1	-0.8	-2.9	600	SOT-89
CPC3703	250	4	-1.6	-3.9	300	SOT-89
CPC3708	350	14	-2	-3.6	130	SOT-89, SOT-223
CPC3710	250	10	-1.6	-3.9	220	SOT-89
CPC3714	350	14	-1.6	-3.9	240	SOT-89
CPC3720	350	22	-1.6	-3.9	130	SOT-89
CPC3730	350	30	-1.6	-3.9	140	SOT-89
CPC3902	250	2.5	-1.4	-3.1	400	SOT-223
CPC3909	400	6	-1.4	-3.1	300	SOT-223
CPC3960	600	44	-1.4	-3.1	100	SOT-223
CPC3980	800	45	-1.4	-3.1	100	SOT-223
CPC3982	800	380	-1.4	-3.1	20	SOT-23
CPC5602	350	14	-2	-3.6	130	SOT-223
CPC5603	415	14	-2	-3.6	130	SOT-223

2 Selecting a Depletion-Mode MOSFET

Depletion-mode power MOSFETs will function in those applications requiring a normally-on switch. The main selection criteria for a depletion-mode MOSFET, based on the application, are as follows:

1. Select the breakdown voltage meeting the margin for reliable operation ~ BV_{DSX}, the drain-to-source breakdown voltage.

The application voltage must be lower than the drain-to-source breakdown voltage of the device. BV_{DSX} needs to be selected to accommodate the voltage swing between the positive bus and the negative bus as well as any voltage peaks caused by voltage ringing due to transients.

2. Identify the current requirement, and pick a package capable of handling that current ~ I_{DSS}, the on-state drain current.

The application current must be lower than the on-state drain current (I_{DSS})of the device. It is the maximum current that can flow between the drain and source, which occurs at a particular drain-to-source voltage (V_{DS}) and when the gate-to-source voltage (V_{GS}) is zero.

3. $V_{GS(off)}$, the gate-to-source cutoff voltage

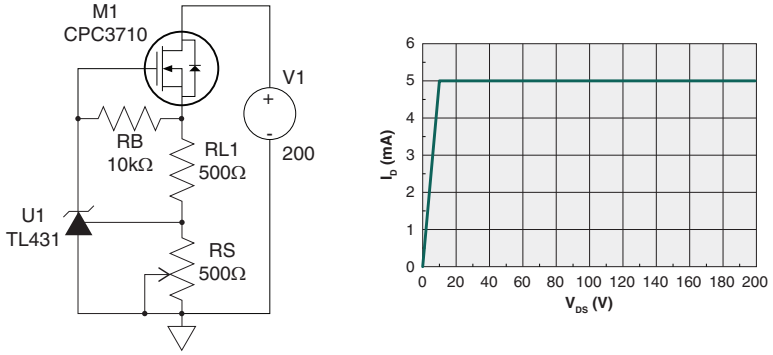
N-channel depletion-mode MOSFETs have a negative channel cutoff voltage, which is designated as $V_{GS(off)}$. A designer has to know the magnitude of the negative cutoff voltage (or threshold voltage). A negative gate-to-source voltage (V_{GS}) will reduce the drain current until the device's cutoff voltage level is reached and conduction ceases.

3 Applications

3.1 Current Source #1

Figure 3 shows a very precise current source to the load, RL1. TL431 is a programmable voltage reference IC. The feedback voltage from the sense resistor RS is controlled to be 2.5V. The circuit will operate as a current source at any current level below the CPC3710's rated current rating, I_{DSS}. Note that at 200V power dissipation will be 1W.

Figure 3 Depletion-Mode MOSFET Current Source and the Current Waveform



The theoretical sense resistor value is given by:

$$RS \cong \frac{V_{REF}}{I_D}$$ **Equation (2)**

Where:

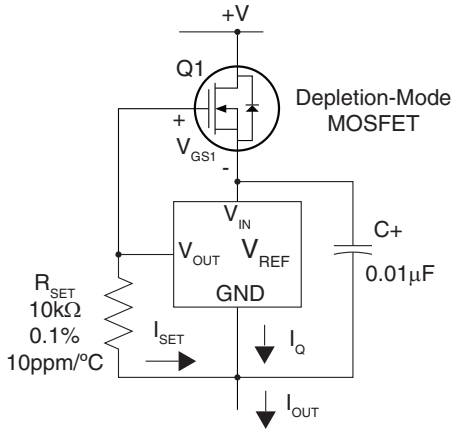
- V_{REF} = 2.5V (TL431)
- I_D = 5mA (Desired Current)

Note that Equation (2) is a theoretical formula that would probably not estimate the practical values of RS. In most cases, it's convenient to use a potentiometer to set the desired current level.

3.2 Current Source #2

Figure 4 shows a current source example with a voltage reference IC and a depletion-mode MOSFET, Q1, which compensates for supply voltage fluctuations. The current source provides a total current to the load comprising the set current through the resistor, RS, and the IC quiescent current, I_Q. This circuit provides precision current and ultra-high output impedance.

Figure 4 N-Channel Depletion-Mode MOSFET with a Voltage Reference to provide a Precise Current Source



$$I_{SET} = \frac{V_{OUT}}{R_{SET}}$$

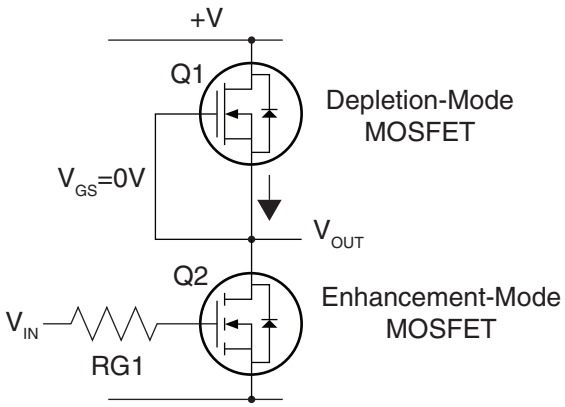
$I_{OUT} = I_{SET} + I_Q$

Output Impedance > 100MΩ

3.3 NMOS Inverter Circuit

Figure 5 shows an NMOS inverter circuit that uses a depletion-mode MOSFET as a load. The depletion-mode MOSFET, Q1, acts as a load for the enhancement-mode MOSFET, Q2, which acts as a switch.

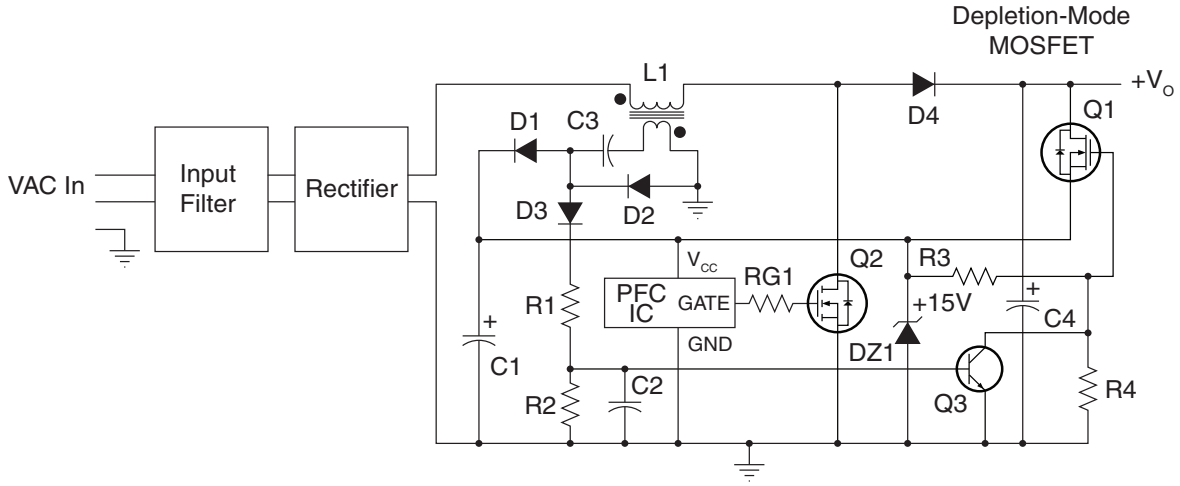
Figure 5 NMOS Inverter with Depletion-Mode Device used as a Load



3.4 Off-Line Switch-Mode Power Supply

Many applications in industrial and consumer electronics require off-line switch-mode power supplies that operate from wide voltage variations of 110VAC to 260VAC. Figure 6 shows such a power supply that uses a depletion-mode MOSFET, Q1, to kick-start the off-line operation by providing initial power to the IC (U1) through the source of Q1.

Figure 6 Power Supply Start-Up Circuit with Depletion-Mode MOSFET

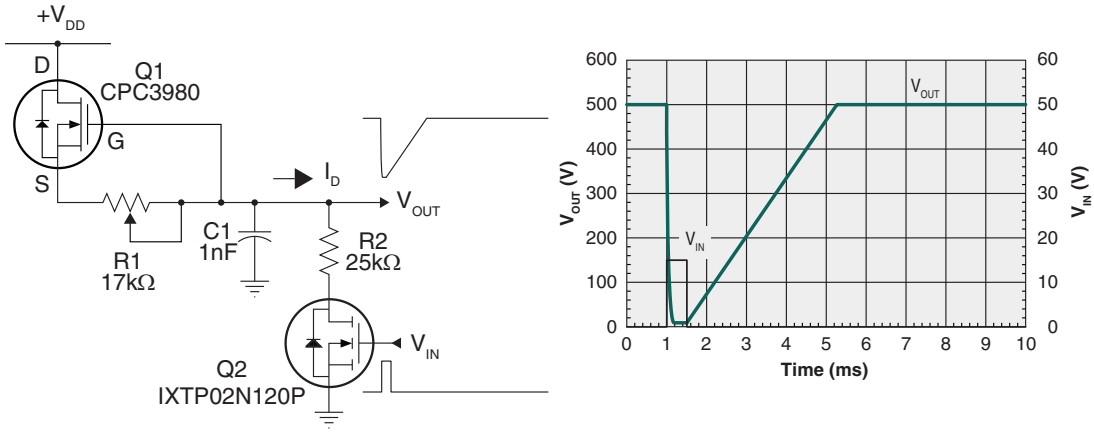


Q1 provides initial power from the output, $+V_O$. R3 and R4 set up a working point to obtain the minimum required current from Q1. The Zener diode, DZ1, limits the voltage across the IC (U1) to +15V. After the start-up, the secondary winding of boost inductor L1 generates the supply voltage for the IC through D1, D2 and C3, and enough current through D3 and R1 for the base of Q3 that turns on and clamps the gate of Q1 to ground.

3.5 Voltage Ramp Generator

Applications such as high voltage sweep circuits and automatic test equipment require high voltage ramps with a linear relationship between output voltage and time. The circuit shown in Figure 7 utilizes one depletion-mode MOSFET to design a voltage-ramp generator circuit.

Figure 7 High Voltage Ramp Generator with Depletion-Mode and Enhancement-Mode N-Channel MOSFETs



Q1 is configured as a constant current source charging a capacitor, C1; R1 provides negative feedback to regulate and set the desired current value. The constant current source charges the capacitor C1, and generates a voltage ramp, V_{OUT}, across the capacitor. Q2 can be turned on with a TTL or a CMOS control signal to reset the ramp voltage by discharging the capacitor to ground through R2. Resistor R2 is used to limit the discharge current for Q2 to operate within its SOA rating.

Assume the ramp voltage:

$$\frac{dV}{dt} = 0.1V/\mu s$$

The value of capacitor C1 should be small enough to reduce excessive charging and discharging of energy, but large enough that output loads and stray capacitances will not introduce significant errors. C1 is chosen to be 1nF.

The charging current is defined as:

$$I = C1 \bullet \frac{dV}{dt}$$

$$I = 1nF \bullet 0.1V/\mu s = 100\mu A$$

Equation (3)

The value of R1 for a 100μA current source can be approximated:

$$R1 \cong \frac{V_{GS}}{I_D} \bullet \left(\sqrt{\frac{I_D}{I_{DSS}}} - 1 \right)$$

Where:

- V_{GS} = Pinch-off voltage = -1.75V @ desired $I_{DS(on)}$
- I_{DSS} = Saturation current = 100mA, typical
- I_D = 100μA

$$R1 = \frac{-1.75V}{100\mu A} \bullet \left(\sqrt{\frac{100\mu A}{100mA}} - 1 \right) = \frac{-1.75V}{100\mu A} \bullet (0.03162 - 1) = \frac{1.695V}{100\mu A} = 16.9k\Omega$$

Assume the switching frequency for Q2 is swf=200 Hz and the discharge time is:

$$t_{Dischg} = 100\mu s$$

Power loss in the output capacitor, C1:

$$P = \frac{1}{2} \bullet C1 \bullet V^2 \bullet f_{sw} \qquad \textbf{Equation (4)}$$

Using equation (4),

$$P = \frac{1}{2} \bullet 1nF \bullet 500^2 \bullet 200Hz = 125\mu J \bullet 200Hz = 25\text{mJ/s} = 25mW$$

Discharging time:

$$t_{Dischg} = 4 \bullet R2C1 \qquad \textbf{Equation (5)}$$

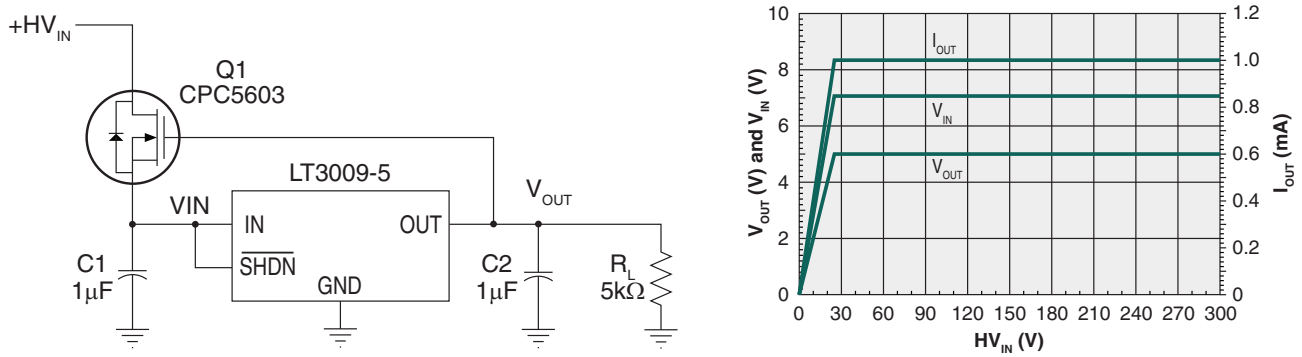
Using equation (5):

$$R2 = \frac{100\mu s}{4 \bullet 1nF} = 25k\Omega$$

3.6 Linear Voltage Regulator

Many applications require a linear voltage regulator that operates from high input voltage that is sourced from a wide voltage range of 120 VAC to 240 VAC with a maximum peak voltage of +/- 340V. Applications like CMOS ICs and small analog circuits require a 5V to 15V DC power supply that provides protection from very fast high voltage transients, and that has low quiescent current requirements. Figure 8 shows a high voltage off-line linear voltage regulator using a Depletion-mode MOSFET that can meet the above requirement of low transient voltage and low quiescent current.

Figure 8 High Voltage Off-line Linear Voltage Regulator



High voltage transients are generated in telecommunication circuits because of lightning and spurious radiation, and in automotive and avionics circuits because of inductive loads. Low quiescent current is required to minimize power dissipation in these linear regulators.

HV_{IN} Calculation:

$$I_D = I_{DSS} \bullet \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Solving for V_{GS}:

$$V_{GS} = V_{GS(off)} \bullet \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

Where:

- $V_{GS} = V_{OUT} - V_{IN}$

$$V_{IN} = V_{OUT} - V_{GS(off)} \bullet \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$V_{IN} = 5 + 2 \bullet \left(1 - \sqrt{\frac{1mA}{10mA}}\right) = 5 + 2 \bullet (1 - 0.3162) = 6.38V$$

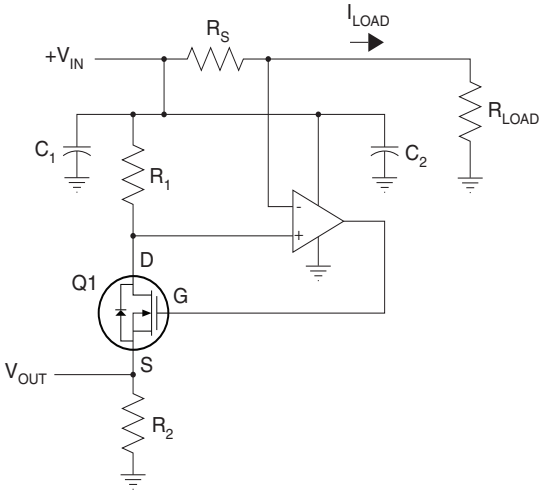
3.7 Current-Monitor Circuit

A simple current monitor circuit using an op-amp and a depletion-mode MOSFET is shown in Figure 9. R_1 monitors the current to the load and the MOSFET, Q1, provides an output voltage proportional to the current being monitored.

$$V_{OUT} = I_{LOAD} \bullet \left(\frac{R_S \bullet R_2}{R_1}\right) \qquad \text{Equation (7)}$$

Resistor, R_1, should have a tolerance of 0.1% with an appropriate wattage rating.

Figure 9 Current Monitor using Depletion-Mode MOSFET and a Single-Supply Op-Amp



For example:

- R_S=0.1Ω
- R_1=100Ω
- R_2=1kΩ

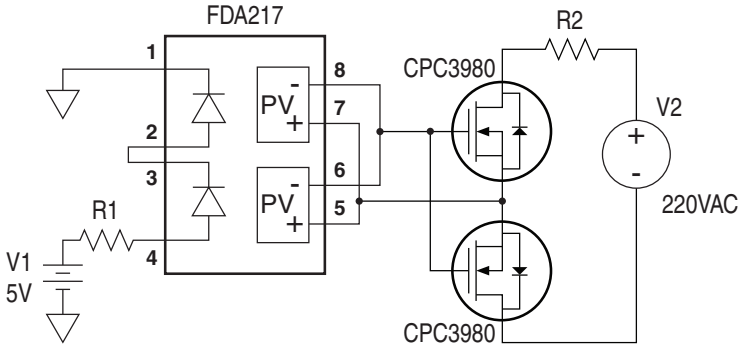
Using equation (7):

$$\frac{V_{OUT}}{I_{LOAD}} = \frac{R_S \bullet R_2}{R_1} = \frac{0.1 \bullet 1000}{100} = 1\text{V/A}$$

3.8 Normally Closed Solid State Relay

Depletion-mode FETs can be used to create normally closed solid state relays using IXYS IC Division's optical driver, FDA217. Figure 10 shows a typical connection of two external CPC3980 depletion FETs arranged in back-to-back configuration to make an AC/DC switch. FDA217 has internal turn-off circuitry so that no external bleed resistors are required.

Figure 10 FDA217 used with CPC3980 FETs to create Normally Closed Solid State Relay



Specification: AN-500-R03

10/3/2014

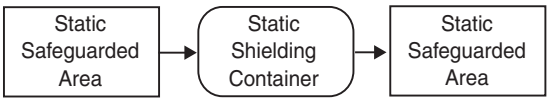
Handling MOS Devices

Static Discharge

Metal Oxide Semiconductor (MOS) devices have gained broad acceptance in telecommunications. This includes use of n-channel (NMOS) transistors, p-channel (PMOS) transistors, or both (complementary or CMOS) transistors. Most IXYS IC Division devices are fabricated using CMOS techniques, but some use PMOS. In any case, MOS circuits require special attention in design and handling because of their susceptibility to damage through buildup of static charges and the currents that occur during discharge.

Whether alone or mounted in circuit boards, MOS ICs are subject to buildup of static charges and damaging discharges. Voltage of several hundred volts can affect these devices, while one or two thousand volts will certainly cause harm. Five hundred volts can easily be generated by a person walking around or moving in a chair, and thousands of volts can be generated by the simple act of pulling out and tearing off a piece of transparent tape. Under these circumstances, precautions must be taken to limit the potential for damage to costly IC devices. MOS ICs should be handled in static-protected or “safeguarded” areas. Such areas include ionized air flow over nonconducting surfaces. When not in these areas, ICs should be kept in static shielded containers. ICs must be handled in safeguarded areas (receiving inspection, stores, assembly, and test) and, when moved from area to area, should be protected by shielded containers. Failure to implement procedures of this sort or relaxation of procedures can result in loss of valuable parts, increased production fallout, and higher repair costs.

Static Transmission



CMOS Latchup

Though all ICs are subject to static discharge damage, CMOS ICs can experience another kind of damaging event known as “latchup” or “SCR.” In this case, large currents can follow-through the part from the power supply, damaging transistors and interconnections. This occurs when currents are injected into the chip where they were not intended, usually through an I/O pin which has been driven to a voltage outside the supply range by some external device or event. This phenomenon is equivalent to four-layer conduction as used in SCRs, where a semiconductor device is “turned on” by injecting a current into a trigger layer. The device stays “on” until voltage is removed. This is useful in SCR control circuits, but in the case of CMOS ICs they may (1) recover completely after power has been cycled, (2) recover, but act very strangely, or (3) blow up completely. Causes can be inadequate power supply filtering, transient protection, or coincidences of PWB track layout. Static discharge may also trigger latchup.

For additional information please visit our website at: www.ixysic.com

Specification: AN-130-R04

4/10/2014

IXYS
INTEGRATED CIRCUITS DIVISION

CPC3720
350V, 22Ω N-Channel Depletion-Mode FET

$V_{(BR)DSX}$ / $V_{(BR)DGX}$	$R_{DS(on)}$ (max)	I_{DSS} (min)	Package
$350V_P$	22Ω	130mA	SOT-89

Features

- Offers Low $R_{DS(on)}$ at Cold Temperatures
- $R_{DS(on)}$ 22Ω max. at 25ºC
- High Input Impedance
- High Breakdown Voltage: $350V_P$
- Low $V_{GS(off)}$ Voltage: -1.6 to -3.9V
- Small Package Size SOT-89
- Flammability Rating UL 94 V-0

Applications

- Ignition Modules
- Normally-On Switches
- Solid State Relays
- Converters
- Telecommunications
- Power Supply

Description

The CPC3720 is an N-channel, depletion mode, field effect transistor (FET) that utilizes IXYS Integrated Circuits Division's proprietary third-generation vertical DMOS process. The third-generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. Our vertical DMOS process yields a robust device, with high input impedance, for use in high power applications. The CPC3720 is a highly reliable FET device that has been used extensively in our solid state relays for industrial and telecommunications applications.

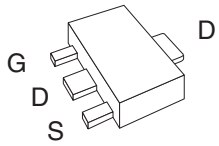
This device excels in power applications requiring low drain-source resistance, particularly in cold environments such as automotive ignition modules. The CPC3720 offers a low, 22Ω maximum, on-state resistance at 25ºC.

The CPC3720 has a minimum breakdown voltage of $350V_P$, and is available in an SOT-89 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

Ordering Information

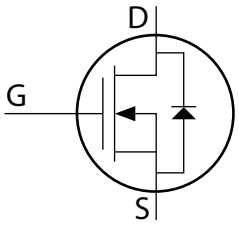
Part #	Description
CPC3720CTR	N-Channel Depletion Mode FET, SOT-89 Pkg. Tape and Reel (1000/Reel)

Package Pinout



(SOT-89)

Circuit Symbol



Absolute Maximum Ratings @ 25ºC

Parameter	Ratings	Units
Drain-to-Source Voltage	350	V_P
Gate-to-Source Voltage	±15	V_P
Pulsed Drain Current	600	mA
Total Package Dissipation	1.4 [1]	W
Junction Temperature	150	ºC
Operational Temperature	-55 to +125	ºC
Storage Temperature	-55 to +125	ºC

[1] Mounted on FR4 board 1"x1"x0.062"

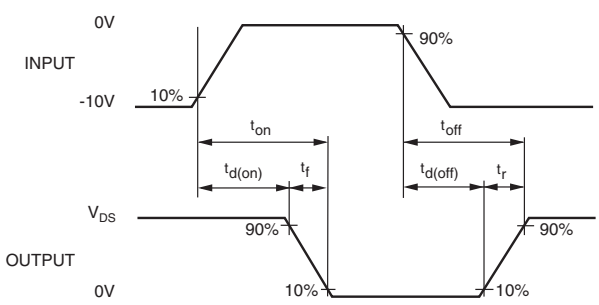
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

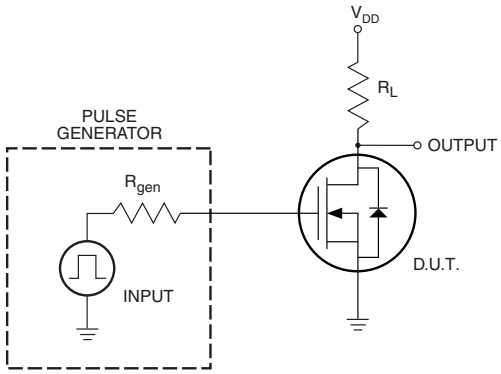
Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

Electrical Characteristics @ 25ºC (Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSX}$	V_{GS}= -5V, I_D=100µA	350	-	-	V_P
Gate-to-Source Off Voltage	$V_{GS(off)}$	V_{DS}= 5V, I_D=1mA	-1.6	-	-3.9	V
Change in $V_{GS(off)}$ with Temperatures	$dV_{GS(off)}/dT$	V_{DS}= 5V, I_D=1µA	-	-	4.5	mV/ºC
Gate Body Leakage Current	I_{GSS}	V_{GS}=±15V, V_{DS}=0V	-	-	100	nA
Drain-to-Source Leakage Current	$I_{D(off)}$	V_{GS}= -5V, V_{DS}=350V	-	-	1	µA
		V_{GS}= -5V, V_{DS}=280V, T_A=125ºC	-	-	1	mA
Saturated Drain-to-Source Current	I_{DSS}	V_{GS}= 0V, V_{DS}=15V	130	-	-	mA
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	V_{GS}= 0V, I_D=130mA	-	-	22	Ω
Change in $R_{DS(on)}$ with Temperatures	$dR_{DS(on)}/dT$	V_{GS}= 0V, I_D=130mA	-	-	1.1	%/ºC
Forward Transconductance	G_{FS}	I_D= 100mA, V_{DS} = 10V	225	-	-	m℧
Input Capacitance	C_{ISS}	V_{GS}= -5V V_{DS}= 25V f= 1MHz	-	70	350	pF
Common Source Output Capacitance	C_{OSS}			20	60	
Reverse Transfer Capacitance	C_{RSS}			10	60	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}= 25V I_D= 150mA V_{GS}= 0V to -10V R_{gen}= 50Ω	-	20	-	ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall time	t_f			50		
Source-Drain Diode Voltage Drop	V_{SD}	V_{GS}= -5V, I_{SD}= 150mA	-	0.6	1.8	V
Thermal Impedance (Junction to Ambient)	θ_{JA}	-	-	90	-	ºC/W

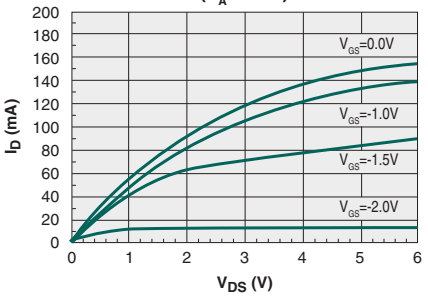
Switching Waveform & Test Circuit



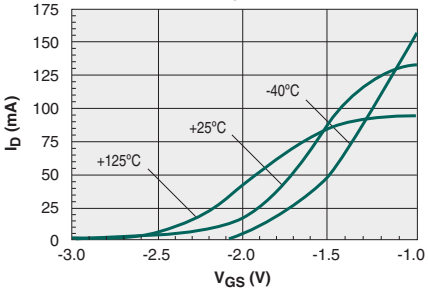


PERFORMANCE DATA*

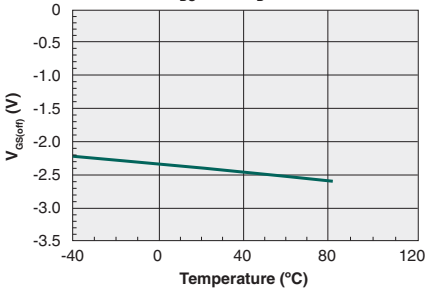
Output Characteristics (T_A=25°C)



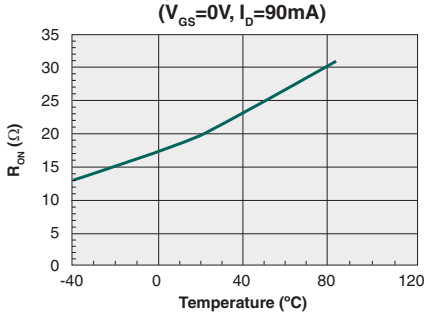
Transfer Characteristics (V_{DS}=5V)



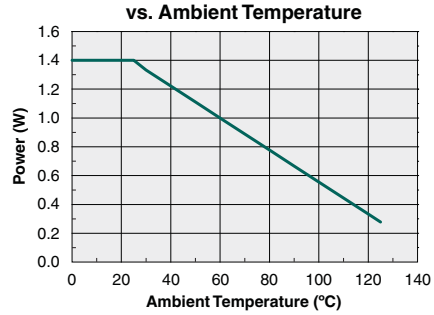
$V_{GS(off)}$ vs. Temperature (V_{DS}=10V, I_D=1mA)



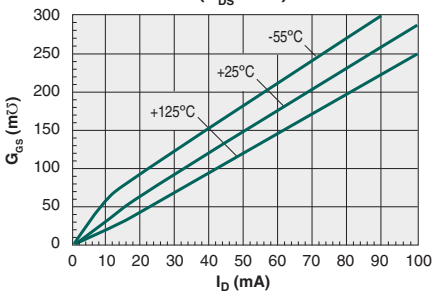
R_{ON} vs. Temperature (V_{GS}=0V, I_D=90mA)



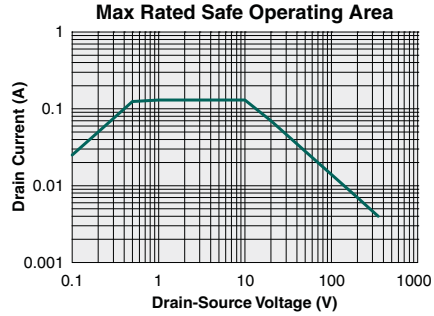
Power Dissipation vs. Ambient Temperature



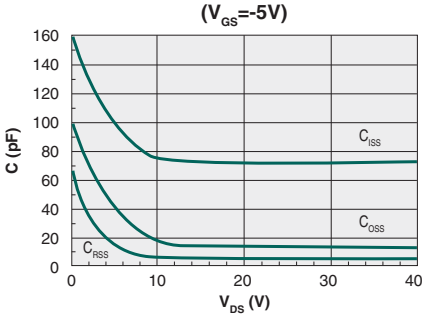
Transconductance vs. Drain Current (V_{DS}=10V)



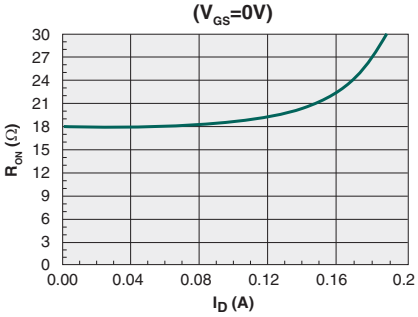
Max Rated Safe Operating Area



Capacitance vs. Drain Source Voltage (V_{GS}=-5V)



On-Resistance vs. Drain Current (V_{GS}=0V)



*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC3720C	MSL 1

ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

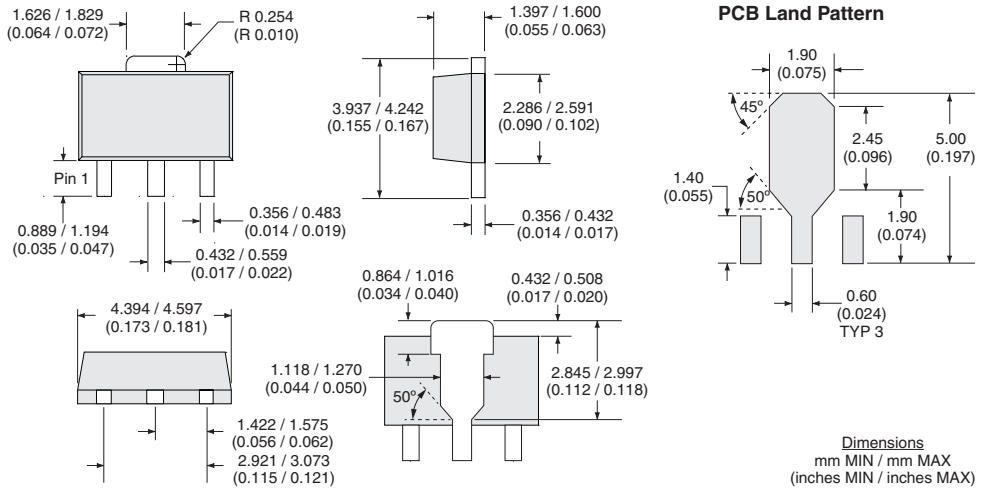
Device	Classification Temperature (T_c)	Dwell Time (t_P)	Max Reflow Cycles
CPC3720C	260°C	30 seconds	3

Board Wash

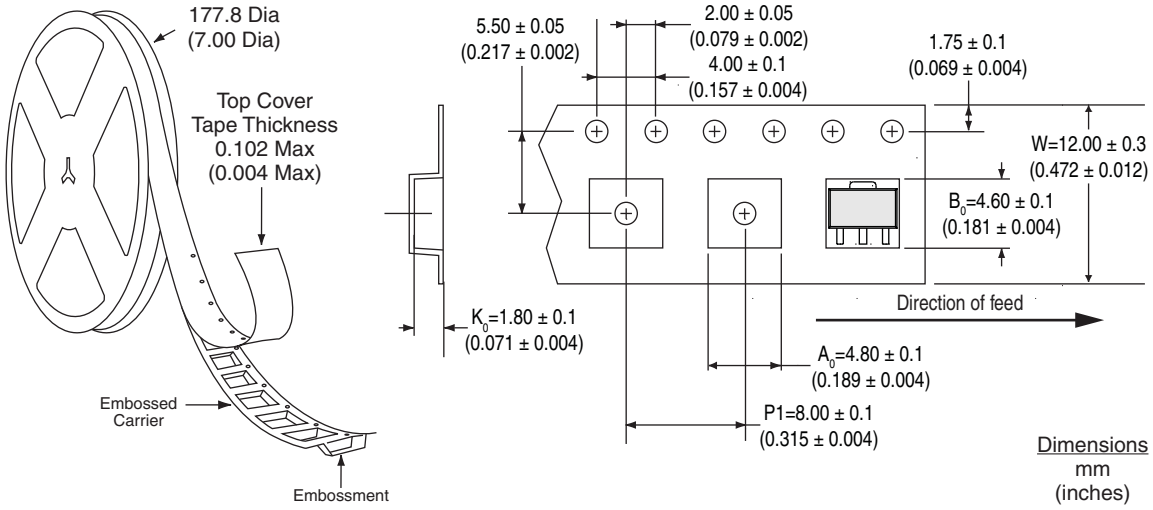
IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

MECHANICAL DIMENSIONS

CPC3720C



CPC3720CTR Tape & Reel



For additional information please visit our website at: www.ixysic.com

IXYS
A Littelfuse Technology

Specification: DS-CPC3720-R01

4/17/2020