Mounting and Handling of Semiconductor Devices

Introduction

Proper mounting and handling of semiconductor devices, particularly those used in power applications, is an important, yet sometimes overlooked, consideration in the assembly of electronic systems. Power devices need adequate heat dissipation to increase operating life and reliability and allow the device to operate within manufacturers' specifications. Also, in order to avoid damage to the semiconductor chip or internal assembly, the devices should not be abused during assembly. Very often, device failures can be attributed directly to a heat sinking or assembly damage problem.

The information in this application note guides the semiconductor user in the proper use of Littelfuse devices, particularly the popular and versatile TO-220 and TO-218 epoxy packages.

Contact the Littelfuse Applications Engineering Group for further details or suggestions on use of Littelfuse devices.

Lead Forming — Typical Configurations

A variety of mounting configurations are possible with Littelfuse power semiconductor TO-92, DO-15, and TO- 220 packages, depending upon such factors as power requirements, heat sinking, available space, and cost considerations. Figure AN1004.1 shows typical examples and basic design rules.

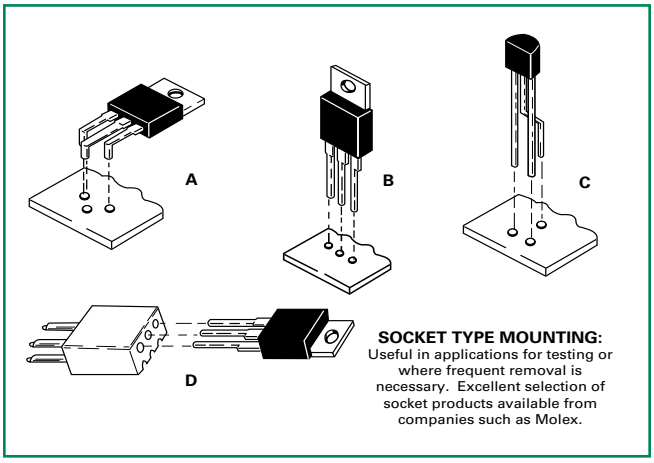


Figure AN1004.1 Component Mounting

These are suitable only for vibration-free environments and low-power, free-air applications. For best results, the device should be in a vertical position for maximum heat dissipation from convection currents.

Standard Lead Forms

Littelfuse encourages users to allow factory production of all lead and tab form options. Littelfuse has the automated machinery and expertise to produce pre-formed parts at minimum risk to the device and with greater convenience for the consumer. See the "Lead Form Dimensions" section of this catalog for a complete list of readily available lead form options. Contact Littelfuse for information regarding custom lead form designs.

Lead Bending Method

Leads may be bent easily and to any desired angle, provided that the bend is made at a minimum 0.063" (0.1" for TO-218 package) away from the package body with a minimum radius of 0.032" (0.040" for TO-218 package) or 1.5 times lead thickness rule. DO-15 device leads may be bent with a minimum radius of 0.050", and DO-35 device leads may be bent with a minimum radius of 0.028". Leads should be held firmly between the package body and the bend so that strain on the leads is not transmitted to the package body, as shown in Figure AN1004.2. Also, leads should be held firmly when trimming length.

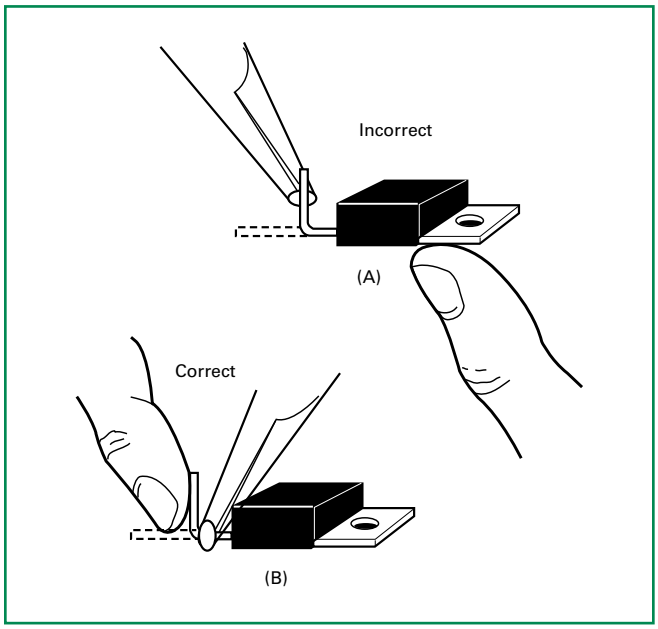


Figure AN1004.2 Lead Bending Method

When bending leads in the plane of the leads (spreading), bend only the narrow part. Sharp angle bends should be done only once as repetitive bending will fatigue and break the leads.

Heat Sinking

Use of the largest, most efficient heat sink as is practical and cost effective extends device life and increases reliability. In the illustration shown in Figure AN1004.3, each device is electrically isolated.

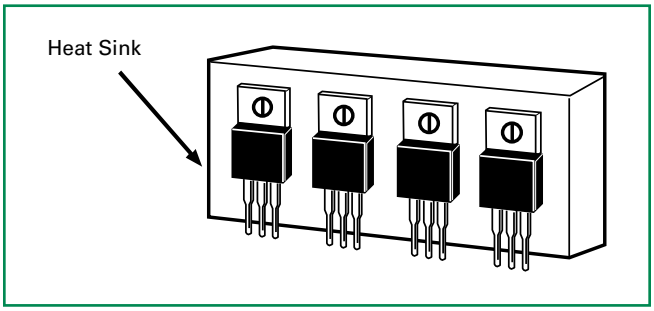


Figure AN1004.3 Several Isolated TO-220 Devices Mounted to a Common Heat Sink

Many power device failures are a direct result of improper heat dissipation. Heat sinks with a mating area smaller than the metal tab of the device are unacceptable. Heat sinking material should be at least 0.062" thick to be effective and efficient.

Note that in all applications the maximum case temperature (T_C) rating of the device must not be exceeded. Refer to the individual device data sheet rating curves (T_C versus I_T) as well as the individual device outline drawings for correct T_C measurement point.

Figure AN1004.4 through Figure AN1004.6 show additional examples of acceptable heat sinks.

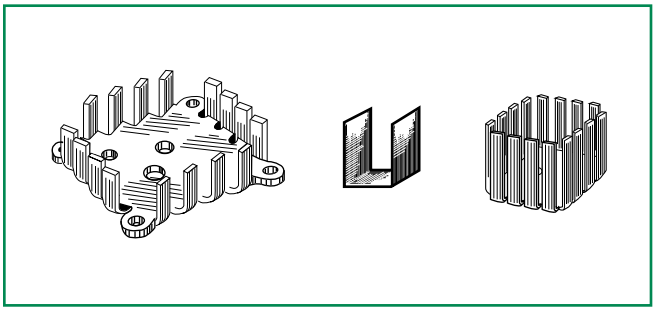


Figure AN1004.4 Examples of PC Board Mounts

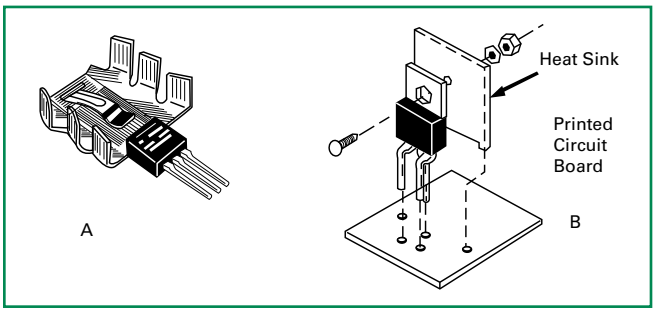


Figure AN1004.5 Vertical Mount Heat Sink

Several types of vertical mount heat sinks are available. Keep heat sink vertical for maximum convection.

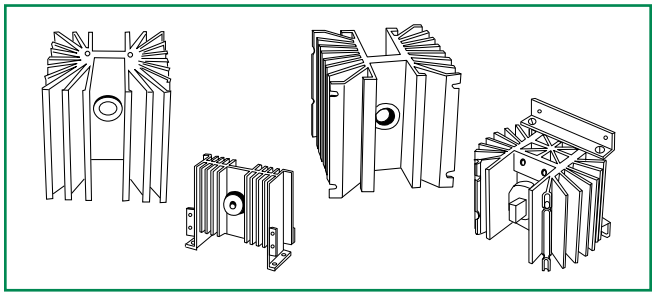


Figure AN1004.6 Examples of Extruded Aluminum

When coupled with fans, extruded aluminum mounts have the highest efficiency.

Heat Sinking Notes

Care should be taken not to mount heat sinks near other heat-producing elements such as power resistors, because black anodized heat sinks may absorb more heat than they dissipate.

Some heat sinks can hold several power devices. Make sure that if they are in electrical contact to the heat sink, the devices do not short-circuit the desired functions. Isolate the devices electrically or move to another location. Recall that the mounting tab of Littelfuse isolated TO-220 devices is electrically isolated so that several devices may be mounted on the same heat sink without extra insulating components. If using an external insulator such as mica, with a thickness of 0.004", an additional thermal resistance of 0.8° C/W for TO-220 or 0.5° C/W for TO-218 devices is added to the $R_{\theta JC}$ device rating.

Allow for adequate ventilation. If possible, route heat sinks to outside of assembly for maximum airflow.

Mounting Surface Selection

Proper mounting surface selection is essential to efficient transfer of heat from the semiconductor device to the heat sink and from the heat sink to the ambient. The most popular heat sinks are flat aluminum plates or finned extruded aluminum heat sinks.

The mounting surface should be clean and free from burrs or scratches. It should be flat within 0.002 inch per inch, and a surface finish of 30 to 60 microinches is acceptable. Surfaces with a higher degree of polish do not produce better thermal conductivity.

Many aluminum heat sinks are black anodized to improve thermal emissivity and prevent corrosion. Anodizing results in high electrical but negligible thermal insulation. This is an excellent choice for isolated TO-220 devices. For applications of non-isolated TO-220 devices where electrical connection to the common anode tab is required, the anodization

should be removed. Iridite or chromate acid dip finish offers low electrical and thermal resistance. Either TO-218, Fastpak or TO-220 devices may be mounted directly to this surface, regardless of application. Both finishes should be cleaned prior to use to remove manufacturing oils and films. Some of the more economical heat sinks are painted black. Due to the high thermal resistance of paint, the paint should be removed in the area where the semiconductor is attached.

Bare aluminum should be buffed with #000 steel wool and followed with an acetone or alcohol rinse. Immediately, thermal grease should be applied to the surface and the device mounted down to prevent dust or metal particles from lodging in the critical interface area.

For good thermal contact, the use of thermal grease is essential to fill the air pockets between the semiconductor and the mounting surface. This decreases the thermal resistance by 20%. For example, a typical TO-220 with $R_{\theta JC}$ of 1.2 °C/W may be lowered to 1 °C/W by using thermal grease.

Littelfuse recommends Dow-Corning 340 as a proven effective thermal grease. Fibrous applicators are not recommended as they may tend to leave lint or dust in the interface area. Ensure that the grease is spread adequately across the device mounting surface, and torque down the device to specification.

Contact Littelfuse Applications Engineering for assistance in choosing and using the proper heat sink for specific application.

Hardware And Methods

TO-220

The mounting hole for the Teccor TO-220 devices should not exceed 0.140" (6/32) clearance. (Figure AN1004.7) No insulating bushings are needed for the L Package (isolated) devices as the tab is electrically isolated from the semiconductor chip. 6/32 mounting hardware, especially round head or Fillister machine screws, is recommended and should be torqued to a value of 6 inch-lbs.

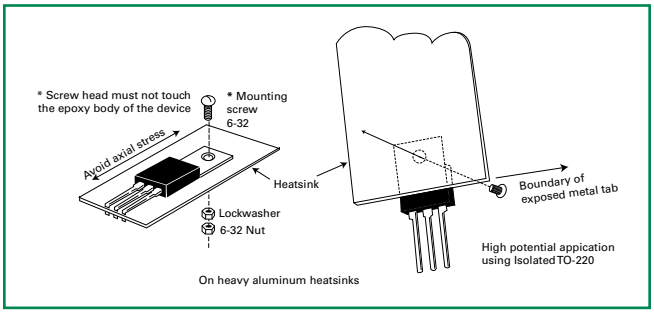


Figure AN1004.7 TO-220 Mounting

Punched holes are not acceptable due to cratering around the hole which can cause the device to be pulled into the crater by the fastener or can leave a significant portion of the device out of contact with the heat sink. The first effect may cause immediate damage to the package and early failure, while the second can create higher operating temperatures which will shorten operating life. Punched holes are quite acceptable in thin metal plates where fine-edge blanking or sheared-through holes are employed.

Drilled holes must have a properly prepared surface. Excessive chamfering is not acceptable as it may create a crater effect. Edges must be deburred to promote good contact and avoid puncturing isolation materials.

For high-voltage applications, it is recommended that only the metal portion of the TO-220 package (as viewed from the bottom of the package) be in contact with the heat sink. This will provide maximum oversurface distance and prevent a high voltage path over the plastic case to a grounded heat sink.

TO-218

The mounting hole for the TO-218 device should not exceed 0.164" (8/32) clearance. Isolated versions of TO-218 do not require any insulating material since mounting tab is electrically isolated from the semiconductor chip. Round lead or Fillister machine screws are recommended. Maximum torque to be applied to mounting tab should not exceed 8 inch-lbs.

The same precautions given for the TO-220 package concerning punched holes, drilled holes, and proper prepared heat sink mounting surface apply to the TO-218 package. Also for high-voltage applications, it is recommended that only the metal portion of the mounting surface of the TO-218 package be in contact with heat sink. This achieves maximum oversurface distance to prevent a high-voltage path over the device body to grounded heat sink.

General Mounting Notes

Care must be taken on TO-220 & TO-218 packages at all times to avoid strain to the mounting tab or leads. For easy insertion of the part onto the board or heat sink, avoid axial strain on the leads. Carefully measure holes for the mounting tab and the leads, and do any forming of the tab or leads before mounting. Refer to the "Lead Form Dimensions" section of this catalog before attempting lead form operations.

Rivets may be used for less demanding and more economical applications. 1/8" all-aluminum pop rivets can be used on both TO-220 and TO-218 packages. Use a 0.129"-0.133" (#30) drill for the hole and insert the rivet from the top side, as shown in Figure AN1004.9. An insertion tool, similar to a "USM" PRG 430 hand riveter, is recommended. A wide selection of grip ranges is available, depending upon the thickness of the heat sink material. Use an appropriate grip range to securely anchor the device, yet not deform the mounting tab. The recommended rivet tool has a protruding nipple that will

allow easy insertion of the rivet and keep the tool clear of the plastic case of the device.

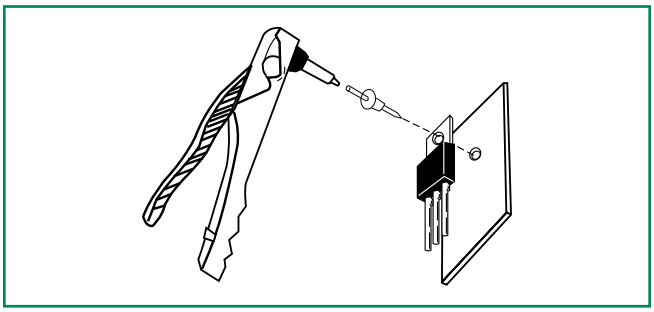


Figure AN1004.9 Pop Riveting Technique

A Milford #511 (Milford Group, Milford, CT) semi-tubular steel rivet set into a 0.129" receiving hole with a riveting machine similar to a Milford S256 is also acceptable. Contact the rivet machine manufacturer for exact details on application and set-up for optimum results.

Pneumatic or other impact riveting devices are not recommended due to the shock they may apply to the device.

Under no circumstance should any tool or hardware come into contact with the case. The case should not be used as a brace for any rotation or shearing force during mounting or in use. Non-standard size screws, nuts, and rivets are easily obtainable to avoid clearance problems.

Always use an accurate torque wrench to mount devices. No gain is achieved by overtorquing devices. In fact, overtorquing may cause the tab and case to deform or rupture, seriously damaging the device. The curve shown in Figure AN1004.10 illustrates the effect of proper torque.

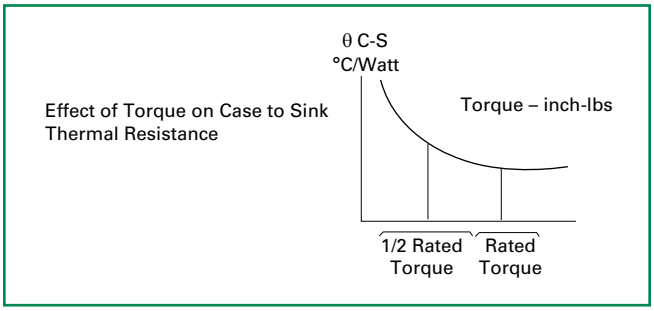


Figure AN1004.10 Effect of Torque to Sink Thermal Resistance

With proper care, the mounting tab of a device can be soldered to a surface. However, the heat required to accomplish this operation can damage or destroy the semiconductor chip or internal assembly. See "Surface Mount Soldering Recommendations" (AN1005) in this catalog.

Spring-steel clips can be used to replace torqued hardware in assembling Thyristors to heat sinks. Clips snap into heat sink slots to hold the device in place for PC board insertion. Clips are available in several sizes for various heat sink thicknesses and Thyristor case styles from *Aavid Thermalloy* in Concord, New Hampshire. A typical heatsink is shown in Figure AN1004.11

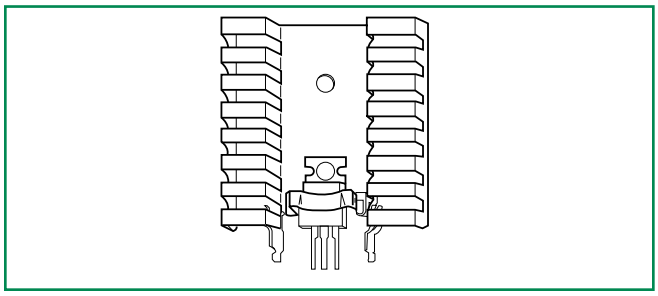


Figure AN1004.11 Typical Heat Sink Using Clips

Soldering Of Leads

A prime consideration in soldering leads is the soldering of device leads into PC boards, heat sinks, and so on. Significant damage can be done to the device through improper soldering. In any soldering process, do not exceed the data sheet lead solder temperature of +280 °C for 10 seconds, maximum, ≥1/16" from the case.

This application note presents details about the following three types of soldering:

- Hand soldering
- Wave soldering
- Dip soldering

Hand Soldering

This method is mostly used in prototype breadboarding applications and production of small modules. It has the greatest potential for misuse. The following recommendations apply to Littelfuse TO-92, TO-220, and TO-218 packages.

Select a small- to medium-duty electric soldering iron of 25 W to 45 W designed for electrical assembly application. Tip temperature should be rated from 600 °F to 800 °F (300 °C to 425 °C). The iron should have sufficient heat capacity to heat the joint quickly and efficiently in order to minimize contact time to the part. Pencil tip probes work very well. Neither heavy-duty electrical irons of greater than 45 W nor flame-heated irons and large heavy tips are recommended, as the tip temperatures are far too high and uncontrollable and can easily exceed the time-temperature limit of the part.

Littelfuse Fastpak devices require a different soldering technique. Circuit connection can be done by either quick-connect terminals or solder.

Since most quick-connect 0.250" female terminals have a maximum rating of 30 A, connection to terminals should be made by soldering wires instead of quick-connects.

Recommended wire is 10 AWG stranded wire for use with MT1 and MT2 for load currents above 30 A. Soldering

should be performed with a 100-watt soldering iron. The iron should not remain in contact with the wire and terminal longer than 40 seconds so the Fastpak Triac is not damaged.

For the Littelfuse TO-218X package, the basic rules for hand soldering apply; however, a larger iron may be required to apply sufficient heat to the larger leads to efficiently solder the joint.

Remember not to exceed the lead solder temperatures of +280 °C for 10 seconds, maximum, ≥1/16" (1.59mm) from the case.

A 60/40 or 63/37 Sn/Pb solder is acceptable. This low melting-point solder, used in conjunction with a mildly activated rosin flux, is recommended.

Insert the device into the PC board and, if required, attach the device to the heat sink before soldering. Each lead should be individually heat sinked as it is soldered. Commercially available heat sink clips are excellent for this use. Hemostats may also be used if available. Needle-nose pliers are a good heat sink choice; however, they are not as handy as stand-alone type clips.

In any case, the lead should be clipped or grasped between the solder joint and the case, as near to the joint as possible. Avoid straining or twisting the lead in any way.

Use a clean pre-tinned iron, and solder the joint as quickly as possible. Avoid overheating the joint or bringing the iron or solder into contact with other leads that are not heat sinked.

Wave Solder

Wave soldering is one of the most efficient methods of soldering large numbers of PC boards quickly and effectively. Guidelines for soldering by this method are supplied by equipment manufacturers. The boards should be pre-heated to avoid thermal shock to semiconductor components, and the time-temperature cycle in the solder wave should be regulated to avoid heating the device beyond the recommended temperature rating. A mildly activated resin flux is recommended. Figures AN1004.12 and .13 show typical heat and time conditions.

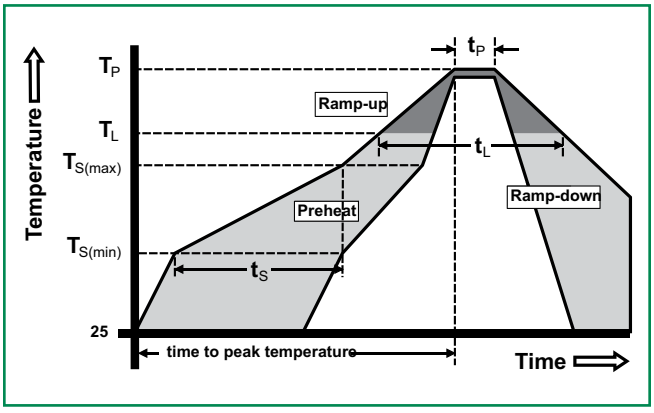


Figure AN1004.12 Reflow Soldering with Pre-heating

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 190 secs
Average ramp up rate (Liquidus Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Time (min to max) (t_s)	60 – 150 seconds
Peak Temperature (T_P)		260 °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		280°C

Figure AN1004.13 Heat and Time Table

Dip Soldering

Dip soldering is very similar to wave soldering, but it is a hand operation. Follow the same considerations as for wave soldering, particularly the time-temperature cycle which may become operator dependent because of the wide process variations that may occur. This method is not recommended.

Board or device clean-up is left to the discretion of the customer. Littelfuse devices are tolerant of a wide variety of solvents, and they conform to MIL-STD 202E method 215 "Resistance to Solvents."

Surface Mount Soldering Recommendations

Introduction

The most important consideration in reliability is achieving a good solder bond between surface mount device (SMD) and substrate since the solder provides the thermal path from the chip. A good bond is less subject to thermal fatiguing and will result in improved device reliability.

The most economic method of soldering is a process in which all different components are soldered simultaneously, such as DO-214, Compak, TO-252 devices, capacitors, and resistors.

Reflow Of Soldering

The preferred technique for mounting microminiature components on hybrid thick- and thin-film is reflow soldering.

The DO-214 is designed to be mounted directly to or on thick-film metallization which has been screened and fired on a substrate. The recommended substrates are Alumina or P.C. Board material.

Recommended metallization is silver palladium or molymanganese (plated with nickel or other elements to enhance solderability). For more information, consult Du Pont's Thick-Film handbook or the factory.

It is best to prepare the substrate by either dipping it in a solder bath or by screen printing a solder paste.

After the substrate is prepared, devices are put in place with vacuum pencils. The device may be laid in place without special alignment procedures since it is self-aligning during the solder reflow process and will be held in place by surface tension.

For reliable connections, keep the following in mind:

(1) Maximum temperature of the leads or tab during the soldering cycle does not exceed 280 °C.

(2) Flux must affect neither components nor connectors.

(3) Residue of the flux must be easy to remove.

Good flux or solder paste with these properties is available on the market. A recommended flux is Alpha 5003 diluted with benzyl alcohol. Dilution used will vary with application and must be determined empirically.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place.

Because solder paste contains a flux, it has good inherent adhesive properties which eases positioning of the components. Allow flux to dry at room temperature or in a 70 °C oven. Flux should be dry to the touch. Time required will depend on flux used.

With the components in position, the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate, on a conveyor belt running through an infrared tunnel, or by using vapor phase soldering.

In the vapor phase soldering process, the entire PC board is uniformly heated within a vapor phase zone at a temperature of approximately 215 °C. The saturated vapor phase zone is obtained by heating an inert (inactive) fluid to the boiling point. The vapor phase is locked in place by a secondary vapor. (Figure AN1005.1) Vapor phase soldering provides uniform heating and prevents overheating.

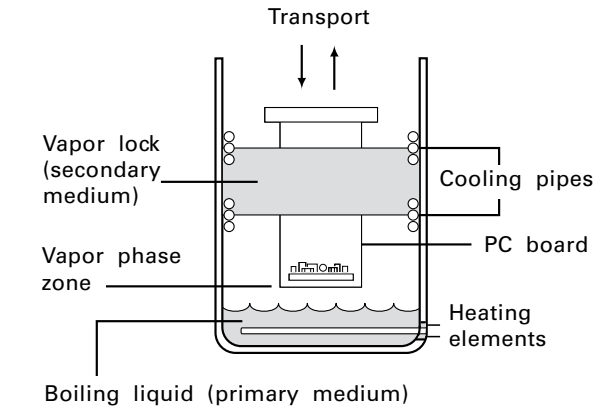


Figure AN1005.1 Principle of Vapor Phase Soldering

No matter which method of heating is used, the maximum allowed temperature of the plastic body must not exceed 250 °C during the soldering process. For additional information on temperature behavior during the soldering process, see Figure AN1005.2 and Figure AN1005.3.

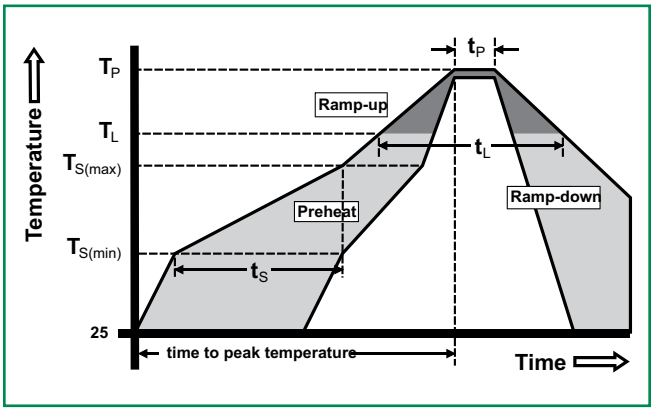


Figure AN1005.2 Reflow Soldering Profile

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 190 secs
Average ramp up rate (Liquidus Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Time (min to max) (t_s)	60 – 150 seconds
Peak Temperature (T_P)		260 °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		280°C

Reflow Soldering Zones

Zone 1: Initial Pre-heating Stage (25 °C to 150 °C)

- Excess solvent is driven off.
- PCB and Components are gradually heated up.
- Temperature gradient shall be <2.5 °C/Sec.

Zone 2: Soak Stage (150 °C to 180 °C)

- Flux components start activation and begin to reduce the oxides on component leads and PCB pads.
- PCB components are brought nearer to the temperature at which solder bonding can occur.
- Soak allows different mass components to reach the same temperature.
- Activated flux keeps metal surfaces from re-oxidizing.

Zone 3: Reflow Stage (180 °C to 235 °C)

- Paste is brought to the alloy's melting point.
- Activated flux reduces surface tension at the metal interface so metallurgical bonding occurs.

Zone 4: Cool-down Stage (180 °C to 25 °C)

Assembly is cooled evenly so thermal shock to the components or PCB is reduced.

The surface tension of the liquid solder tends to draw the leads of the device towards the center of the soldering area and so has a correcting effect on slight mispositionings. However, if the layout is not optimized, the same effect can result in undesirable shifts, particularly if the soldering areas on the substrate and the components are not concentrically arranged. This problem can be solved by using a standard contact pattern which leaves sufficient scope for the self-positioning effect (Figure AN1005.3 and Figure AN1005.4) Figure AN1005.5 shows the reflow soldering procedure.

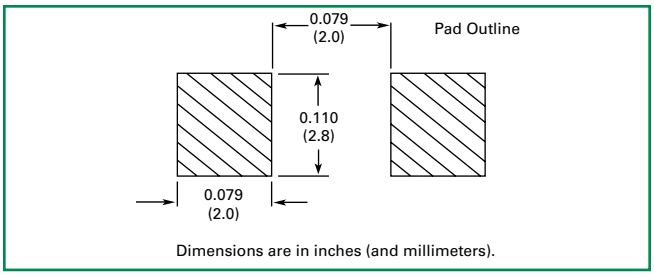


Figure AN1005.3 Minimum Required Dimensions of Metal Connection of Typical DO-214 Pads on Hybrid Thick- and Thin-film Substrates

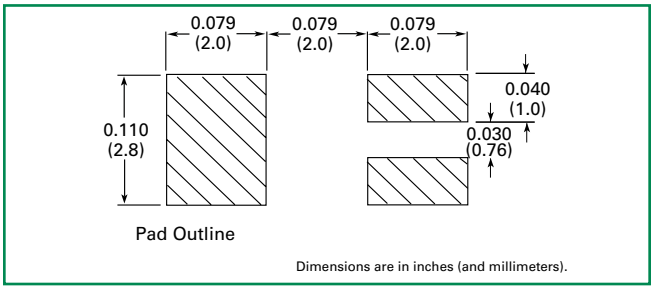


Figure AN1005.4 Modified DO-214 Compak — Three-leaded Surface Mount Package

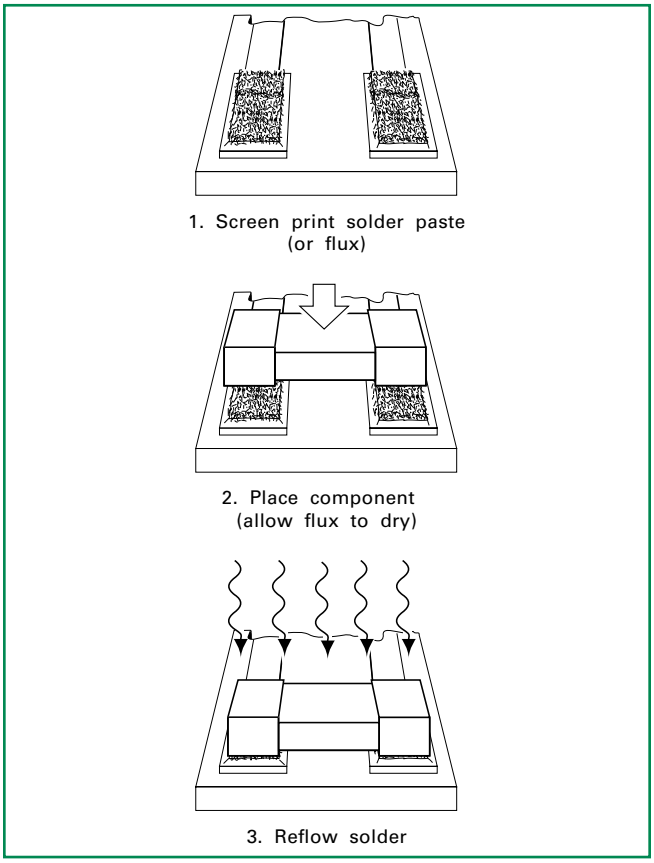


Figure AN1005.5 Reflow Soldering Procedure

After the solder is set and cooled, visually inspect the connections and, where necessary, correct with a soldering iron. Finally, the remnants of the flux must be removed carefully.

Use vapor degrease with an azeotrope solvent or equivalent to remove flux. Allow to dry.

After the drying procedure is complete, the assembly is ready for testing and/or further processing.

Wave Soldering

Wave soldering is the most commonly used method for soldering components in PCB assemblies. As with other soldering processes, a flux is applied before soldering. After the flux is applied, the surface mount devices are glued into place on a PC board. The board is then placed in contact with a molten wave of solder at a temperature between 240 °C and 260 °C, which affixes the component to the board.

Dual wave solder baths are also in use. This procedure is the same as mentioned above except a second wave of solder removes excess solder.

Although wave soldering is the most popular method of PCB assembly, drawbacks exist. The negative features include solder bridging and shadows (pads and leads not completely wetted) as board density increases. Also, this method has the sharpest thermal gradient. To prevent thermal shock, some sort of pre-heating device must be used. Figure AN1005.6 shows the procedure for wave soldering PCBs with surface mount devices only. Figure AN1005.7 shows the procedure for wave soldering PCBs with both surface mount and leaded components.

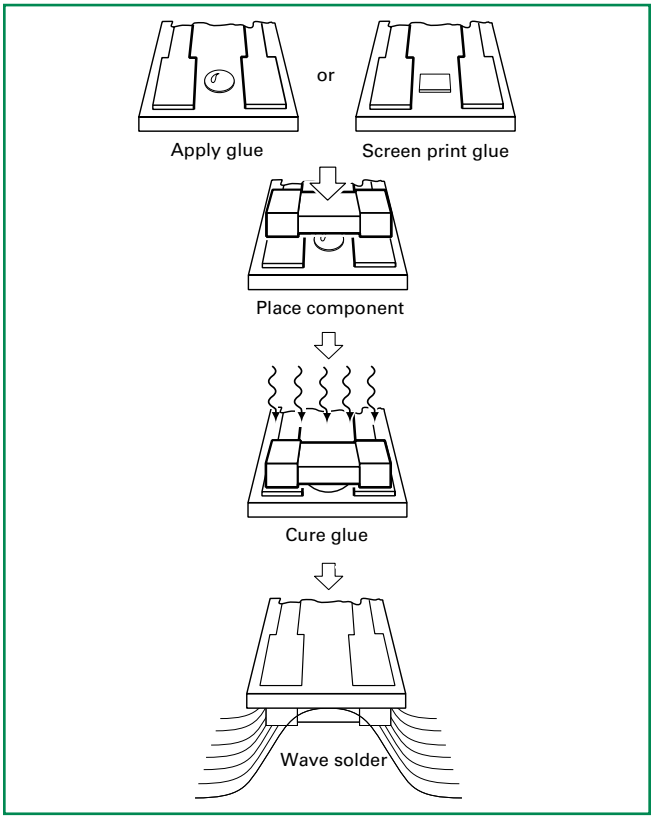


Figure AN1005.6 Wave Soldering PCBs With Surface Mount Devices Only

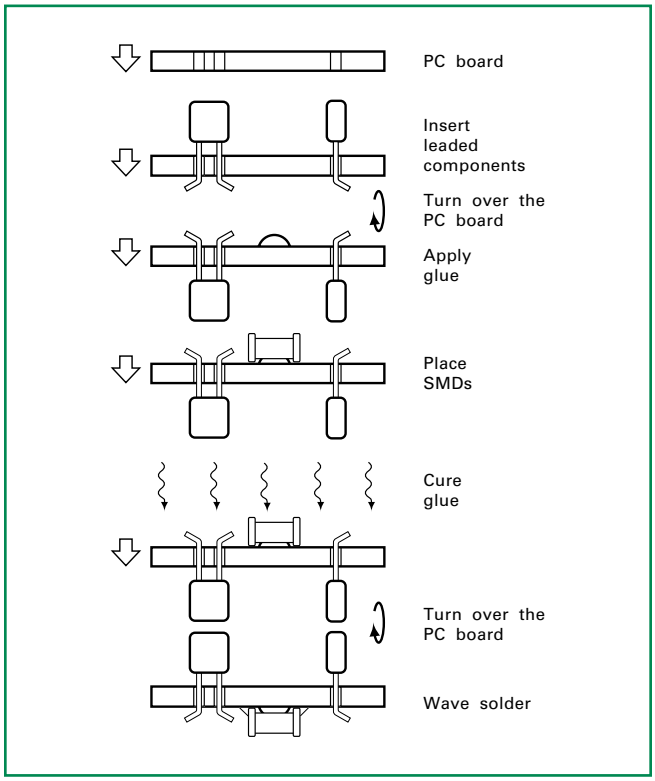


Figure AN1005.7 Wave Soldering PCBs With Both Surface Mount and Leaded Components

Immersion Soldering

Maximum allowed temperature of the soldering bath is 235 °C. Maximum duration of soldering cycle is five seconds, and forced cooling must be applied.

Hand Soldering

It is possible to solder the DO-214, Compak, and TO-252 devices with a miniature hand-held soldering iron, but this method has particular drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits.

Recommended Metal-alloy

(1) 63/37 Sn/Pb - non - RoHS

(2) (SAC 305) 96.5/3/0.5 Sn/Ag/Cu - RoHS

Pre-Heating

Pre-heating is recommended for good soldering and to avoid damage to the DO-214, Compak, TO-252 devices, other components, and the substrate. Maximum pre-heating temperature is 165 °C while the maximum pre-heating duration may be 10 seconds. However, atmospheric pre-heating is permissible for several minutes provided temperature does not exceed 125 °C.

Gluing Recommendations

Prior to wave soldering, surface mount devices (SMDs) must be fixed to the PCB or substrate by means of an appropriate adhesive. The adhesive (in most cases a multicomponent adhesive) has to fulfill the following demands:

- Uniform viscosity to ensure easy coating
- No chemical reactions upon hardening in order not to deteriorate component and PC board
- Straightforward exchange of components in case of repair

Low-temperature Solder for Reducing PC Board Damage

In testing and troubleshooting surface-mounted components, changing parts can be time consuming. Moreover, desoldering and soldering cycles can loosen and damage circuit-board pads. Use low-temperature solder to minimize damage to the PC board and to quickly remove a component. One low-temperature alloy is indium-tin, in a 50/50 mixture. It melts between 118 °C and 125 °C, and tin-lead melts at 183 °C. If a component needs replacement, holding the board upside down and heating the area with a heat gun will cause the component to fall off. Performing the operation quickly minimizes damage to the board and component.

Proper surface preparation is necessary for the In-Sn alloy to wet the surface of the copper. The copper must be clean, and you must add flux to allow the alloy to flow freely. You can use rosin dissolved in alcohol. Perform the following steps:

(1) Cut a small piece of solder and flow it onto one of the pads.

(2) Place the surface-mount component on the pad and melt the soldered pad to its pin while aligning the part. (This operation places all the pins flat onto their pads.)

(3) Cut small pieces of the alloy solder and flow each piece onto each of the other legs of the component.

Indium-tin solder is available from ACI Alloys, San Jose, CA and Indium Corporation of America, Utica, NY.

Multi-use Footprint

Package soldering footprints can be designed to accommodate more than one package. Figure AN1005.8 shows a footprint design for using both the Compak and an SOT-223. Using the dual pad outline makes it possible to use more than one supplier source.

Cleaning Recommendations

Using solvents for PC board or substrate cleaning is permitted from approximately 70 °C to 80 °C.

The soldered parts should be cleaned with azeotrope solvent followed by a solvent such as methol, ethyl, or isopropyl alcohol.

Ultrasonic cleaning of surface mount components on PCBs or substrates is possible.

The following guidelines are recommended when using ultrasonic cleaning:

- Cleaning agent: Isopropanol
- Bath temperature: approximately 30 °C
- Duration of cleaning: MAX 30 seconds
- Ultrasonic frequency: 40 kHz
- Ultrasonic changing pressure: approximately 0.5 bar

Cleaning of the parts is best accomplished using an ultrasonic cleaner which has approximately 20 W of output per one liter of solvent. Replace the solvent on a regular basis.

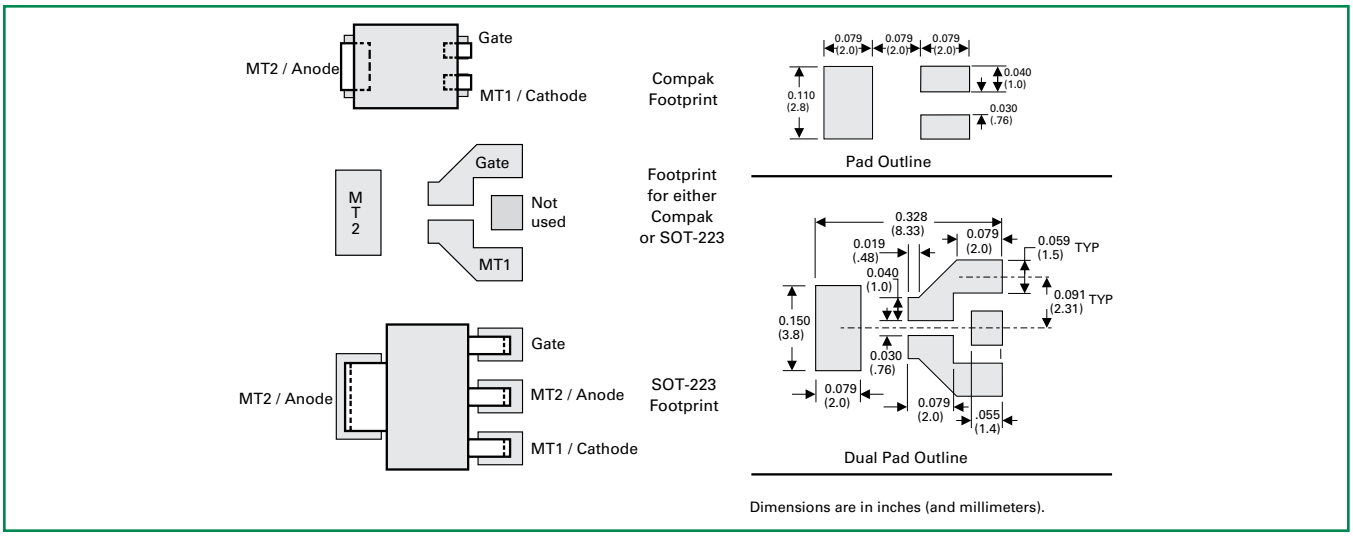


Figure AN10058 Dual Footprint for Compak Package

Thyristor and Rectifier Testing Using Curve Tracers

Introduction

One of the most useful and versatile instruments for testing semiconductor devices is the curve tracer (CT). Tektronix is the best known manufacturer of curve tracers and produces four basic models: 575, 576, 577 and 370. These instruments are specially adapted CRT display screens with associated electronics such as power supplies, amplifiers, and variable input and output functions that allow the user to display the operating characteristics of a device in an easy-to-read, standard graph form. Operation of Tektronix CTs is simple and straightforward and easily taught to non-technical personnel. Although widely used by semiconductor manufacturers for design and analytical work, the device consumer will find many uses for the curve tracer, such as incoming quality control, failure analysis, and supplier comparison. Curve tracers may be easily adapted for go-no go production testing. Tektronix also supplies optional accessories for specific applications along with other useful hardware.

Tektronix Equipment

Although Tektronix no longer produces curve tracer model 575, many of the units are still operating in the field, and it is still an extremely useful instrument. The 576, 577 and 370 are current curve tracer models and are more streamlined in their appearance and operation. The 577 is a less elaborate version of the 576, yet retains all necessary test functions.

The following basic functions are common to all curve tracers:

- **Power supply** supplies positive DC voltage, negative DC voltage, or AC voltage to bias the device. Available power is varied by limiting resistors.
- **Step generator** supplies current or voltage in precise steps to control the electrode of the device. The number, polarity, and frequency of steps are selectable.
- **Horizontal amplifier** displays power supply voltage as applied to the device. Scale calibration is selectable.
- **Vertical amplifier** displays current drawn from the supply by the device. Scale calibration is selectable.

Curve tracer controls for beam position, calibration, pulse operation, and other functions vary from model to model. The basic theory of operation is that for each curve one terminal is driven with a constant voltage or current and the other one is swept with a half sinewave of voltage. The driving voltage is stepped through several values, and a different trace is drawn on each sweep to generate a family of curves.

Limitations, Accuracy, and Correlation

Although the curve tracer is a highly versatile device, it is not capable of every test that one may wish to perform on semiconductor devices such as dv/dt, secondary reverse breakdown, switching speeds, and others. Also, tests at very high currents and/or voltages are difficult to conduct accurately and without damaging the devices. A special high-current test fixture available from Tektronix can extend operation to 200 A pulsed peak. Kelvin contacts available on the 576 and 577 eliminate inaccuracy in voltage measured at high current (V_{TM}) by sensing voltage drop due to contact resistance and subtracting from the reading.

Accuracy of the unit is within the published manufacturer's specification. Allow the curve tracer to warm up and stabilize before testing begins. Always expand the horizontal or vertical scale as far as possible to increase the resolution. Be judicious in recording data from the screen, as the trace line width and scale resolution factor somewhat limit the accuracy of what may be read. Regular calibration checks of the instrument are recommended. Some users keep a selection of calibrated devices on hand to verify instrument operation when in doubt. Re-calibration or adjustment should be performed only by qualified personnel.

Often discrepancies exist between measurements taken on different types of instrument. In particular, most semiconductor manufacturers use high-speed, computerized test equipment to test devices. They test using very short pulses. If a borderline unit is then measured on a curve tracer, it may appear to be out of specification. The most common culprit here is heat. When a semiconductor device increases in temperature due to current flow, certain characteristics may change, notably gate characteristics on SCRs, gain on transistors, leakage, and so on. It is very difficult to operate the curve tracer in such a way as to eliminate the heating effect. Pulsed or single-trace operation helps reduce this problem, but care should be taken in comparing curve tracer measurements to computer tests. Other factors such as stray capacitances, impedance matching, noise, and device oscillation also may create differences.

Safety (Cautions and Warnings)

Adhere rigidly to Tektronix safety rules supplied with each curve tracer. No attempt should be made to defeat any of the safety interlocks on the device as the curve tracer can produce a lethal shock. Also, older 575 models do not have the safety interlocks as do the new models. Take care never to touch any device or open the terminal while energized.

WARNING: Devices on the curve tracer may be easily damaged from electrical overstress.

Follow these rules to avoid destroying devices:

- Familiarize yourself with the expected maximum limits of the device.
- Limit the current with the variable resistor to the minimum necessary to conduct the test.
- Increase power slowly to the specified limit.
- Watch for device "runaway" due to heating.
- Apply and increase gate or base drive slowly and in small steps.
- Conduct tests in the minimum time required.

General Test Procedures

Read all manuals before operating a curve tracer.

Perform the following manufacturer's equipment check:

1. Turn on and warm up curve tracer, but turn off, or down, all power supplies.
2. Correctly identify terminals of the device to be tested. Refer to the manufacturer's guide if necessary.
3. Insert the device into the test fixture, matching the device and test terminals.
4. Remove hands from the device and/or close interlock cover.
5. Apply required bias and/or drive.
6. Record results as required.
7. Disconnect all power to the device before removing.

Model 576 Curve Tracer Procedures

The following test procedures are written for use with the model 576 curve tracer. (Figure AN1006.1)

See "Model 370 Curve Tracer Procedure Notes" on page AN1006-16 and "Model 577 Curve Tracer Procedure Notes" on page AN1006-18 for setting adjustments required when using model 370 and 577 curve tracers.

The standard 575 model lacks AC mode, voltage greater than 200 V, pulse operations, DC mode, and step offset controls. The 575 MOD122C does allow voltage up to 400 V, including 1500 V in an AC mode. Remember that at the time of design, the 575 was built to test only transistors and diodes. Some ingenuity, experience, and external hardware may be required to test other types of devices.

For further information or assistance in device testing on Tektronix curve tracers, contact the Littelfuse Applications Engineering group.

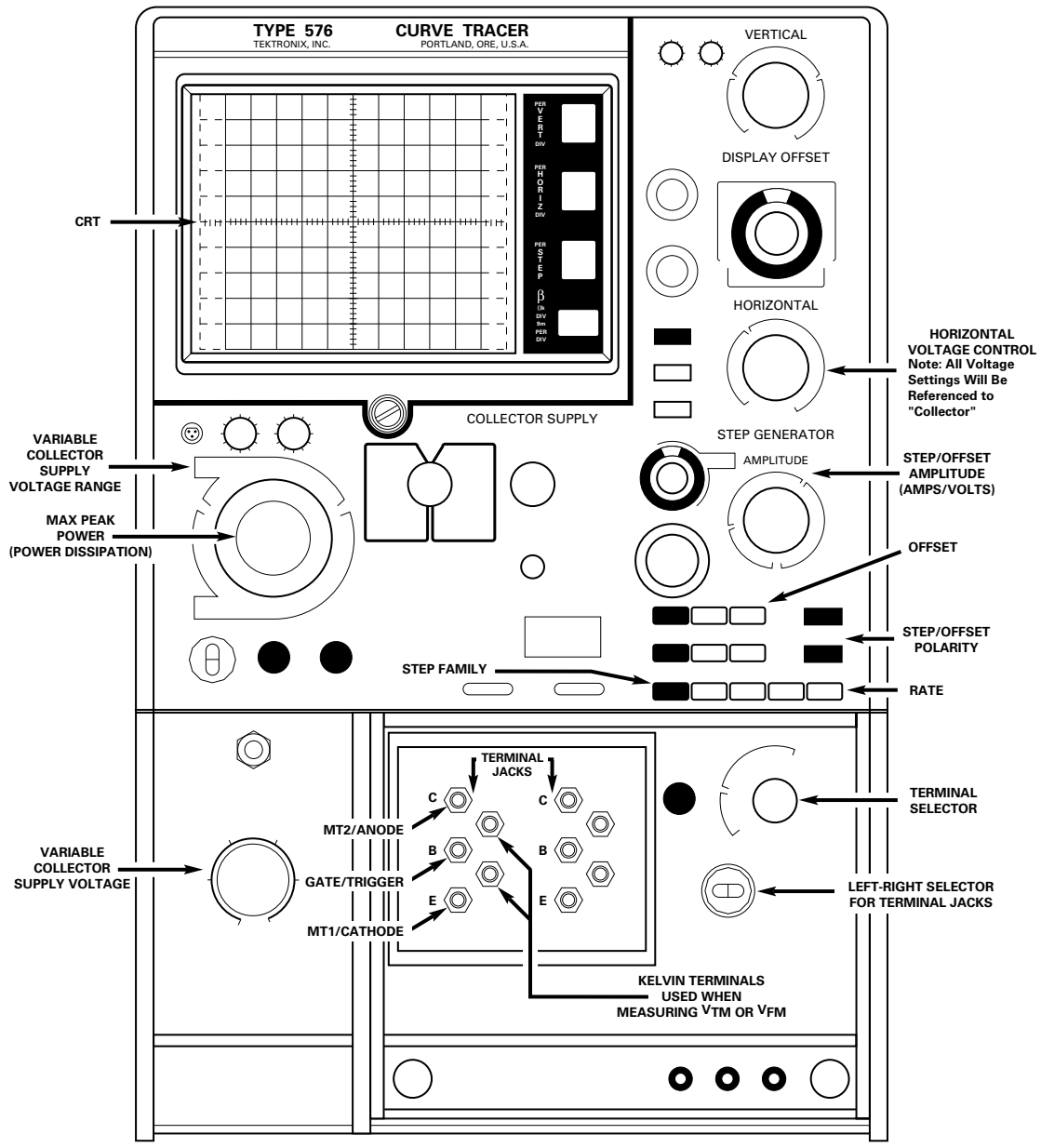


Figure AN1006.1 Tektronix Model 576 Curve Tracer

Power Rectifiers

The rectifier is a unidirectional device which conducts when forward voltage (above 0.7 V) is applied.

To connect the rectifier:

1. Connect *Anode to Collector Terminal (C).*
2. Connect *Cathode to Emitter Terminal (E).*

To begin testing, perform the following procedures.

Procedure 1: V_{RRM} and I_{RM}

To measure the V_{RRM} and I_{RM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 V.*(*2000 V on 370*)
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level (*100 V/DIV* for 400 V and 600 V devices and *50 V/DIV for 200 V devices*).
3. Set **Mode** to *Leakage.*
4. Set **Vertical** knob to *100 µA/DIV.* (Due to leakage setting, the CRT readout will be 100 nA per division.)
5. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
6. Set **Polarity** to (-).
7. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370)
8. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
9. Increase **Variable Collector Supply Voltage** to the rated V_{RRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.2)

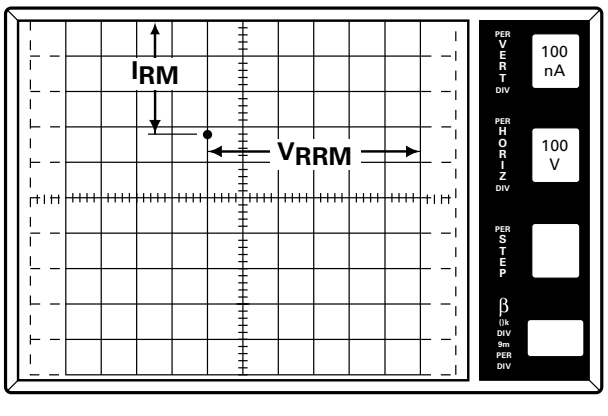


Figure AN1006.2 I_{RM} = 340 nA at V_{RRM} = 600 V

Procedure 2: V_{FM}

Before testing, note the following:

- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of VFM will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.
- Due to the current limitations of standard curve tracer model 576, V_{FM} cannot be tested at rated current without a Tektronix model 176 high-current module. The procedure below is done at $I_{T(RMS)}$ = 10 A (20 A_{PK}). This test parameter allows the use of a standard curve tracer and still provides an estimate of whether V_{FM} is within specification.

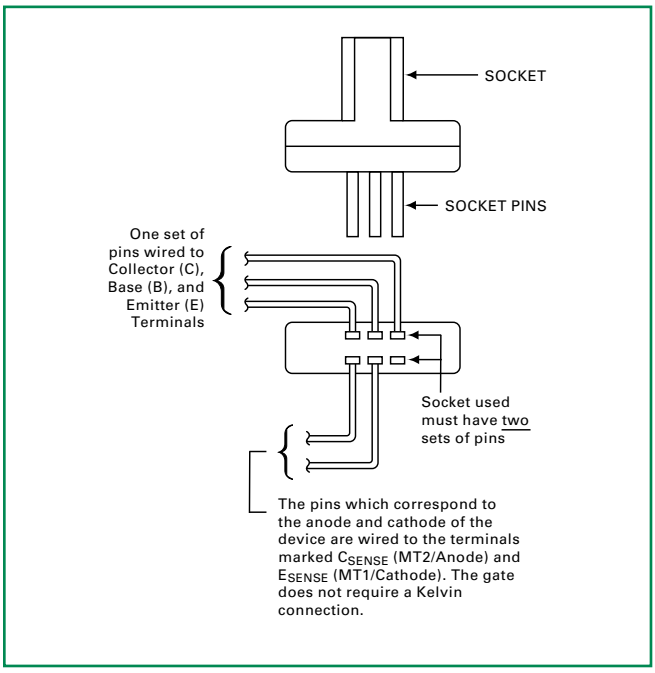


Figure AN1006.3 Instructions for Wiring Kelvin Socket

To measure the V_{FM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *15 Max Peak Volts.* (*16 V on 370*)
2. Set **Horizontal** knob to *0.5 V/DIV.*
3. Set **Mode** to *Norm.*
4. Set **Vertical** knob to *2 A/DIV.*
5. Set **Power Dissipation** to *220 W* (*100 W on 577*).
6. Set **Polarity** to (+).
7. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
8. Increase **Variable Collector Supply Voltage** until current reaches 20 A.

WARNING: Limit test time to 15 seconds maximum.

To measure V_{FM}, follow along horizontal scale to the point where the trace crosses the 20 A axis. The distance from the left-hand side of scale to the crossing point is the V_{FM} value. (Figure AN1006.4)

Note: Model 370 current is limited to 10 A.

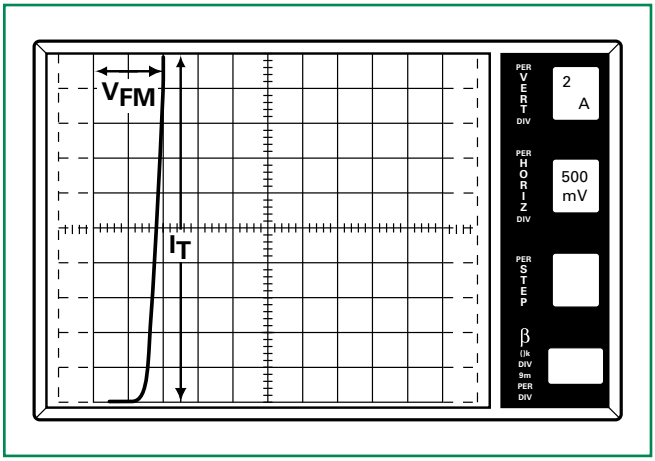


Figure AN1006.4 V_{FM} = 1 V at I_{PK} = 20 A

SCRs

SCRs are half-wave unidirectional rectifiers turned on when current is supplied to the gate terminal. If the current supplied to the gate is to be in the range of 12 µA and 500 µA, then a sensitive SCR is required; if the gate current is between 1 mA and 50 mA, then a non-sensitive SCR is required.

To connect the rectifier:

1. Connect *Anode to Collector Terminal (C).*
2. Connect *Cathode to Emitter Terminal (E).*

Note: When sensitive SCRs are being tested, a 1 kΩ resistor must be connected between the gate and the cathode, except when testing I_{GT}.

To begin testing, perform the following procedures.

Procedure 1: V_{DRM} / V_{RRM} / I_{DRM} / I_{RRM}

To measure the V_{DRM} / V_{RRM} / I_{DRM}, and I_{RRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to or greater than the device's V_{DRM} rating.)
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level. (The *100 V/DIV* scale should be used for testing devices having a V_{DRM} value of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 300 V to 500 V, and so on.)
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.*(*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
7. Set **Vertical** knob to approximately ten times the maximum leakage current (I_{DRM}, I_{RRM}) specified for the device. (For sensitive SCRs, set to *50 µA.*)

Note: The CRT screen readout should show 1% of the maximum leakage current if the vertical scale is divided by 1,000 when leakage current mode is used.

Procedure 2: V_{DRM} / I_{DRM}

To measure the V_{DRM} and I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
2. Set **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.5)

WARNING: Do NOT exceed V_{DRM}/V_{RRM} rating of SCRs, Triacs, or Quadracs. These devices can be damaged.

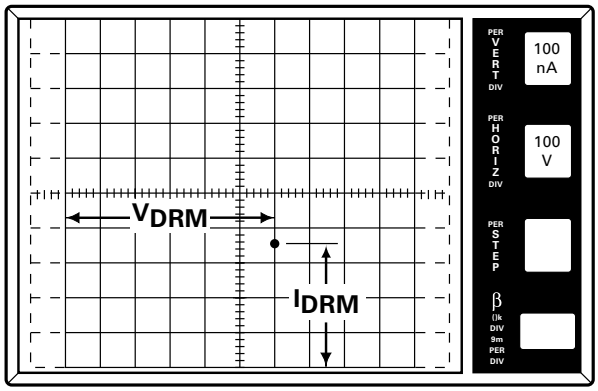


Figure AN1006.5 I_{DRM} = 350 nA at V_{DRM} = 600 V

Procedure 3: V_{RRM} / I_{RRM}

To measure the V_{RRM} and I_{RRM} parameter:

1. Set **Polarity** to (-).
2. Repeat Steps 1 and 2 (V_{DRM}, I_{DRM}) except substitute V_{RRM} value for V_{DRM}. (Figure AN1006.6)

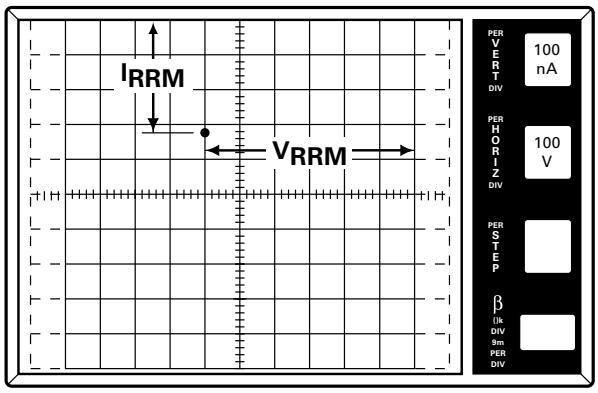


Figure AN1006.6 I_{RRM} = 340 nA at V_{RRM} = 600 V

Procedure 4: V_{TM}

To measure the V_{TM} parameter:

1. Set **Terminal Selector** to *Step Generator-Emitter Grounded.*
2. Set **Polarity** to *(+).*
3. Set **Step/Offset Amplitude** to twice the maximum I_{GT} rating of the device (to ensure the device turns on). For sensitive SCRs, set to *2 mA.*
4. Set **Max Peak Volts** to *15 V.* (*16 V* on 370)
5. Set **Offset** by depressing *0* (zero).
6. Set **Rate** by depressing *Norm.*
7. Set **Step Family** by depressing *Rep* (repetitive).
8. Set **Mode** to *DC.*
9. Set **Horizontal** knob to *0.5 V/DIV.*
10. Set **Power Dissipation** to *220 W* (*100 W on 577*).
11. Set **Number of Steps** to *1.* (Set steps to 0 (zero) on 370.)
12. Set **Vertical** knob to a sufficient setting to allow the viewing of 2 times the $I_{T(RMS)}$ rating of the device ($I_{T(peak)}$) on CRT.

    Before continuing with testing, note the following:

    (1) Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 6 A or less should be tested on standard curve tracer. If testing devices above 6 A, a Tektronix model 176 high-current module is required.

    (2) A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in the fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connectors.
13. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
14. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is twice the $I_{T(RMS)}$ rating of theSCR under test.

Note: Model 370 current is limited to 10 A.

WARNING: Limit test time to 15 seconds maximum after the *Variable Collector Supply* has been set to $I_{T(peak)}$, After the *Variable Collector Supply Voltage* has been set to $I_{T(peak)}$, the test time can automatically be shortened by changing *Step Family* from repetitive to single by depressing the *Single button.*

To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. The distance from the left-hand side of scale to the intersection point is the V_{TM} value. (Figure AN1006.7)

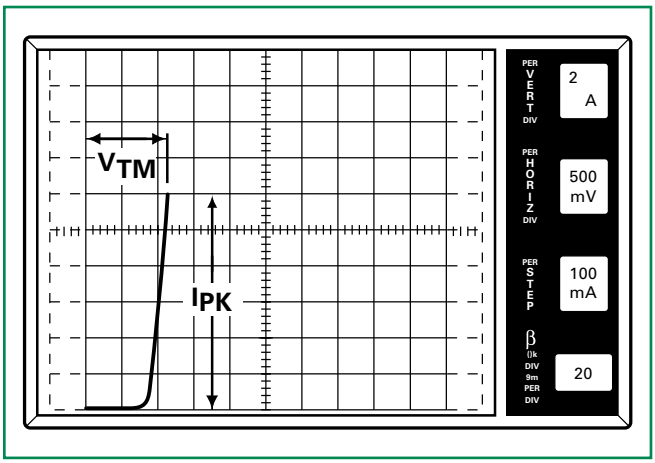


Figure AN1006.7 V_{TM} = 1.15 V at $I_{T(peak)}$ = 12 A

Procedure 5: I_H

To measure the I_H parameter:

1. Set **Polarity** to (+).
2. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370)
3. Set **Max Peak Volts** to *75 V.* (80 V on 370)
4. Set **Mode** to *DC.*
5. Set **Horizontal** knob to *Step Generator.*
6. Set **Vertical** knob to approximately 10 percent of the maximum I_H specified.

Note: Due to large variation of holding current values, the scale may have to be adjusted to observe holding current.

7. Set **Number of Steps** to *1.*
8. Set **Offset** by depressing *0*(zero). (Press *Aid* and Oppose at the same time on 370.)
9. Set **Step/Offset Amplitude** to twice the maximum I_{GT} of the device.
10. Set **Terminal Selector** to *Step Generator-Emitter Grounded.*
11. Set **Step Family** by depressing *Single.*
12. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
13. Increase **Variable Collector Supply Voltage** to maximum position (*100*).
14. Set **Step Family** by depressing *Single.* (This could possibly cause the dot on CRT to disappear, depending on the vertical scale selected.)
15. Change **Terminal Selector** from *Step Generator-Emitter Grounded* to *Open Base-Emitter Grounded.*
16. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line becomes a dot, represents the holding current value. (Figure AN1006.8)

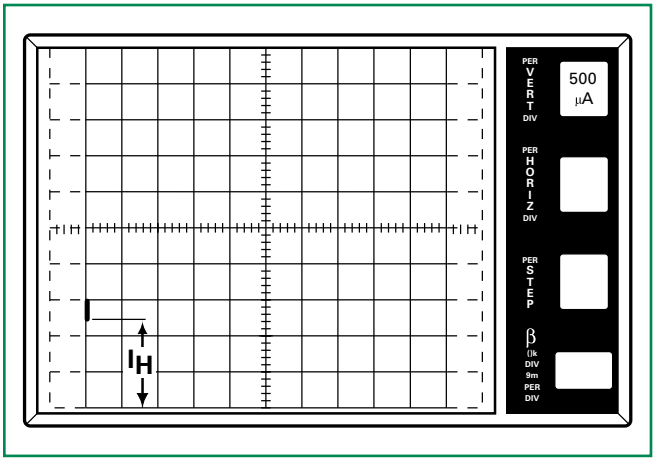


Figure AN1006.8 I_H = 1.2 mA

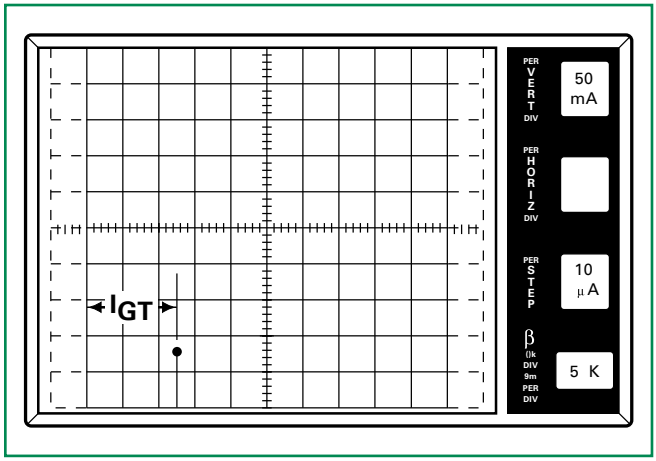


Figure AN1006.9 I_{GT} = 25 µA

Procedure 6: I_{GT} and V_{GT}

To measure the I_{GT} and V_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps** to 1.
3. Set **Offset** by depressing *Aid*.
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and *Oppose* at the same time on 370.)
5. Set *Terminal Selector* to *Step Generator-Emitter Grounded*.
6. Set **Mode** to *Norm*.
7. Set **Max Peak Volts** to *15 V*. (*16 V* on 370)
8. Set **Power Dissipation** to *2.2 W*. (*2 W* on 370) For sensitive SCRs, set at 0.5 W. (*0.4 W* on 370)
9. Set **Horizontal** knob to *2 V/DIV*.
10. Set **Vertical** knob to *50 mA/DIV*.
11. Increase **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
12. After 12 V setting is completed, change **Horizontal** knob to *Step Generator*.

Procedure 7: I_{GT}

To measure the I_{GT} parameter:

1. Set **Step/Offset Amplitude** to 20% of maximum rated I_{GT}.

   Note: R_{GK} should be removed when testing I_{GT}
2. Set **Left-Right Terminal Jack Selector** to correspond with location of the test fixture.
3. Gradually increase **Offset Multiplier** until device reaches the conduction point. (Figure AN1006.9) Measure I_{GT} by following horizontal axis to the point where the vertical line crosses axis. This measured value is I_{GT}. (On 370, I_{GT} will be numerically displayed on screen under offset value.)

Procedure 8: V_{GT}

To measure the V_{GT} parameter:

1. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and *Oppose* at the same time on 370.)
2. Set **Step Offset Amplitude** to 20% rated V_{GT}.
3. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
4. Gradually increase **Offset Multiplier** until device reaches the conduction point. (Figure AN1006.10) Measure V_{GT} by following horizontal axis to the point where the vertical line crosses axis. This measured value is V_{GT}. (On 370, V_{GT} will be numerically displayed on screen, under offset value.)

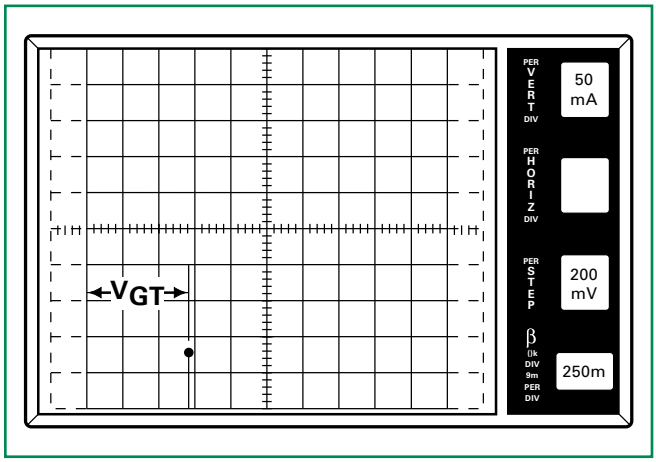


Figure AN1006.10 V_{GT} = 580 mV

Triacs

Triacs are full-wave bidirectional AC switches turned on when current is supplied to the gate terminal of the device. If gate control in all four quadrants is required, then a sensitive gate Triac is needed, whereas a standard Triac can be used if gate control is only required in Quadrants I through III.

To connect the Triac:

1. Connect the *Gate* to the *Base Terminal* (B).
2. Connect *MT1* to the *Emitter Terminal* (E).
3. Connect *MT2* to the *Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, (-)I_{DRM}

Note: The (+) and (-) symbols are used to designate the polarity MT2 with reference to MT1.

To measure the (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, and (-)I_{DRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to the device's V_{DRM} rating.)

   WARNING: DO NOT exceed V_{DRM}/V_{RRM} rating of SCRs, Triacs, or Quadracs. These devices can be damaged.
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level. (The *100 V/DIV* scale should be used for testing devices having a V_{DRM} rating of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 30 V to 500 V, and so on.)
3. Set **Mode** to *Leakage.*
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
7. Set **Vertical** knob to ten times the maximum leakage current (I_{DRM}) specified for the device.

Note: The CRT screen readout should show 1% of the maximum leakage current. The vertical scale is divided by 1,000 when leakage mode is used.

Procedure 2: (+)V_{DRM}, (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set Left-Right Terminal Jack Selector to correspond with location of the test fixture.
2. Increase Variable Collector Supply Voltage to the rated V_{DRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.11)

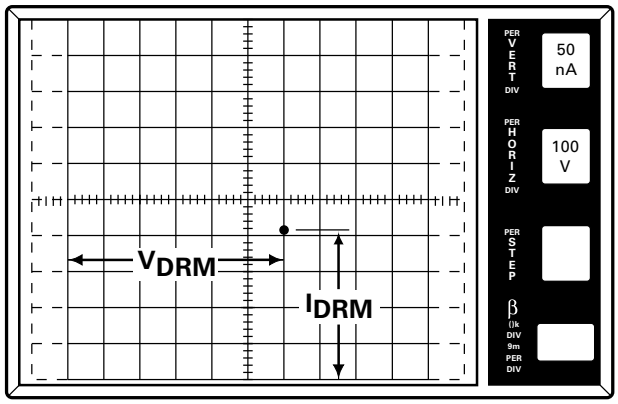


Figure AN1006.11 (+)I_{DRM} = 205 nA at (+)V_{DRM} = 600 V

Procedure 3: (-)V_{DRM}, (-)I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (-).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of the screen.)

Procedure 4: $V_{TM\ (Forward\ and\ Reverse)}$

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Terminal Selector** to Step Generator-Emitter Grounded.
2. Set **Step/Offset Amplitude** to twice the maximum I_{GT} rating of the device (to insure the device turns on).
3. Set **Variable Collector Supply Voltage Range** to *15 V Max Peak volts.* (*16 V* on 370)
4. Set **Offset** by depressing *0* (zero).
5. Set **Rate** by depressing *Norm.*
6. Set **Step Family** by depressing *Rep* (Repetitive).
7. Set **Mode** to *Norm.*
8. Set **Horizontal** knob to *0.5 V/DIV.*
9. Set **Power Dissipation** to *220 W* (*100 W* on 577).
10. Set **Number of Steps** to *1.*
11. Set **Step/Offset Polarity** to non-inverted (button extended; on 577 button depressed).
12. Set **Vertical** knob to a sufficient setting to allow the viewing of 1.4 times the $I_{T(RMS)}$ rating of the device [$I_{T(peak)}$ on CRT].

Note the following:

- Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 8 A or less should be tested on standard curve tracer. If testing devices above 8 A, a Tektronix model 176 high-current module is required.
- A Kelvin test fixture is required for this test. If a

Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.

Procedure 5: $V_{TM\ (Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times $I_{T(RMS)}$ rating of the Triac under test.

   Note: Model 370 current is limited to 10 A.

WARNING: Limit test time to 15 seconds maximum. After the *Variable Collector Supply Voltage* has been set to $I_{T(peak)}$, the test time can automatically be set to a short test time by changing *Step Family* from repetitive to single by depressing the *Single* button.

To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. The distance from the left-hand side of scale to the crossing point is the V_{TM} value. (Figure AN1006.12)

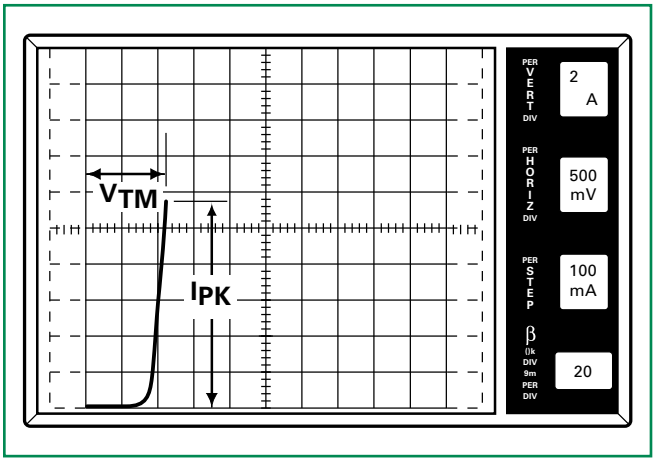


Figure AN1006.12 $V_{TM\ (forward)}$ = 1.1 V at I_{PK} = 11.3 A (8 A rms)

Procedure 6: $V_{TM\ (Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

1. Set **Polarity** to (-).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$.
4. Measure $V_{TM(Reverse)}$ similar to Figure AN1006.12, except from upper right hand corner of screen.

Procedure 7: $I_{H(Forward\ and\ Reverse)}$

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Step/Offset Amplitude** to twice the I_{GT} rating of the device.
2. Set **Power Dissipation** to *10 W*.
3. Set **Max Peak Volts** to *75 V*. (*80 V* on 370)
4. Set **Mode** to *DC*.
5. Set **Horizontal** knob to *Step Generator*.
6. Set **Vertical** knob to approximately 10% of the maximum I_H specified.

   Note: Due to large variation of holding current values, the scale may have to be adjusted to observe holding current.
7. Set **Number of Steps** to *1*.
8. Set **Step/Offset Polarity** to non-inverted (button extended, on 577 button depressed).
9. Set **Offset** by depressing *0* (zero). (Press *Aid* and *Oppose* at same time on 370.)
10. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.

Procedure 8: $I_{H(Forward)}$

To measure the $I_{H\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Increase **Variable Collector Supply Voltage** to maximum position (*100*).
4. Set **Step Family** by depressing *Single*.

   This could possibly cause the dot on the CRT to disappear, depending on the vertical scale selected).
5. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line becomes a dot, represents the holding current value. (Figure AN1006.13)

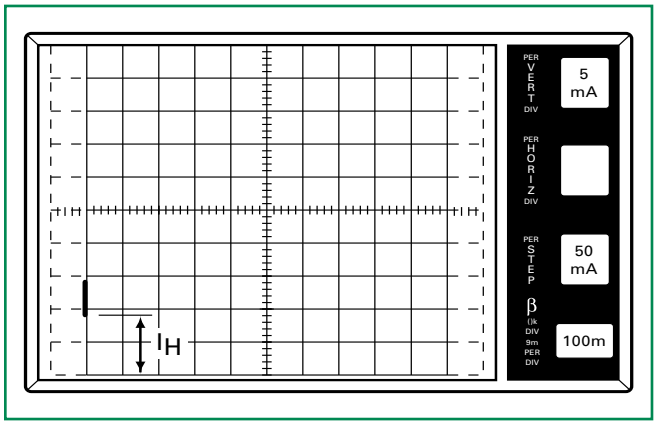


Figure AN1006.13 $I_{H\ (Forward)}$ = 8.2 mA

Procedure 9: $I_{H(Reverse)}$

To measure the $I_{H (Reverse)}$ parameter:

1. Set **Polarity** to (-).
2. Repeat Procedure 7 measuring $I_{H(Reverse)}$. (Read measurements from upper right corner of the screen.)

Procedure 10: I_{GT}

To measure the I_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps**to *1*. (Set number of steps to *0* (zero) on 370.)
3. Set **Offset** by depressing *Aid*. (On 577, also set **Zero** button to *Offset*. Button is extended.)
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and Oppose at same time on 370.)
5. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.
6. Set **Mode** to **Norm.**
7. Set **Max Peak Volts** to *15 V*. (*16 V* on 370)
8. Set **Power Dissipation** to *10 W*.
9. Set **Step Family** by depressing *Single*.
10. Set **Horizontal** knob to *2 V/DIV*.
11. Set **Vertical** knob to *50 mA/DIV*.
12. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
13. Set **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
14. After 12 V setting is completed, change **Horizontal** knob to *Step Generator*.

Procedure 11: I_{GT} - Quadrant I [MT2 (+) Gate (+)]

To measure the I_{GT} - Quadrant I parameter:

1. Set **Step/Offset Amplitude** to approximately 10% of rated I_{GT}.
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Gradually increase **Offset Multiplier** until device reaches conduction point. (Figure AN1006.14) Measure I_{GT} by following horizontal axis to the point where the vertical line passes through the axis. This measured value is I_{GT}. (On 370, I_{GT} is numerically displayed on screen under offset value.)

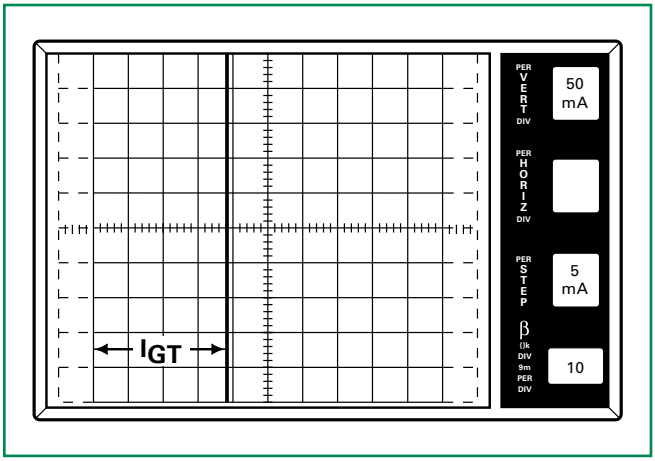


Figure AN1006.14 I_{GT} in Quadrant I = 18.8 mA

Procedure 12: I_{GT} - Quadrant II [MT2 (+) Gate (-)]

To measure the I_{GT} - Quadrant II parameter:

1. Set **Step/Offside Polarity** by depressing Invert (release button on 577).
2. Set **Polarity** to (+).
3. Set observed dot to bottom right corner of CRT grid by turning the horizontal position knob. When Quadrant II testing is complete, return dot to original position.
4. Repeat Procedure 11.

Procedure 13: I_{GT} - Quadrant III [MT2 (-) Gate (-)]

To measure the I_{GT} - Quadrant III parameter:

1. Set **Polarity** to (-).
2. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
3. Repeat Procedure 11. (Figure AN1006.15)

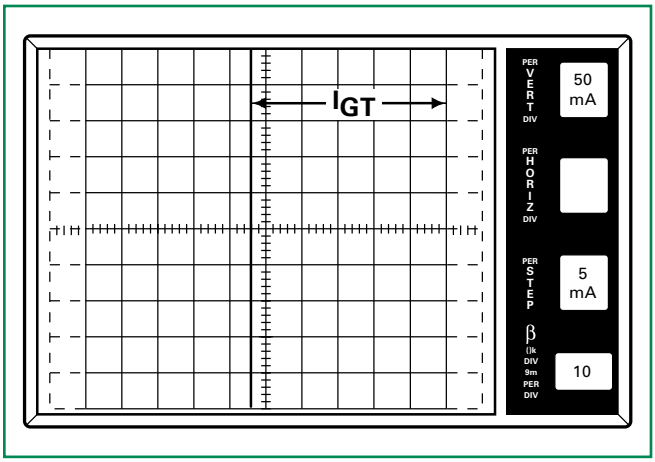


Figure AN1006.15 I_{GT} in Quadrant III = 27 mA

Procedure 14: I_{GT} - Quadrant IV [MT2 (-) Gate (+)]

To measure the I_{GT} - Quadrant IV parameter:

1. Set **Polarity** to (-).
2. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).
3. Set observed dot to top left corner of CRT grid by turning the **Horizontal** position knob. When Quadrant IV testing is complete, return dot to original position.
4. Repeat Procedure 11.

Procedure 15: V_{GT}

To measure the V_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps** to *1*. (Set steps to *0* (zero) on 370.)
3. Set **Offset** by depressing *Aid*. (On 577, also set *0* (zero) button to *Offset*. Button is extended.)
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and *Oppose* at same time on 370.)
5. Set **Terminal Selector** to *Step Generator-Emitter Grounded.*
6. Set **Mode** to *Norm.*
7. Set **Max Peak Volts** to *15 V.* (*16 V* on 370)
8. Set **Power Dissipation** to *10 W.*
9. Set **Step Family** by depressing *Single.*
10. Set **Horizontal** knob to *2 V/DIV.*
11. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
12. Set **Current Limit** to 500 mA (not available on 577).
13. Increase **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
14. After 12 V setting is complete, change **Horizontal** knob to *Step Generator.*

Procedure 16: V_{GT} - Quadrant I [MT2 (+) Gate (+)]

To measure the V_{GT} - Quadrant I parameter:

1. Set **Step/Offset Amplitude** to 20% of rated V_{GT}.
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Gradually increase **Offset Multiplier** until device reaches conduction point. (Figure AN1006.16) Measure V_{GT} by following horizontal axis to the point where the vertical line passes through the axis. This measured value will be V_{GT}. (On 370, V_{GT} will be numerically displayed on screen under offset value.)

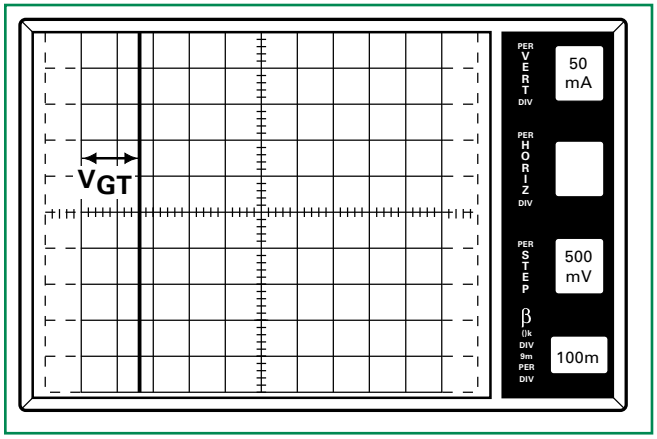


Figure AN1006.16 V_{GT} in Quadrant I = 780 mV

Procedure 17: V_{GT} - Quadrant II [MT2 (+) Gate (-)]

To measure the V_{GT} - Quadrant II parameter:

1. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).
2. Set **Polarity** to (+).
3. Set observed dot to bottom right corner of CRT grid by turning the **Horizontal** position knob. When Quadrant II testing is complete, return dot to original position.
4. Repeat Procedure 16.

Procedure 18: V_{GT} - Quadrant III [MT2 (-) Gate (-)]

To measure the V_{GT} - Quadrant III parameter:

1. Set **Polarity** to (-).
2. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
3. Repeat Procedure 16. (Figure AN1006.17)

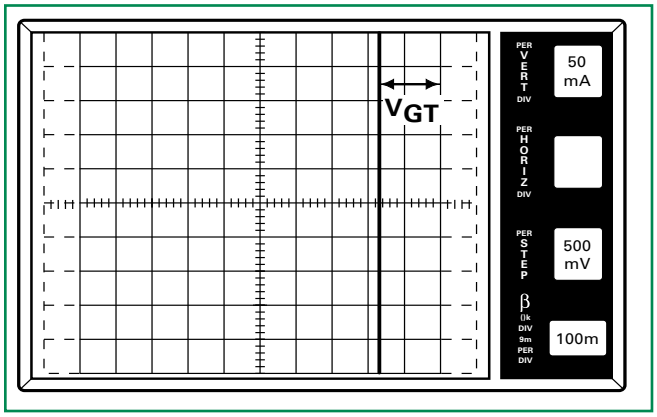


Figure AN1006.17 V_{GT} in Quadrant III = 820 mV

Procedure 19: V_{GT} - Quadrant IV [MT2 (-) Gate (+)]

To measure the V_{GT} - Quadrant IV parameter:

1. Set **Polarity** to (-).
2. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).

3. Set observed dot to top left corner of CRT grid by turning the **Horizontal** position knob. When testing is complete in Quadrant IV, return dot to original position.
4. Repeat Procedure 16.

Quadracs

Quadracs are simply Triacs with an internally-mounted DIAC. As with Triacs, Quadracs are bidirectional AC switches which are gate controlled for either polarity of main terminal voltage.

To connect the Quadrac*:*

1. Connect *Trigger* to *Base Terminal* (B).
2. Connect *MT1* to *Emitter Terminal* (E).
3. Connect *MT2* to *Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, (-)I_{DRM}

Note: The (+) and (-) symbols are used to designate the polarity of MT2 with reference to MT1.

To measure the (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, and (-)I_{DRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to or greater than the device's V_{DRM} rating).
2. Set **Horizontal** knob to sufficient scale to allow *viewing of trace at the required voltage level. (The* 100 V/DIV scale should be used for testing devices having a V_{DRM} rating of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 300 V to 500 V, and so on).
3. Set **Mode** to Leakage.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
7. Set **Vertical** knob to ten times the maximum leakage current (I_{DRM}) specified for the device.

   Note: The CRT readout should show 1% of the maximum leakage current. The vertical scale is divided by 1,000 when the leakage mode is used.

Procedure 2: (+)V_{DRM} and (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on the CRT. (Read across horizontally from the dot to the vertical current scale.) This measured value is the leakage current. (Figure AN1006.18)

WARNING: Do NOT exceed V_{DRM}/V_{RRM} rating of SCRs, Triacs, or Quadracs. These devices can be damaged.

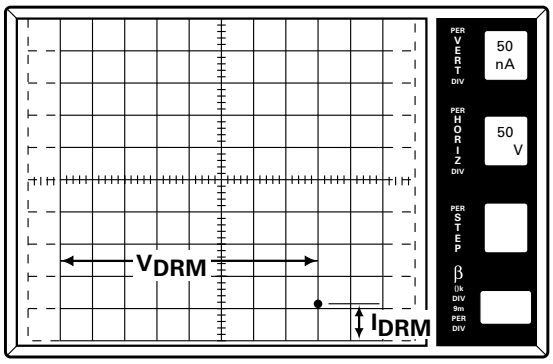


Figure AN1006.18 (+)I_{DRM} = 51 nA at (+)V_{DRM} = 400 V

Procedure 3: (-)V_{DRM} and (-)I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (-).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of screen).

Procedure 4: V_{BO}, I_{BO}, V_{BO}

(Quadrac Trigger DIAC or Discrete DIAC)

To connect the Quadrac:

1. Connect *MT1 to Emitter Terminal* (E).
2. Connect *MT2 to Collector Terminal* (C).
3. Connect *Trigger Terminal* to *MT2 Terminal* through a 10 Ω resistor.

To measure the V_{BO}, I_{BO}, and ΔV_{BO} parameter:

1. Set **Variable Collector Supply Voltage Range** to *75 Max Peak Volts.*(*80 V* on 370)
2. Set **Horizontal** knob to *10 V/DIV.*
3. Set **Vertical** knob to *50 µA/DIV.*
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*

Procedure 5: V_{BO} (Positive and Negative)

To measure the $V_{BO\ (Positive\ and\ Negative)}$ parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Set **Variable Collector Supply Voltage** to *55 V* (*65 V* on 370) and apply voltage to the device under test (D.U.T.) using the **Left Hand Selector Switch**. The peak voltage at which current begins to flow is the V_{BO} value. (Figure AN1006.19)

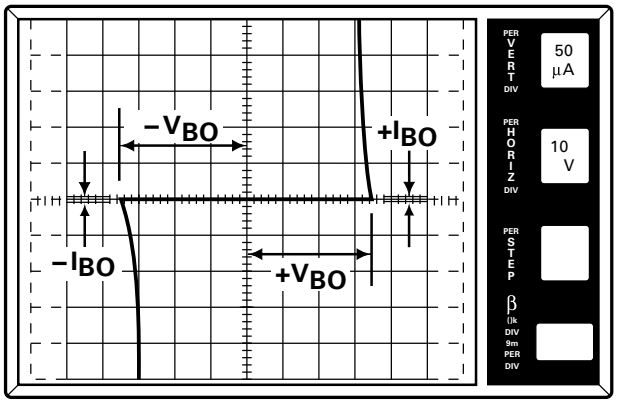


Figure AN1006.19 (+)V_{BO} = 35 V; (-)V_{BO} = 36 V; (±)I_{BO} < 10 A

Procedure 6: I_{BO} (Positive and Negative)

To measure the $I_{BO\ (Positive\ and\ Negative)}$ parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover point. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on curve tracer.

Procedure 7: $\Delta V_{BO\ (Voltage\ Breakover\ Symmetry)}$

To measure the $\Delta V_{BO\ (Voltage\ Breakover\ Symmetry)}$ parameter:

1. Measure positive and negative V_{BO} values per Procedure 5.
2. Subtract the absolute value of V_{BO} (-) from V_{BO} (+).

   The absolute value of the result is:

   $\Delta V_{BO} = [\ |+V_{BO}| - |-V_{BO}|\ ]$

Procedure 8: $V_{TM\ (Forward\ and\ Reverse)}$

To test V_{TM}, the Quadrac must be connected the same as when testing V_{BO}, I_{BO}, and ΔV_{BO}.

To connect the Quadrac:

1. Connect *MT1* to *Emitter Terminal* (E).
2. Connect *MT2* to *Collector Terminal* (C).
3. Connect *Trigger Terminal* to *MT2 Terminal* through a 10 Ω resistor.

Note the following:

Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 8 A or less should be tested on standard curve tracer. If testing devices above 8 A, a Tektronix model 176 high-current module is required.

A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
2. Set **Max Peak Volts** to *75 V.* (*80 V* on 370)
3. Set **Mode** to *Norm.*
4. Set **Horizontal** knob to *0.5 V/DIV.*
5. Set **Power Dissipation** to *220 watts* (*100 watts* on a 577).
6. Set **Vertical** knob to a sufficient setting to allow the viewing of 1.4 times the $I_{T(RMS)}$ rating of the device $I_{T(peak)}$ on the CRT.

Procedure 9: $V_{TM(Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable** Collector **Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times the $I_{T(RMS)}$ rating of the Triac under test.

   Note: Model 370 current is limited to 10 A.

   WARNING: Limit test time to 15 seconds maximum.
4. To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. This horizontal distance is the V_{TM} value. (Figure AN1006.20)

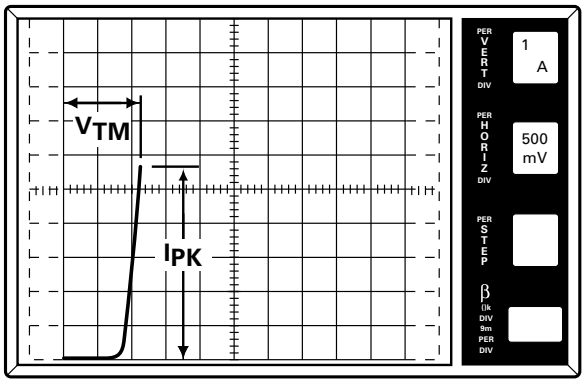


Figure AN1006.20 $V_{TM\ (Forward)}$ = 1.1 V at I_{PK} = 5.6 A

Procedure 10: $V_{TM(Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

1. Set **Polarity** to (-).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable** Collector **Supply Voltage** until current reaches rated $I_{T(peak)}$.
4. Measure $V_{TM(Reverse)}$ the same as in Procedure 8. (Read measurements from upper right corner of screen).

Procedure 11: $I_{H(Forward\ and\ Reverse)}$

For these steps, it is again necessary to connect the *Trigger* to *MT2* through a 10 Ω resistor. The other connections remain the same.

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Power Dissipation** to *50 W*.
2. Set **Max Peak Volts** to *75 V*. (*80 V* on 370)
3. Set **Mode** to *DC*.
4. Set **Horizontal** knob to *5 V/DIV*.
5. Set **Vertical** knob to approximately 10% of the maximum I_H specified.

   Note: Due to large variations of holding current values, the scale may have to be adjusted to observe holding current.
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.

Procedure 12: $I_{H(Forward)}$

To measure the $I_{H\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable** Collector **Supply Voltage** to maximum position (*100*).

   Note: Depending on the vertical scale being used, the dot may disappear completely from the screen.
4. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line changes to a dot, represents the I_H value. (Figure AN1006.21)

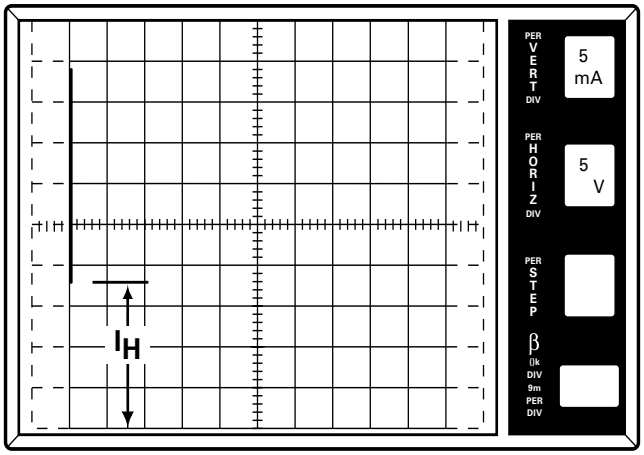


Figure AN1006.21 $I_{H\ (Forward)}$ = 18 mA

Procedure 13: $I_{H(Reverse)}$

To measure the $I_{H\ (Reverse)}$ parameter:

1. Set **Polarity** to (-).
2. Continue testing per Procedure 12 for measuring $I_{H\ (Reverse)}$.

SIDACs

The SIDAC is a bidirectional voltage-triggered switch. Upon application of a voltage exceeding the SIDAC breakover voltage point, the SIDAC switches on through a negative resistance region (similar to a DIAC) to a low on-state voltage. Conduction continues until current is interrupted or drops below minimum required holding current.

To connect the SIDAC:

1. Connect *MT1* to *the Emitter Terminal* (E).
2. Connect *MT2* to *the Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: (+) V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, (-)I_{DRM}

Note: The (+) and (-) symbols are used to designate the polarity of MT2 with reference to MT1.

To measure the (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, and (-)I_{DRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts*.
2. Set **Horizontal** knob to *50 V/DIV*.
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *2.2 W*. (*2 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
7. Set **Vertical** knob to *50 µA/DIV*. (Due to leakage mode, the CRT readout will show 50 nA.)

Procedure 2: (+)V_{DRM} and (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.22)

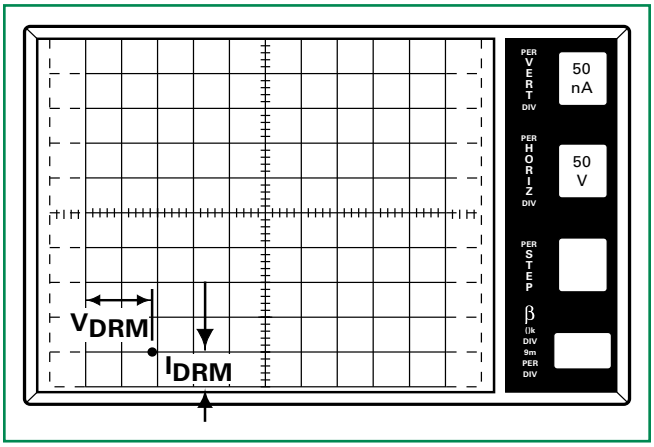


Figure AN1006.22 I_{DRM} = 50 nA at V_{DRM} = 90 V

Procedure 3: (-) V_{DRM} and (-) I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (-).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of the screen).

Procedure 4: V_{BO} and I_{BO}

To measure the V_{BO} and I_{BO} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts.* (*2000 V* on 370)
2. Set **Horizontal** knob to a sufficient scale to allow viewing of trace at the required voltage level (*50 V/DIV* for 95 V to 215 V V_{BO} range devices and *100 V/DIV* for devices having $V_{BO} \geq$ 15 V).
3. Set **Vertical** knob to *50 A/DIV.*
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *10 W.*
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
8. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.

Procedure 5: V_{BO}

To measure the V_{BO} parameter, increase **Variable Collector Supply Voltage** until breakover occurs. (Figure AN1006.23) The voltage at which current begins to flow and voltage on CRT does not increase is the V_{BO} value.

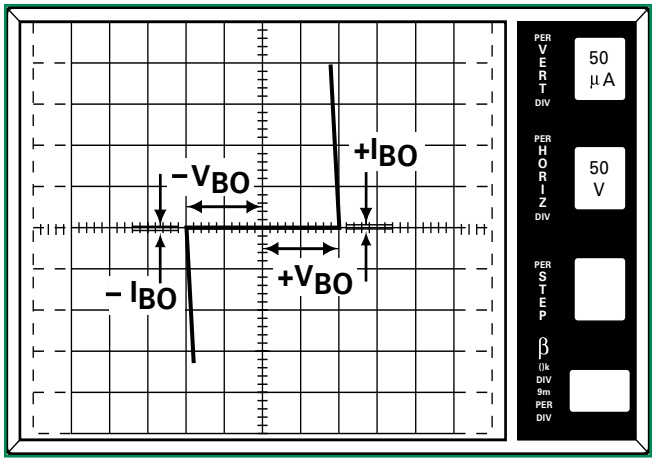


Figure AN1006.23 (+)V_{BO} = 100 V; (-)V_{BO} = 100 V; (±)I_{BO} < 10 µA

Procedure 6: I_{BO}

To measure the I_{BO} parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover mode. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on the curve tracer.

Procedure 7: $I_{H(Forward\ and\ Reverse)}$

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts* (*400 V* on 577; *2000 V* on 370).
2. Set **Horizontal** knob to a sufficient scale to allow viewing of trace at the required voltage level (50 V/DIV for devices with V_{BO} range from 95 V to 215 V and 100 V/DIV for devices having $V_{BO} \geq$ 215 V).
3. Set **Vertical** knob to 20% of maximum holding current specified.
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *220 W* (*100 W* on 577).
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
8. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.

WARNING: Limit test time to 15 seconds maximum.

9. Increase **Variable Collector Supply Voltage** until device breaks over and turns on. (Figure AN1006.24)

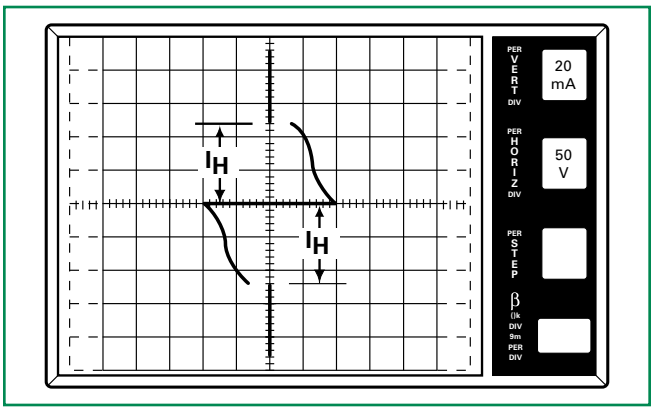


Figure AN1006.24 I_H = 48 mA in both forward and reverse directions

I_H is the vertical distance between the center horizontal axis and the beginning of the line located on center vertical axis.

Procedure 8: $V_{TM(Forward\ and\ Reverse)}$

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Variable Collector Supply Voltage Range** to *350 Max Peak Volts.* (*400 V* on 370)
2. Set **Horizontal** knob to *0.5 V/DIV.*
3. Set **Vertical** knob to *0.5 A/DIV.*
4. Set **Polarity** to (+).
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *220 W* (*100 W* on 577).
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*

Before continuing with testing, note the following:

- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin Connections.

To continue testing, perform the following procedures.

Procedure 9: $V_{TM(Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times the $I_{T(RMS)}$ rating of the SIDAC.

   Note: Model 370 current is limited. Set to 400 mA. Check for 1.1 V MAX.

   WARNING: Limit test time to 15 seconds.
3. To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. This horizontal distance is the V_{TM} value. (Figure AN1006.25)

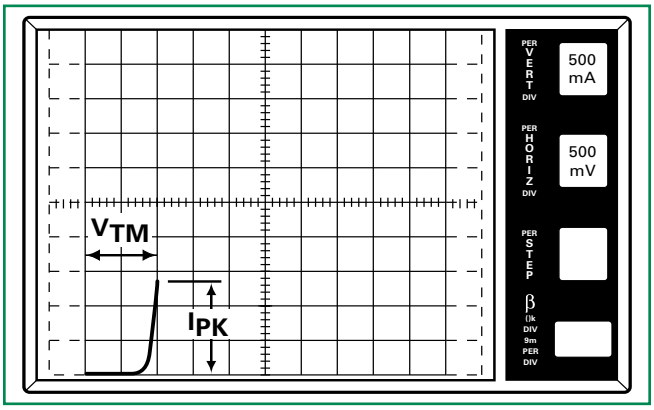


Figure AN1006.25 $V_{TM\ (Forward)}$ = 950 mV at I_{PK} = 1.4 A

Procedure 10: $V_{TM(Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

Set **Polarity** to (-).

Repeat Procedure 8 to measure $V_{TM(Reverse)}$.

DIACs

DIACs are voltage breakdown switches used to trigger-on Triacs and non-sensitive SCRs in phase control circuits.

Note: DIACs are bi-directional devices and can be connected in either direction.

To connect the DIAC:

Connect one side of the DIAC to the Collector Terminal (C).

Connect other side of the DIAC to the Emitter Terminal (E).

To begin testing, perform the following procedures.

Procedure 1: Curve Tracer Setup

To set the curve tracer and begin testing:

1 Set **Variable Collector Supply Voltage Range** to *75 Max Peak Volts.* (*80 V* on 370)

2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level (*10 V* to *20 V/DIV* depending on device being tested).
3. Set **Vertical** knob to *50 µA/DIV.*
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*

Procedure 2: V_{BO}

To measure the V_{BO} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Set **Variable Collector Supply Voltage** to *55 V* (*65 V* for 370) and apply voltage to device under test (D.U.T.), using **Left-Right-Selector Switch**. The peak voltage at which current begins to flow is the V_{BO} value. (Figure AN1006.26)

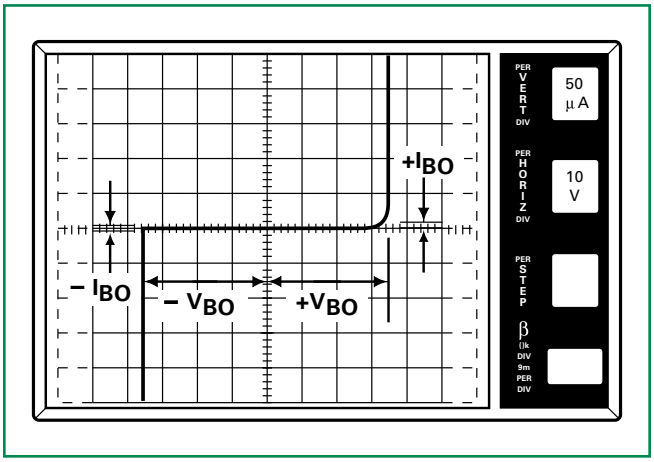


Figure AN1006.26 (+)V_{BO} = 35 V; (-)V_{BO} = 36 V; (±)I_{BO} < 15 µA; (-) I_{BO} < 10 µA and Cannot Be Read Easily

Procedure 3: I_{BO}

To measure the I_{BO} parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover mode. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on the curve tracer.

Procedure 4: $\Delta V_{BO(Voltage\ Breakover\ Symmetry)}$

To measure the $\Delta V_{BO\ (Voltage\ Breakover\ Symmetry)}$ parameter:

1. Measure positive and negative values of V_{BO} as shown in Figure AN1006.26.
2. Subtract the absolute value of V_{BO}(-) from V_{BO}(+).

   The absolute value of the result is:

   $\Delta V_{BO} = [\ |\ +V_{BO}\ |\ -\ |\ -V_{BO}\ |\ ]$

Model 370 Curve Tracer Procedure Notes

Because the curve tracer procedures in this application note are written for the Tektronix model 576 curve tracer, certain settings must be adjusted when using model 370. Variable Collector Supply Voltage Range and Power Dissipation controls have different scales than model 576. The following table shows the guidelines for setting Power Dissipation when using model 370. (Figure AN1006.27)

Model 576	Model 370
If power dissipation is 0.1 W,	set at 0.08 W.
If power dissipation is 0.5 W,	set at 0.4 W.
If power dissipation is 2.2 W,	set at 2 W.
If power dissipation is 10 W,	set at 10 W.
If power dissipation is 50 W,	set at 50 W.
If power dissipation is 220 W,	set at 220 W.

Although the maximum power setting on the model 370 curve tracer is 200 W, the maximum collector voltage available is only 400 V at 220 W. The following table shows the guidelines for adapting Collector Supply Voltage Range settings for model 370 curve tracer procedures:

Model 576	Model 370
If voltage range is 15 V	set at 16 V.
If voltage range is 75 V	set at 80 V.
If voltage range is 350 V	set at 400 V.
If voltage range is 1500 V	set at 2000 V

The following table shows the guidelines for adapting terminal selector knob settings for model 370 curve tracer procedures:

Model 576	Model 370
If Step generator (base) is emitter grounded	then Base Step generator is emitter common.
If Emitter grounded is open base	then Base open is emitter common.

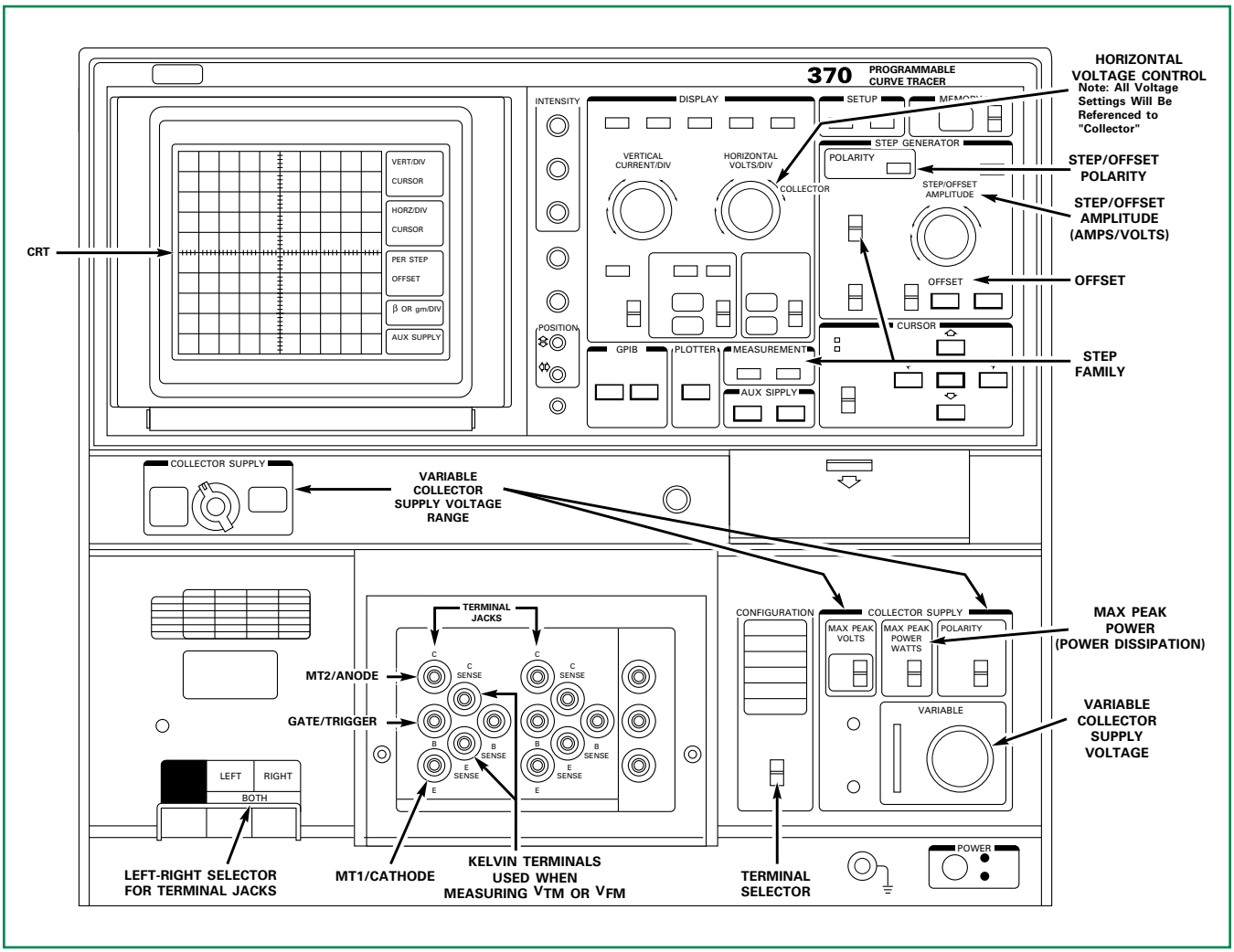


Figure AN1006.27 Tektronix Model 370 Curve Tracer

Model 577 Curve Tracer Procedure Notes

Because the curve tracer procedures in this application note are written for the Tektronix model 576 curve tracer, certain settings must be adjusted when using model 577. Model 576 curve tracer has separate controls for polarity (AC,+,-) and mode (Norm, DC, Leakage), whereas Model 577 has only a polarity control. The following table shows the guidelines for setting Collector Supply Polarity when using model 577. (Figure AN1006.28)

Model 576	Model 577
If using Leakage mode along with polarity setting of +(NPN) and -(PNP),[vertical scale divided by 1,000],	set **Collector Supply Polarity** to either *+DC* or *-DC*, depending on polarity setting specified in the procedure. The vertical scale is read directly from the scale on the control knob.
If using DC mode along with either +(NPN) or -(PNP) polarity,	set **Collector Supply Polarity** to either *+DC* or *-DC* depending on polarity specified.
If using Norm mode along with either +(NPN) or -(PNP) polarity,	set **Collector Supply Polarity** to either *+(NPN)* or *-(PNP)* per specified procedure.
If using Norm mode with *AC* polarity,	set **Collector Supply Polarity** to *AC*.

One difference between models 576 and 577 is the Step/Offset Polarity setting. The polarity is inverted when the button is depressed on the Model 576 curve tracer. The Model 577 is opposite — the Step/Offset Polarity is "inverted" when the button is extended and "Normal" when the button is depressed. The Step/Offset Polarity is used only when measuring I_{GT} and V_{GT} of Triacs and Quadracs in Quadrants I through IV.

Also, the Variable Collector Supply Voltage Range and Power Dissipation controls have different scales than model 576. The following table shows the guidelines for setting Power Dissipation when using model 577.

Model 576	Model 577
If power dissipation is 0.1 W,	set at 0.15 W.
If power dissipation is 0.5 W,	set at 0.6 W.
If power dissipation is 2.2 W,	set at 2.3 W.
If power dissipation is 10 W,	set at 9 W.
If power dissipation is 50 W,	set at 30 W.
If power dissipation is 220 W,	set at 100 W.

Although the maximum power setting on model 576 curve tracer is 220 W (compared to 100 W for model 577), the maximum collector current available is approximately the same. This is due to the minimum voltage range on model 577 curve tracer being 6.5 V compared to 15 V for model 576. The following table shows the guidelines for adapting Collector Voltage Supply Range settings for model 577 curve tracer procedures:

Model 576	Model 577
If voltage range is 15 V	set at either 6.5 V or 25 V, depending on parameter being tested. Set at 6.5 V when measuring V_{TM} (to allow maximum collector current) and set at 25 V when measuring I_{GT} and V_{GT}.
If voltage range is 75 V	set at 100 V.
If voltage range is 1500 V,	set at 1600 V.

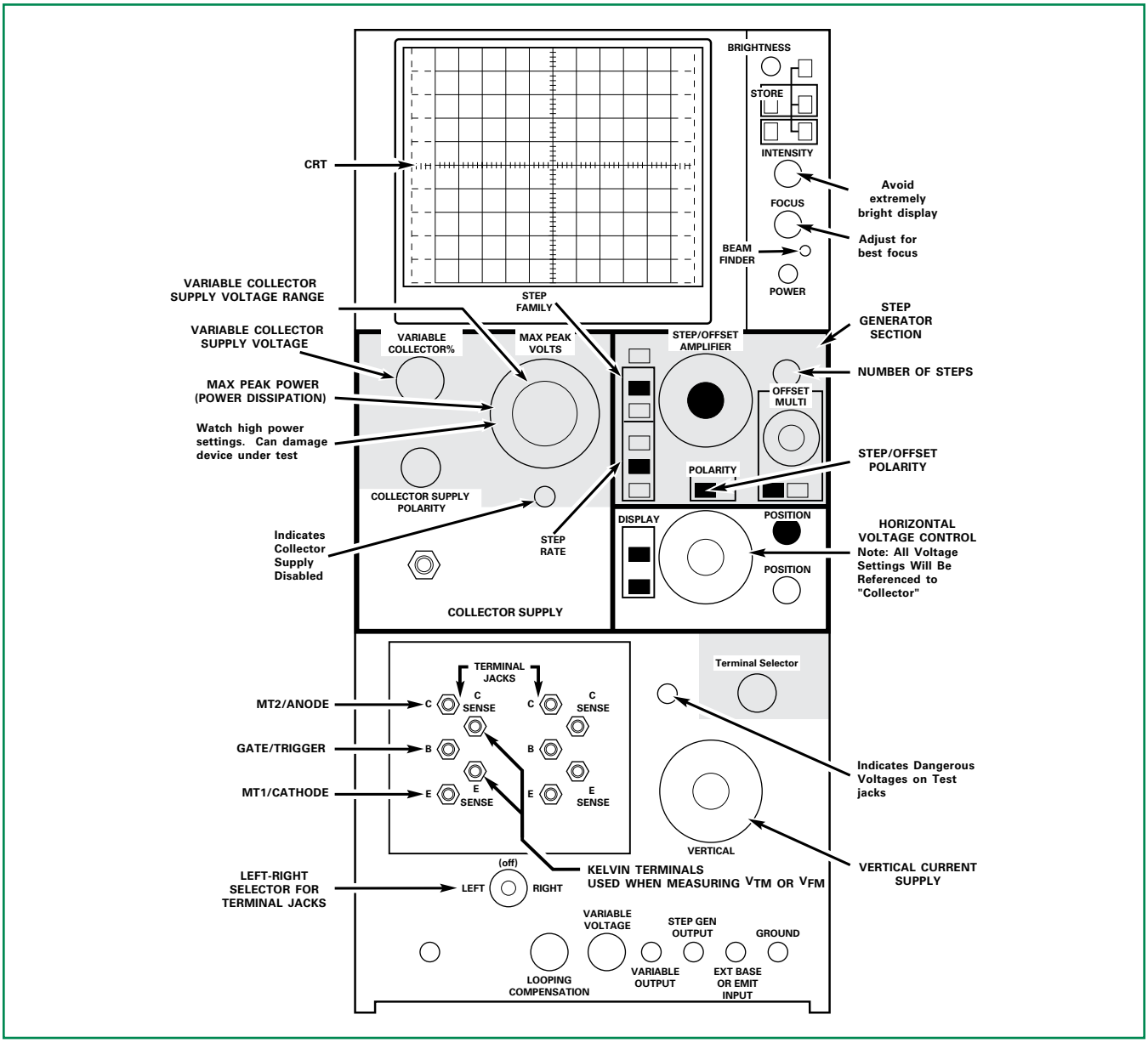


Figure AN1006.28 Tektronix Model 577 Curve Tracer

Fundamental Characteristics of Thyristors

Introduction

The Thyristor family of semiconductors consists of several very useful devices. The most widely used of this family are silicon controlled rectifiers (SCRs), Triacs, SIDACs, and DIACs. In many applications these devices perform key functions and are real assets in meeting environmental, speed, and reliability specifications which their electro-mechanical counterparts cannot fulfill.

This application note presents the basic fundamentals of SCR, Triac, SIDAC, and DIAC Thyristors so the user understands how they differ in characteristics and parameters from their electro-mechanical counterparts. Also, Thyristor terminology is defined.

SCR

Basic Operation

Figure AN1001.1 shows the simple block construction of an SCR.

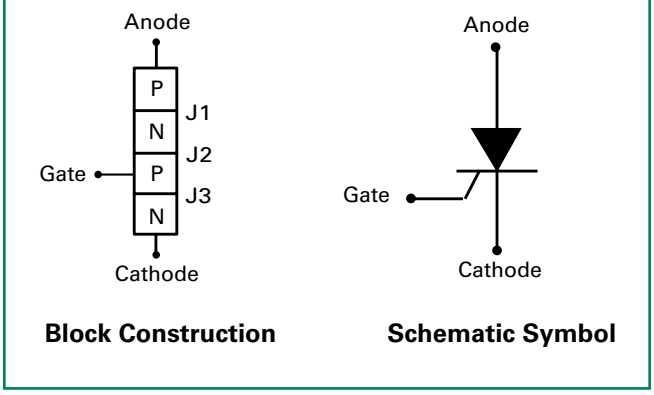


Figure AN1001.1 SCR Block Construction

The operation of a PNPN device can best be visualized as a specially coupled pair of transistors as shown in Figure AN1001.2.

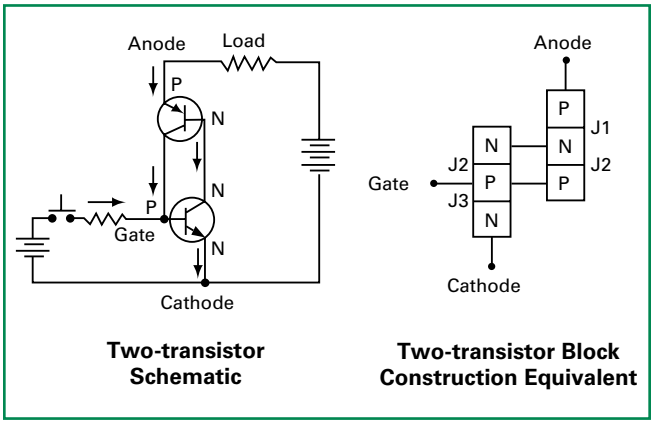


Figure AN1001.2 Coupled Pair of Transistors as a SCR

The connections between the two transistors trigger the occurrence of regenerative action when a proper gate signal is applied to the base of the NPN transistor. Normal leakage current is so low that the combined h_{FE} of the specially coupled two-transistor feedback amplifier is less than unity, thus keeping the circuit in an off-state condition. A momentary positive pulse applied to the gate biases the NPN transistor into conduction which, in turn, biases the PNP transistor into conduction. The effective h_{FE} momentarily becomes greater than unity so that the specially coupled transistors saturate. Once saturated, current through the transistors is enough to keep the combined h_{FE} greater than unity. The circuit remains "on" until it is "turned off" by reducing the anode-to-cathode current (I_T) so that the combined h_{FE} is less than unity and regeneration ceases. This threshold anode current is the holding current of the SCR.

Geometric Construction

Figure AN1001.3 shows cross-sectional views of an SCR chip and illustrations of current flow and junction biasing in both the blocking and triggering modes.

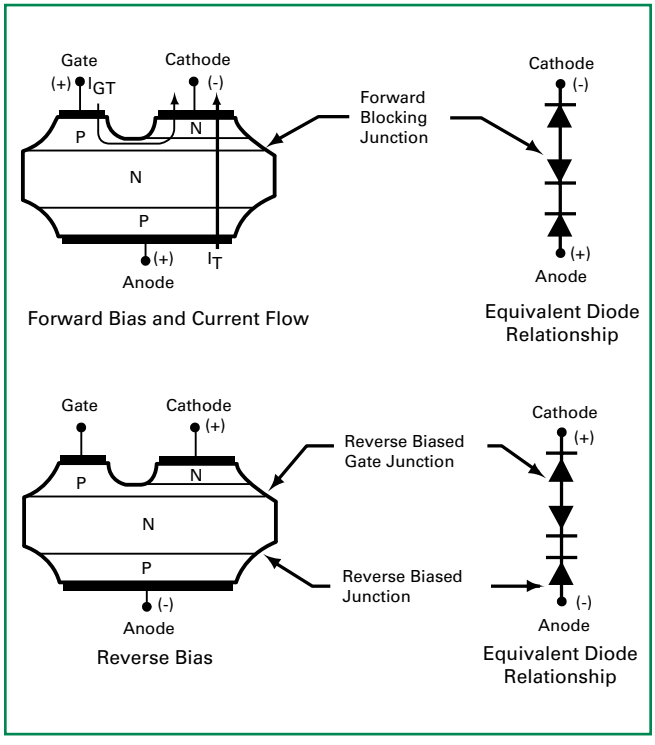


Figure AN1001.3 Cross-sectional View of SCR Chip

Triac

Basic Operation

Figure AN1001.4 shows the simple block construction of a Triac. Its primary function is to control power bilaterally in an AC circuit.

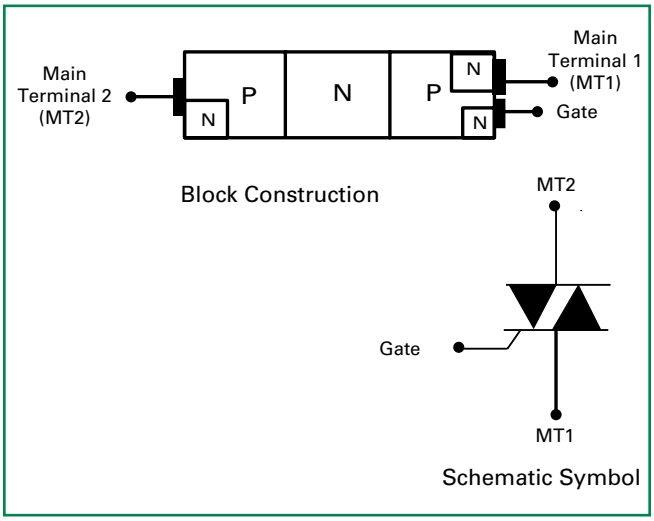


Figure AN1001.4 Triac Block Construction

Operation of a Triac can be related to two SCRs connected in parallel in opposite directions as shown in Figure AN1001.5.

Although the gates are shown separately for each SCR, a Triac has a single gate and can be triggered by either polarity.

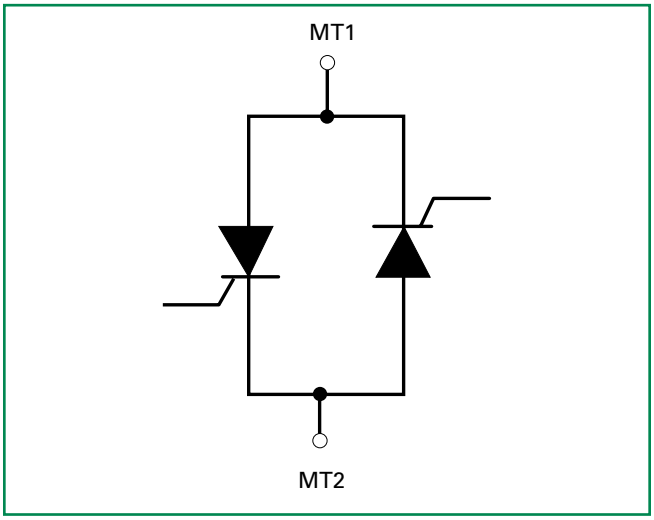


Figure AN1001.5 SCRs Connected as a Triac

Since a Triac operates in both directions, it behaves essentially the same in either direction as an SCR would behave in the forward direction (blocking or operating).

Geometric Construction

Figure AN1001.6 show simplified cross-sectional views of a Triac chip in various gating quadrants and blocking modes.

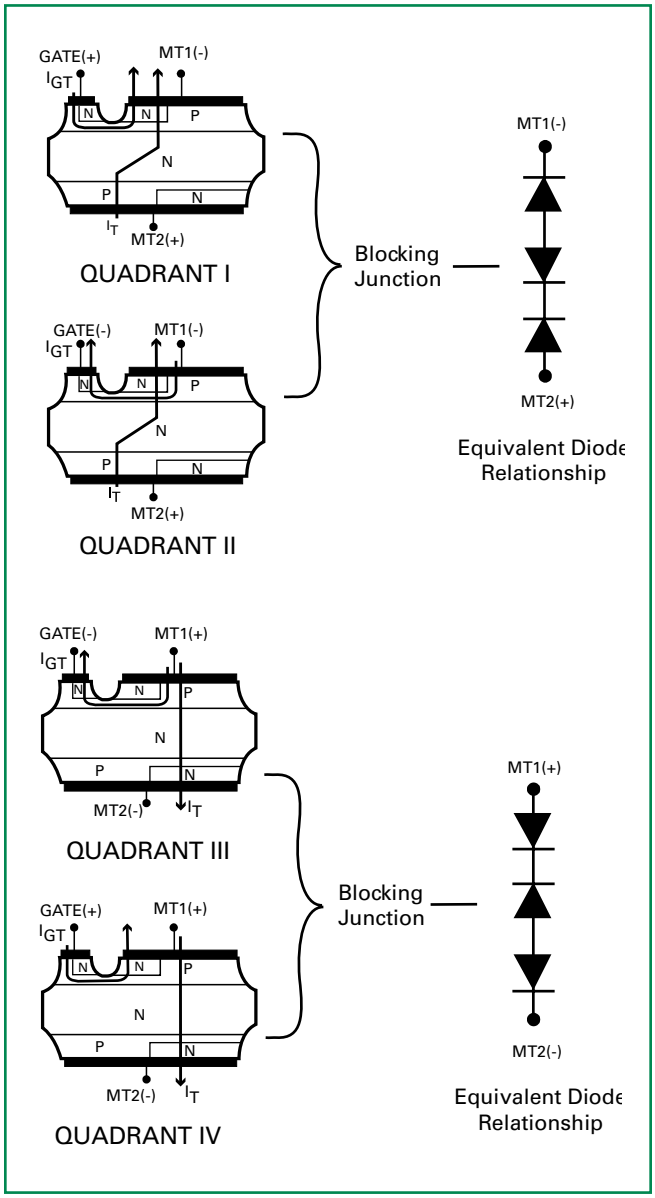


Figure AN1001.6 Simplified Cross-sectional of Triac Chip

SIDAC

Basic Operation

The SIDAC is a multi-layer silicon semiconductor switch. Figure AN1001.7 illustrates its equivalent block construction using two Shockley diodes connected inverse parallel. Figure AN1001.7 also shows the schematic symbol for the SIDAC.

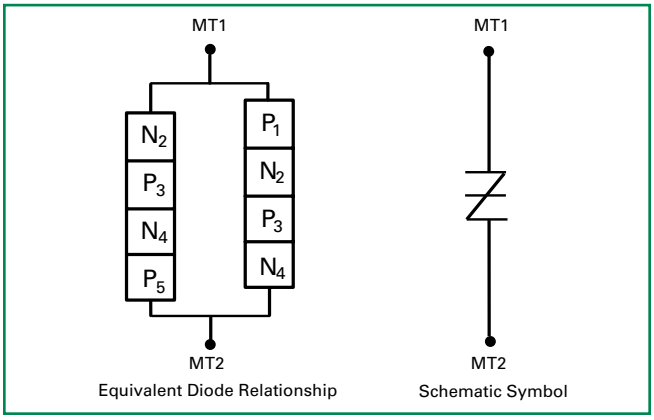


Figure AN1001.7 SIDAC Block Construction

The SIDAC operates as a bidirectional switch activated by voltage. In the off state, the SIDAC exhibits leakage currents (I_{DRM}) less than 5 µA. As applied voltage exceeds the SIDAC V_{BO}, the device begins to enter a negative resistance switching mode with characteristics similar to an avalanche diode. When supplied with enough current (I_S), the SIDAC switches to an on state, allowing high current to flow. When it switches to on state, the voltage across the device drops to less than 5 V, depending on magnitude of the current flow. When the SIDAC switches on and drops into regeneration, it remains on as long as holding current is less than maximum value (150 mA, typical value of 30 mA to 65 mA). The switching current (I_S) is very near the holding current (I_H) value. When the SIDAC switches, currents of 10 A to 100 A are easily developed by discharging small capacitor into primary or small, very high-voltage transformers for 10 µs to 20 µs.

The main application for SIDACs is ignition circuits or inexpensive high voltage power supplies.

Geometric Construction

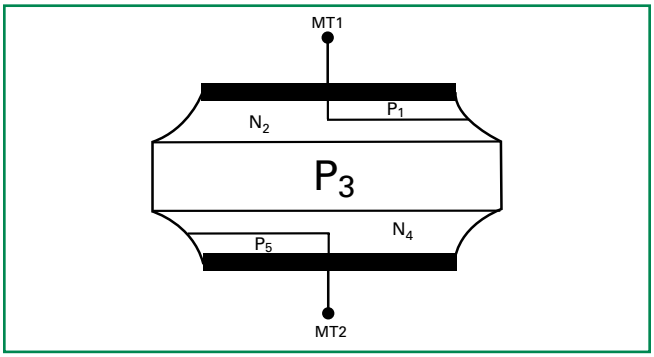


Figure AN1001.8 Cross-sectional View of a Bidirectional SIDAC Chip with Multi-layer Construction

DIAC

Basic Operation

The construction of a DIAC is similar to an open base NPN transistor. Figure AN1001.9 shows a simple block construction of a DIAC and its schematic symbol.

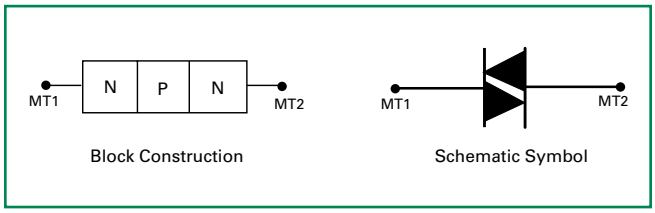


Figure AN1001.9 DIAC Block Construction

The bidirectional transistor-like structure exhibits a high-impedance blocking state up to a voltage breakover point (V_{BO}) above which the device enters a negative-resistance region. These basic DIAC characteristics produce a bidirectional pulsing oscillator in a resistor-capacitor AC circuit. Since the DIAC is a bidirectional device, it makes a good economical trigger for firing Triacs in phase control circuits such as light dimmers and motor speed controls. Figure AN1001.10 shows a simplified AC circuit using a DIAC and a Triac in a phase control application.

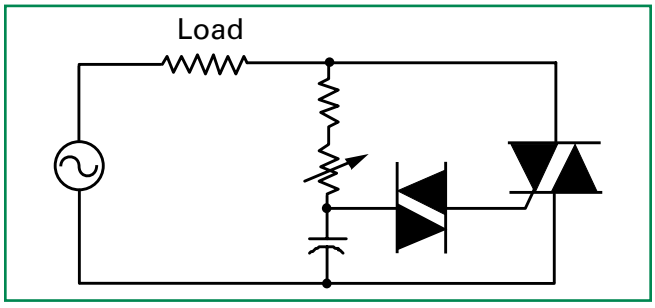


Figure AN1001.10 AC Phase Control Circuit

Geometric Construction

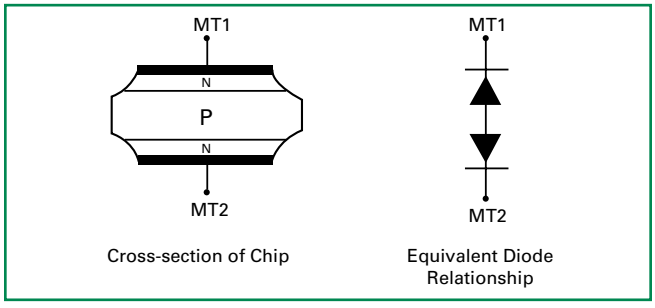


Figure AN1001.11 Cross-sectional View of DIAC Chip

Electrical Characteristic Curves of Thyristors

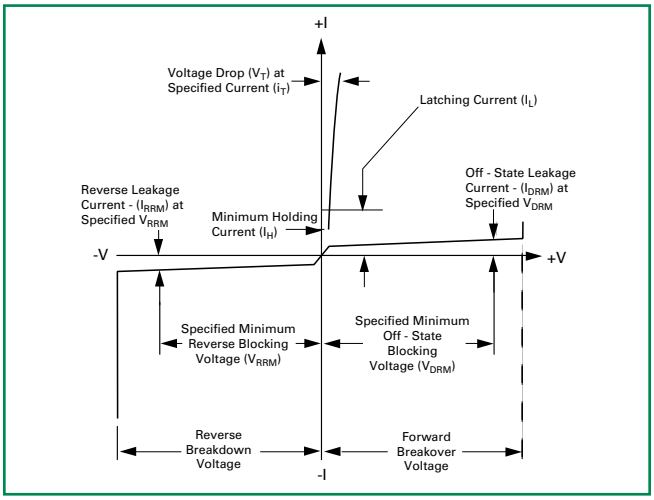


Figure AN1001.12 V-I Characteristics of SCR Device

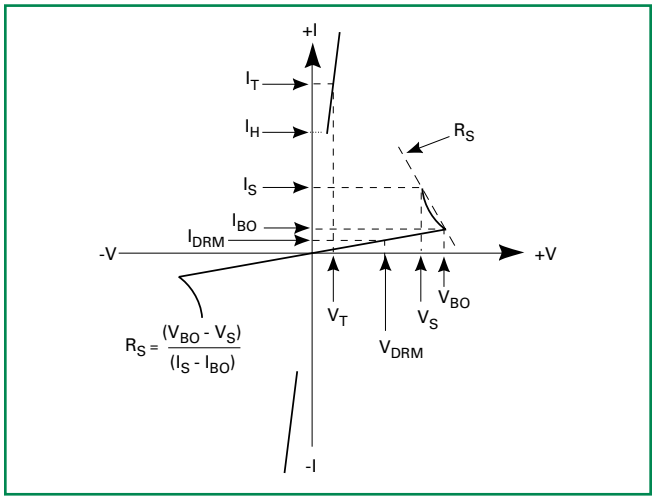


Figure AN1001.15 V-I Characteristics of a SIDAC Chip

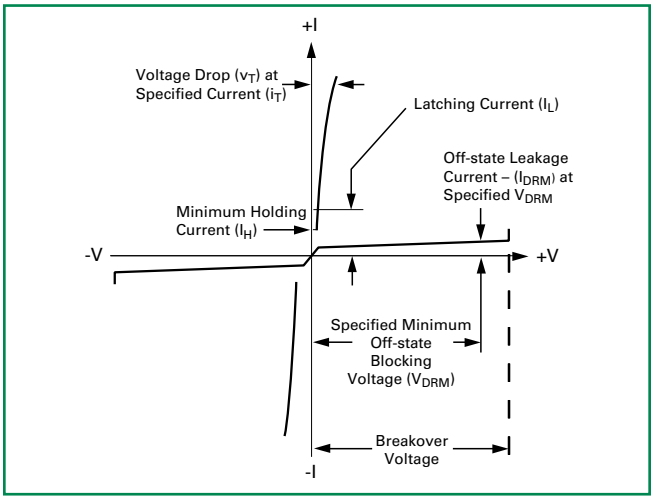


Figure AN1001.13 V-I Characteristics of Triac Device

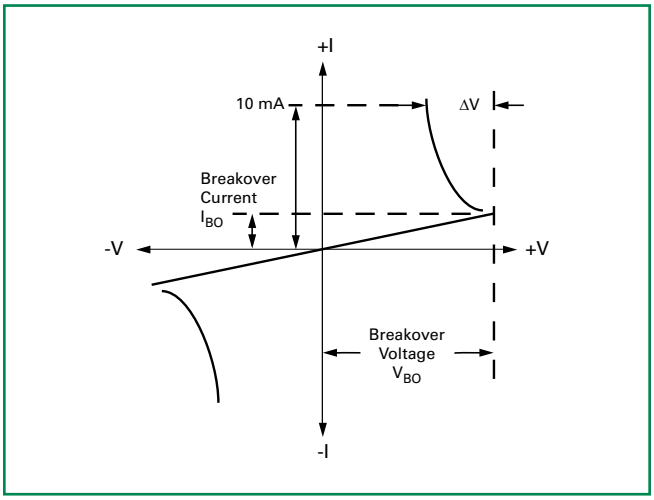


Figure AN1001.14 V-I Characteristics of Bilateral Trigger DIAC

Methods of Switching on Thyristors

Three general methods are available for switching Thyristors to on-state condition:

- Application of gate signal
- Static dv/dt turn-on
- Voltage breakover turn-on

Application Of Gate Signal

Gate signal must exceed I_{GT} and V_{GT} requirements of the Thyristor used. For an SCR (unilateral device), this signal must be positive with respect to the cathode polarity. A Triac (bilateral device) can be turned on with gate signal of either polarity; however, different polarities have different requirements of I_{GT} and V_{GT} which must be satisfied. Since DIACs and SIDACs do not have a gate, this method of turn-on is not applicable. In fact, the single major application of DIACs is to switch on Triacs.

Static dv/dt Turn-on

Static dv/dt turn-on comes from a fast-rising voltage applied across the anode and cathode terminals of an SCR or the main terminals of a Triac. Due to the nature of Thyristor construction, a small junction capacitor is formed across each PN junction. Figure AN1001.16 shows how typical internal capacitors are linked in gated Thyristors.

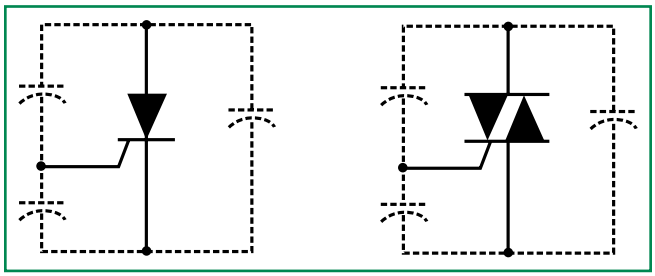


Figure AN1001.16 Internal Capacitors Linked in Gated Thyristors

When voltage is impressed suddenly across a PN junction, a charging current flows, equal to:

$$i = C\left(\frac{dv}{dt}\right)$$

When $C\left(\frac{dv}{dt}\right)$ becomes greater or equal to Thyristor I_{GT},

the Thyristor switches on. Normally, this type of turn-on does not damage the device, providing the surge current is limited.

Generally, Thyristor application circuits are designed with static dv/dt snubber networks if fast-rising voltages are anticipated.

Voltage Breakover Turn-on

This method is used to switch on SIDACs and DIACs. However, exceeding voltage breakover of SCRs and Triacs is definitely not recommended as a turn-on method.

In the case of SCRs and Triacs, leakage current increases until it exceeds the gate current required to turn on these gated Thyristors in a small localized point. When turn-on occurs by this method, localized heating in a small area may melt the silicon or damage the device if di/dt of the increasing current is not sufficiently limited.

DIACs used in typical phase control circuits are basically protected against excessive current at breakover as long as the firing capacitor is not excessively large. When DIACs are used in a zener function, current limiting is necessary.

SIDACs are typically pulse-firing, high-voltage transformers and are current limited by the transformer primary. The SIDAC should be operated so peak current amplitude, current duration, and di/dt limits are not exceeded.

Triac Gating Modes Of Operation

Triacs can be gated in four basic gating modes as shown in Figure AN1001.17.

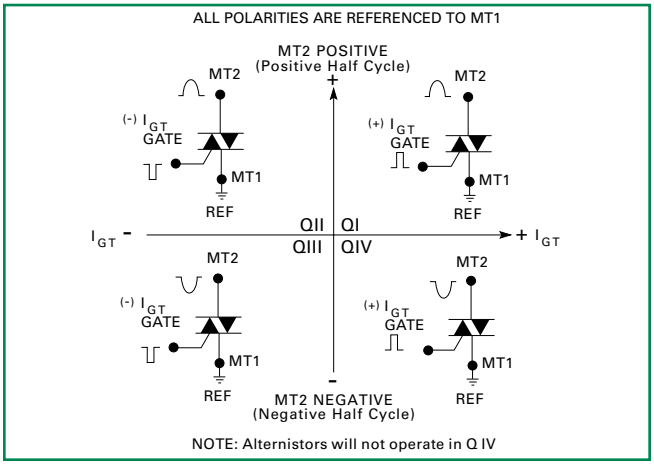


Figure AN1001.17 Gating Modes

The most common quadrants for Triac gating-on are Quadrants I and III, where the gate supply is synchronized with the main terminal supply (gate positive – MT2 positive, gate negative – MT2 negative). Gate sensitivity of Triacs is most optimum in Quadrants I and III due to the inherent Thyristor chip construction. If Quadrants I and III cannot be used, the next best operating modes are Quadrants II and III where the gate has a negative polarity supply with an AC main terminal supply. Typically, Quadrant II is approximately equal in gate sensitivity to Quadrant I; however, latching current sensitivity in Quadrant II is lowest. Therefore, it is difficult for Triacs to latch on in Quadrant II when the main terminal current supply is very low in value.

Special consideration should be given to gating circuit design when Quadrants I and IV are used in actual application, because Quadrant IV has the lowest gate sensitivity of all four operating quadrants.

General Terminology

The following definitions of the most widely-used Thyristor terms, symbols, and definitions conform to existing EIA-JEDEC standards:

Breakover Point – Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value

Principal Current – Generic term for the current through the collector junction (the current through main terminal 1 and main terminal 2 of a Triac or anode and cathode of an SCR)

Principal Voltage – Voltage between the main terminals:

(1) In the case of reverse blocking Thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential and negative when the anode potential is lower than the cathode potential.

(2) For bidirectional Thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.

Off State – Condition of the Thyristor corresponding to the high-resistance, low-current portion of the principal voltage-current characteristic between the origin and the breakover point(s) in the switching quadrant(s)

On State – Condition of the Thyristor corresponding to the low-resistance, low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

Specific Terminology

Average Gate Power Dissipation [$P_{G(AV)}$] – Value of gate power which may be dissipated between the gate and main terminal 1 (or cathode) averaged over a full cycle

Breakover Current (I_{BO}) – Principal current at the breakover point

Breakover Voltage (V_{BO}) – Principal voltage at the breakover point

Circuit-commutated Turn-off Time (t_q) – Time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit and the instant when the Thyristor is capable of supporting a specified principal voltage without turning on

Critical Rate-of-rise of Commutation Voltage of a Triac (Commutating dv/dt) – Minimum value of the rate-of-rise of principal voltage which will cause switching from the off state to the on state immediately following on-state current conduction in the opposite quadrant

Critical Rate-of-rise of Off-state Voltage or Static dv/dt (dv/dt) – Minimum value of the rate-of-rise of principal voltage which will cause switching from the off state to the on state

Critical Rate-of-rise of On-state Current (di/dt) – Maximum value of the rate-of-rise of on-state current that a Thyristor can withstand without harmful effect

Gate-controlled Turn-on Time (t_{gt}) – Time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped to a specified low value (or risen to a specified high value) during switching of a Thyristor from off state to the on state by a gate pulse.

Gate Trigger Current (I_{GT}) – Minimum gate current required to maintain the Thyristor in the on state

Gate Trigger Voltage (V_{GT}) – Gate voltage required to produce the gate trigger current

Holding Current (I_H) – Minimum principal current required to maintain the Thyristor in the on state

Latching Current (I_L) – Minimum principal current required to maintain the Thyristor in the on state immediately after the switching from off state to on state has occurred and the triggering signal has been removed

On-state Current (I_T) – Principal current when the Thyristor is in the on state

On-state Voltage (V_T) – Principal voltage when the Thyristor is in the on state

Peak Gate Power Dissipation (P_{GM}) – Maximum power which may be dissipated between the gate and main terminal 1 (or cathode) for a specified time duration

Repetitive Peak Off-state Current (I_{DRM}) – Maximum instantaneous value of the off-state current that results from the application of repetitive peak off-state voltage

Repetitive Peak Off-state Voltage (V_{DRM}) – Maximum instantaneous value of the off-state voltage which occurs across a Thyristor, including all repetitive transient voltages and excluding all non-repetitive transient voltages

Repetitive Peak Reverse Current of an SCR (I_{RRM}) – Maximum instantaneous value of the reverse current resulting from the application of repetitive peak reverse voltage

Repetitive Peak Reverse Voltage of an SCR (V_{RRM})– Maximum instantaneous value of the reverse voltage which occurs across the Thyristor, including all repetitive transient voltages and excluding all non-repetitive transient voltages

Surge (Non-repetitive) On-state Current (I_{TSM}) – On-state current of short-time duration and specified waveshape

Thermal Resistance, Junction to Ambient ($R_{\theta JA}$)– Temperature difference between the Thyristor junction and ambient divided by the power dissipation causing the temperature difference under conditions of thermal equilibrium

Note: Ambient is the point at which temperature does not change as the result of dissipation.

Thermal Resistance, Junction to Case ($R_{\theta JC}$) – Temperature difference between the Thyristor junction and the Thyristor case divided by the power dissipation causing the temperature difference under conditions of thermal equilibrium

Miscellaneous Design Tips and Facts

Introduction

This application note presents design tips and facts on the following topics:

- Relationship of I_{AV}, I_{RMS}, and I_{PK}
- dv/dt Definitions
- Examples of gate terminations
- Curves for Average Current at Various Conduction Angles
- Double-exponential Impulse Waveform
- Failure Modes of Thyristor
- Characteristics Formulas for Phase Control Circuits

Relationship of I_{AV}, I_{RMS}, and I_{PK}

Since a single rectifier or SCR passes current in one direction only, it conducts for only half of each cycle of an AC sinewave. The average current (I_{AV}) then becomes half of the value determined for full-cycle conduction, and the RMS current (I_{RMS}) is equal to the square root of half the mean-square value for full-cycle conduction or half the peak current (I_{PK}). In terms of half-cycle sinewave conduction (as in a single-phase half-wave circuit), the relationships of the rectifier currents can be shown as follows:

$I_{PK} = \pi \bullet I_{AV} = 3.14 \bullet I_{AV}$

$I_{AV} = (1/\pi)\ I_{PK} = 0.32 \bullet I_{PK}$

$I_{PK} = 2 \bullet I_{RMS}$

$I_{RMS} = 0.5 \bullet I_{PK}$

$I_{AV} = (2/\pi)\ I_{RMS} = 0.64 \bullet I_{RMS}$

$I_{RMS} = (\pi/2)\ I_{AV} = 1.57 \bullet I_{AV}$

When two identically rated SCRs are connected inverse parallel for full-wave operation, as shown in Figure AN1009.1, they can handle 1.41 times the RMS current rating of either single SCR. Therefore, the RMS value of two half sinewave current pulses in one cycle is √2 times the RMS value of one such pulse per cycle.

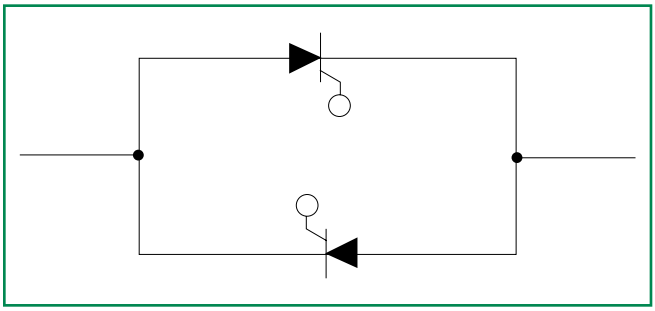


Figure AN1009.1 SCR Anti-parallel Circuit

dv/dt Definitions

The rate-of-rise of voltage (dv/dt) of an exponential waveform is 63% of peak voltage (excluding any overshoots) divided by the time at 63% minus 10% peak voltage. (Figure AN1009.2)

Exponential dv/dt = $0.63 \bullet [V_{PK}] = (t_2 - t_1)$

Resistor Capacitor circuit t = RC = $(t_2 - t_1)$

Resistor Capacitor circuit $4 \bullet RC = (t_3 - t_2)$

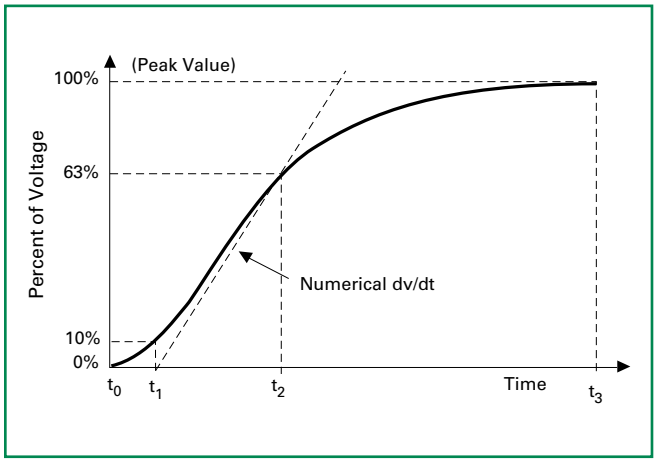


Figure AN1009.2 Exponential dv/dt Waveform

The rate-of-rise of voltage (dv/dt) of a linear waveform is 80% of peak voltage (excluding any overshoots) divided by the time at 90% minus 10% peak voltage. (Figure AN1009.3)

Linear dv/dt = $0.8 = [V_{PK}] = (t_2 - t_1)$

Linear dv/dt = $[0.9 \bullet V_{PK} - 0.1 \bullet V_{PK}] = (t_2 - t_1)$

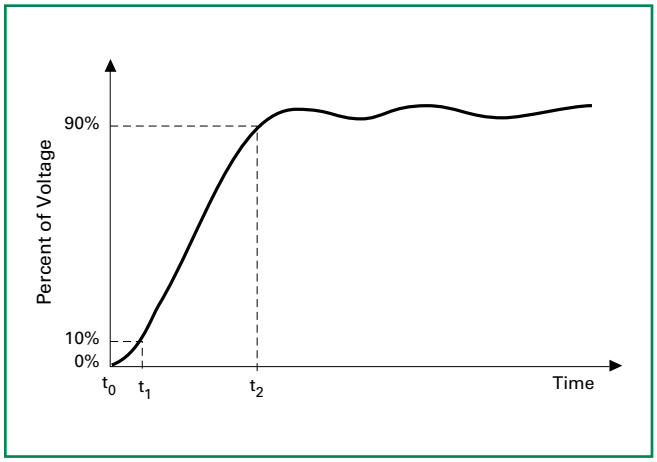
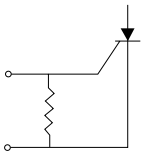


Figure AN1009.3 Linear dv/dt Waveform

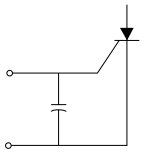
Examples of Gate Terminations



Primary Purpose

(1) Increase dv/dt capability
(2) Keep gate clamped to ensure V_{DRM} capability
(3) Lower t_q time

Related Effect – Raises the device latching and holding current

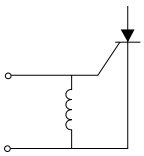


Primary Purpose

(1) Increase dv/dt capability
(2) Remove high frequency noise

Related Effects

(1) Increases delay time
(2) Increases turn-on interval
(3) Lowers gate signal rise time
(4) Lowers di/dt capability
(5) Increases t_q time

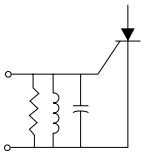


Primary Purpose

(1) Decrease DC gate sensitivity
(2) Decrease t_q time

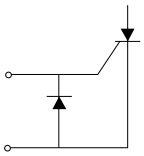
Related Effects

(1) Negative gate current increases holding current and causes gate area to drop out of conduction
(2) In pulse gating gate signal tail may cause device to drop out of conduction



Primary Purpose – Select frequency

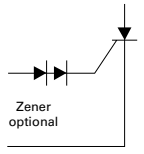
Related Effects – Unless circuit is "damped," positive and negative gate current may inhibit conduction or bring about sporadic anode current



Primary Purpose

(1) Supply reverse bias in off period
(2) Protect gate and gate supply for reverse transients
(3) Lower t_q time

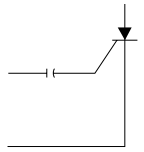
Related Effects – Isolates the gate if high impedance signal source is used without sustained diode current in the negative cycle



Primary Purpose – Decrease threshold sensitivity

Related Effects

(1) Affects gate signal rise time and di/dt rating
(2) Isolates the gate



Primary Purpose – Isolate gate circuit DC component

Related Effects – In narrow gate pulses and low impedance sources, I_{gt} followed by reverse gate signals which may inhibit conduction

Curves for Average Current at Various Conduction Angles

SCR maximum average current curves for various conduction angles can be established using the factors for maximum average current at conduction angle of:

30° = 0.40 x Avg 180°
60° = 0.56 x Avg 180°
90° = 0.70 x Avg 180°
120° = 0.84 x Avg 180°

The reason for different ratings is that the average current for conduction angles less than 180° is derated because of the higher RMS current connected with high peak currents.

Note that maximum allowable case temperature (T_C) remains the same for each conduction angle curve but is established from average current rating at 180° conduction as given in the data sheet for any particular device type. The maximum T_C curve is then derated down to the maximum junction (T_J). The curves illustrated in Figure AN1009.4 are derated to 125 °C since the maximum T_J for the non-sensitive SCR series is 125 °C.

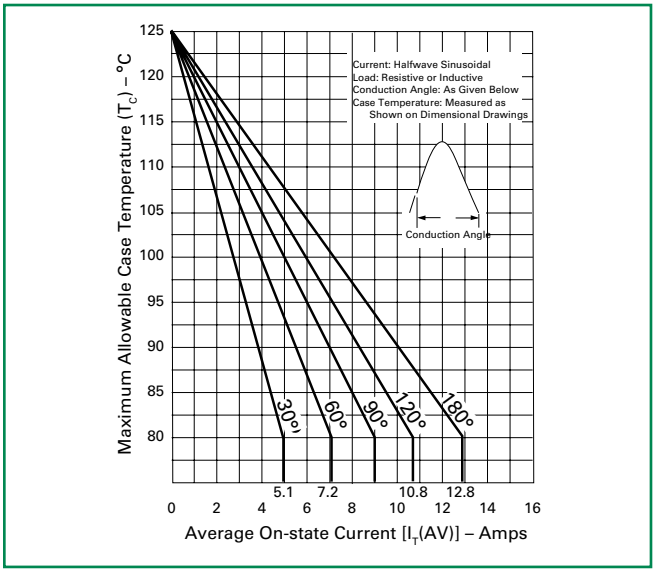


Figure AN1009.4 Typical Curves for Average On-state Current at Various Conduction Angles versus T_C for a SXX20L SCR.

Double-Exponential Impulse Waveform

A double-exponential impulse waveform or waveshape of current or voltage is designated by a combination of two numbers (t_r/t_d or t_r x t_d µs). The first number is an exponential rise time (t_r) or wave front and the second number is an exponential decay time (t_d) or wave tail. The rise time (t_r) is the maximum rise time permitted. The decay time (t_d) is the minimum time permitted. Both the t_r and the t_d are in the same units of time, typically microseconds, designated at the end of the waveform description as defined by ANSI/IEEE C62.1-1989.

The rise time (t_r) of a current waveform is 1.25 times the time for the current to increase from 10% to 90% of peak value. See Figure AN1009.5.

t_r = Rise Time = 1.25 • [t_c - t_a]

t_r = 1.25 • [t(0.9 I_{PK}) - t(0.1 I_{PK})] = T_1 - T_0

The rise time (t_r) of a voltage waveform is 1.67 times the time for the voltage to increase from 30% to 90% of peak value. (Figure AN1009.5)

t_r = Rise Time = 1.67 • [t_c - t_b]

t_r = 1.67 • [t(0.9 V_{PK}) - t(0.3 V_{PK})] = T_1 - T_0

The decay time (t_d) of a waveform is the time from virtual zero (10% of peak for current or 30% of peak for voltage) to the time at which one-half (50%) of the peak value is reached on the wave tail. (Figure AN1009.5)

Current Waveform t_d = Decay Time

= [t(0.5 I_{PK}) - t(0.1 I_{PK})] = T_2 - T_0

Voltage Waveform t_d = Decay Time

= [t(0.5 V_{PK}) - t(0.3 V_{PK})] = T_2 - T_0

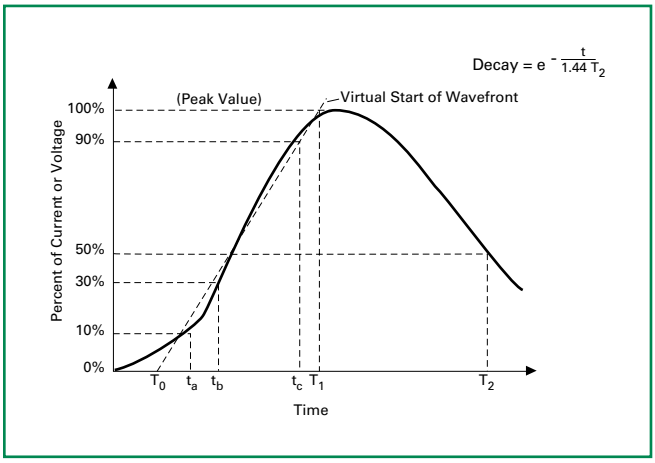


Figure AN1009.5 Double-exponential Impulse Waveform

Failure Modes of Thyristor

Thyristor failures may be broadly classified as either degrading or catastrophic. A degrading type of failure is defined as a change in some characteristic which may or may not cause a catastrophic failure, but could show up as a latent failure. Catastrophic failure is when a device exhibits a sudden change in characteristic that renders it inoperable. To minimize degrading and catastrophic failures, devices must be operated within maximum ratings at all times.

Degradation Failures

A significant change of on-state, gate, or switching characteristics is quite rare. The most vulnerable characteristic is blocking voltage. This type of degradation increases with rising operating voltage and temperature levels.

Catastrophic Failures

A catastrophic failure can occur whenever the Thyristor is operated beyond its published ratings. The most common failure mode is an electrical short between the main terminals, although a Triac can fail in a half-wave condition. It is possible, but not probable, that the resulting short-circuit current could melt the internal parts of the device which could result in an open circuit.

Failure Causes

Most Thyristor failures occur due to exceeding the maximum operating ratings of the device. Overvoltage or overcurrent operations are the most probable cause for failure. Overvoltage failures may be due to excessive voltage transients or may also occur if inadequate cooling allows the operating temperature to rise above the maximum allowable junction temperature. Overcurrent failures are generally caused by improper fusing or circuit protection, surge current from load initiation, load abuse, or load failure. Another common cause of device failure is incorrect handling procedures used in the manufacturing process. Mechanical damage in the form of excessive mounting torque and/or force applied to the terminals or leads can transmit stresses to the internal Thyristor chip and cause cracks in the chip which may not show up until the device is thermally cycled.

Prevention of Failures

Careful selection of the correct device for the application's operating parameters and environment will go a long way toward extending the operating life of the Thyristor. Good design practice should also limit the maximum current through the main terminals to 75% of the device rating. Correct mounting and forming of the leads also help ensure against infant mortality and latent failures. The two best ways to ensure long life of a Thyristor is by proper heat sink methods and correct voltage rating selection for worst case conditions. Overheating, overvoltage, and surge currents are the main killers of semiconductors.

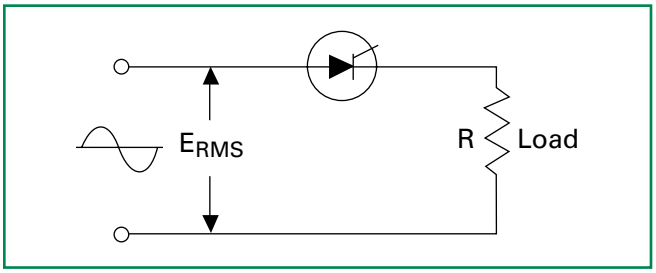
Most Common Thyristor Failure Mode

When a Thyristor is electrically or physically abused and fails either by degradation or a catastrophic means, it will short (full-wave or half-wave) as its normal failure mode. Rarely does it fail open circuit. The circuit designer should add line breaks, fuses, over-temperature interrupters or whatever is necessary to protect the end user and property if a shorted or partially shorted Thyristor offers a safety hazard.

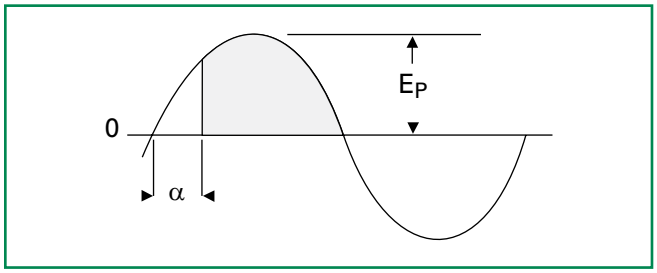
Characteristics Formulas for Phase Control Circuits

Circuit Name	Max Thyristor Voltage	PRV	Max. Load Voltage E_d=Avg. E_a=RMS Load	Load Voltage with Delayed Firing	Max. Average Thyristor or Rectifier Current	
		SCR			Avg. Amps	Conduction Period
Half-wave Resistive Load	1.4 E_{RMS}	E_P	$E_d = \frac{E_p}{\pi}$ $E_a = \frac{E_p}{2}$	$E_d = \frac{E_p}{2\pi}(1+\cos\alpha)$ $E_a = \frac{E_p}{2\sqrt{\pi}}\sqrt{(\pi - \alpha + \frac{1}{2}\sin 2\alpha)}$	$\frac{E_p}{\pi R}$	180°
Full-wave Bridge	1.4 E_{RMS}	E_P	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{2\sqrt{\pi}}(1+\cos\alpha)$	$\frac{E_p}{\pi R}$	180°
Full-wave AC Switch Resistive Load	1.4 E_{RMS}	E_P	$E_a = \frac{E_p}{1.4}$	$E_a = \frac{E_p}{\sqrt{2\pi}}\sqrt{(\pi - \alpha + \frac{1}{2}\sin 2\alpha)}$	$\frac{E_p}{\pi R}$	180°

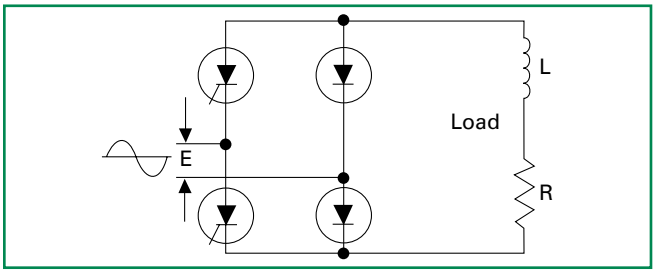
NOTE: Angle alpha (α) is in radians.



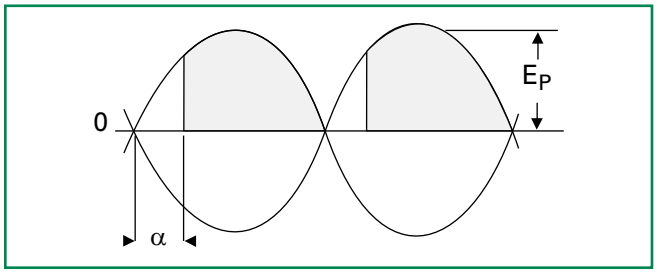
Half-wave Resistive Load - Schematic



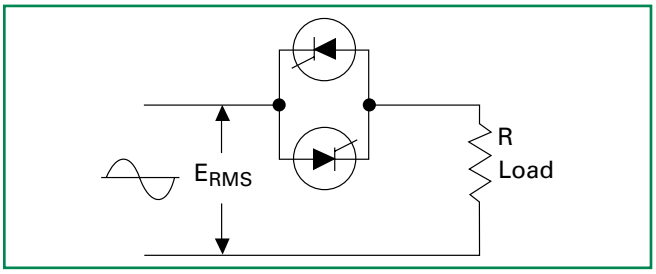
Half-wave Resistive Load - Waveform



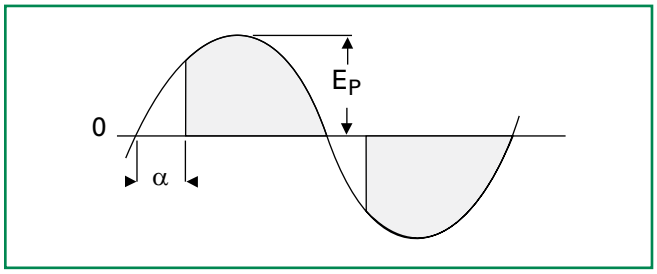
Full-wave Bridge - Schematic



Full-wave Bridge - Waveform



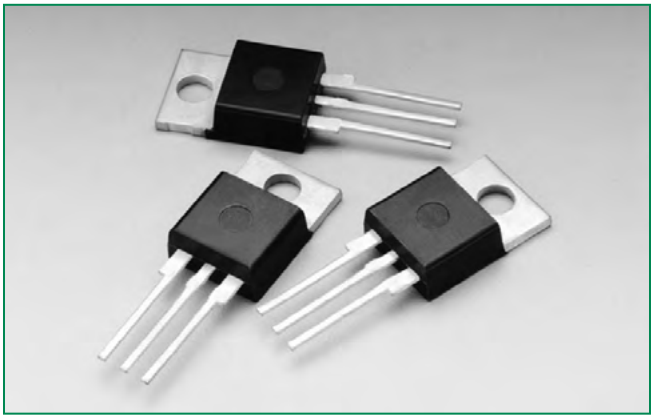
Full-wave AC Switch Resistive Load - Schematic



Full-wave AC Switch Resistive Load - Waveform

Dxx15L & Dxx20L & Dxx25L Series

RoHS



Description

Silicon rectifiers that are excellent for DC phase control applications with motor loads.

Isolated mounting tab allows for use in circuits with common anode or common cathode connections.

Features & Benefits

- RoHS Compliant
- Glass – passivated junctions
- Voltage capability up to 1000 V
- Surge capability up to 350 A

Agency Recognitions

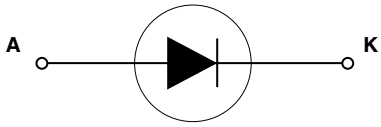
Agency	Agency File Number
	L Package : E71639

Applications

Typical applications are AC to DC solid-state switches for industrial power tools, exercise equipment, white goods, and commercial appliances.

Internally constructed isolated package is offered for ease of heat sinking with highest isolation voltage.

Schematic Symbol



Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	15 / 20 / 25	A
V_{RRM}	400 to 1000	V

Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Value			Unit
			Dxx15L	Dxx20L	Dxx25L	
$I_{F(RMS)}$	RMS forward current	Dxx15L: T_C = 90°C Dxx20L/Dxx25L: T_C = 80°C	15	20	25	A
$I_{F(AV)}$	Average forward current		9.5	12.7	15.9	A
I_{FSM}	Peak non-repetitive surge current	single half cycle; f = 50Hz; T_J (initial) = 25°C	188	255	300	A
		single half cycle; f = 60Hz; T_J (initial) = 25°C	225	300	350	
I^2t	I^2t Value for fusing	t_p = 8.3 ms	210	374	508	A^2s
T_{stg}	Storage temperature range		-40 to 150			°C
T_J	Operating junction temperature range		-40 to 125			°C

Note: xx = voltage

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Electrical Characteristics (T_J = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Value	Unit
t_{rr}	Reverse-recovery Time	I_F=0.9A, I_R=1.5A	TYP.	4	µs

Static Characteristics

Symbol	Test Conditions				Value	Unit
V_{FM}	15A Component I_T = 30A; t_p = 380µs			MAX.	1.6	V
	20A Component I_T = 40A; t_p = 380µs					
	25A Component I_T = 50A; t_p = 380µs					
I_{RM}	V_{RRM}	T_J = 25°C	400-600V	MAX.	10	µA
			800-1000V		20	
		T_J = 100°C	400-800V		500	
			1000V		3000	
		T_J = 125°C	400-800V		1000	

Thermal Resistances

Symbol	Parameter		Value	Unit
$R_{\theta(JC)}$	Junction to case (AC)	Dxx15L	2.60	°C/W
		Dxx20L	2.55	
		Dxx25L	2.50	

Note: xx = voltage

Figure 1: On-State Current vs. On-State Voltage (Typical)

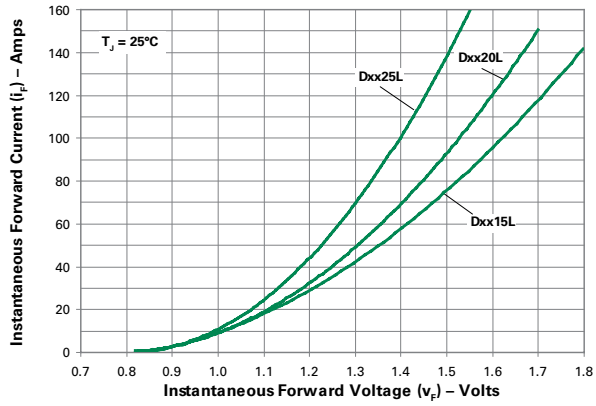

Figure 2: Power Dissipation vs. Average Forward On-State Current (Typical)

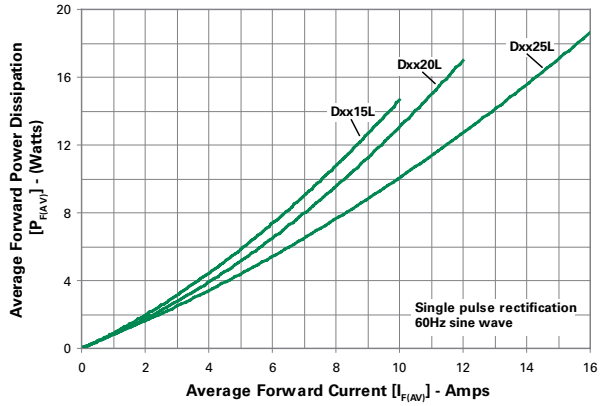

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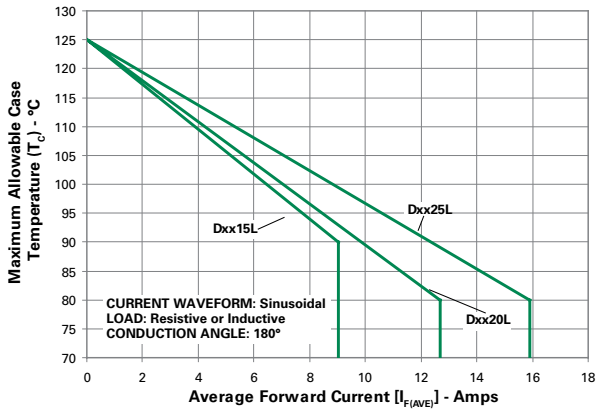
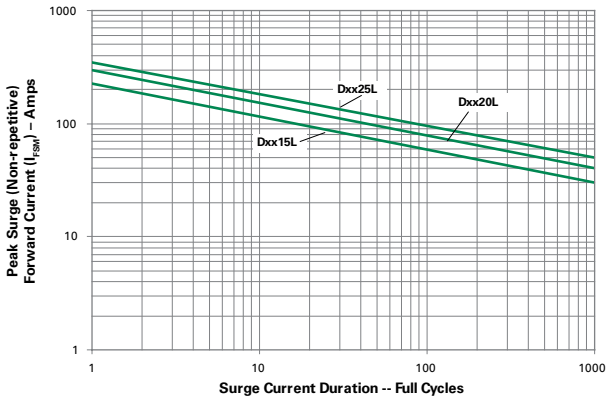
Figure 3: Maximum Allowable Case Temperature vs. Average On-State Current



Note: xx = voltage

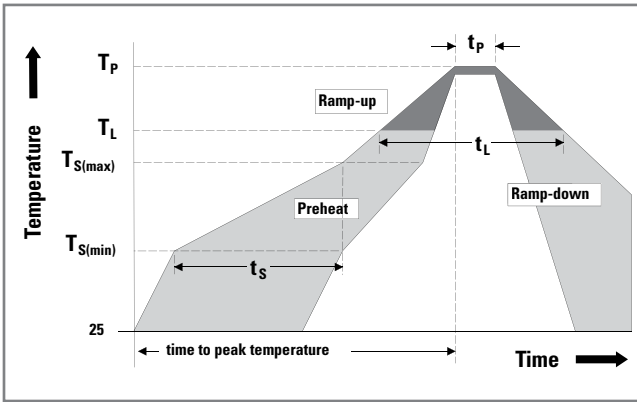
Figure 4: Surge Peak On-State Current vs. Number of Cycles



Supply Frequency: 60Hz Sinusoidal
Load: Resistive
RMS Forward Current : [$I_{T(RMS)}$]: Maximum Rated Value at Specific Case Temperature

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus Temp) (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Time (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		280°C



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Physical Specifications

Terminal Finish	100% Matte Tin Plated
Body Material	UL Recognized compound meeting flammability rating V-0
Lead Material	Copper Alloy

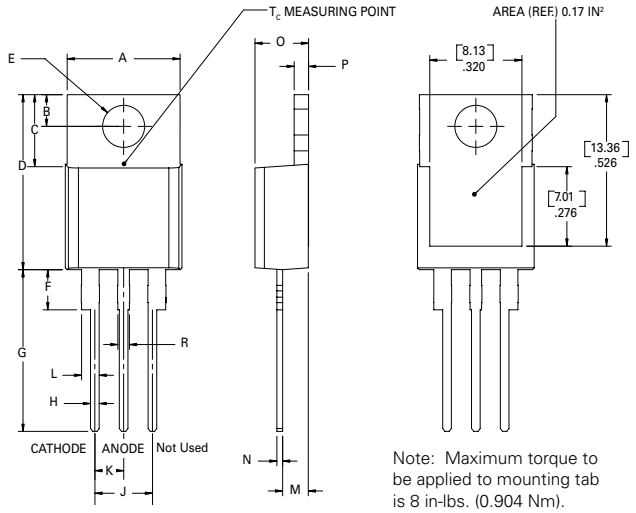
Design Considerations

Careful selection of the correct component for the application's operating parameters and environment will go a long way toward extending the operating life of the rectifier. Good design practice should limit the maximum continuous current through the main terminals to 75% of the component rating. Other ways to ensure long life for a power discrete semiconductor are proper heat sinking and selection of voltage ratings for worst case conditions. Overheating, overvoltage (including dv/dt), and surge currents are the main killers of semiconductors. Correct mounting, soldering, and forming of the leads also help protect against component damage.

Environmental Specifications

Test	Specifications and Conditions
High Temperature Voltage Blocking	MIL-STD-750: Method 1040, Condition A Rated V_{RRM}, 125°C, 1008 hours
Temperature Cycling	MIL-STD-750: Method 1051 -40°C to 150°C, 15-minute dwell, 100 cycles
Biased Temperature & Humidity	EIA/JEDEC: JESD22-A101 320VDC, 85°C, 85%RH, 1008 hours
High Temp Storage	MIL-STD-750: Method 1031 150°C, 1008 hours
Low-Temp Storage	1008 hours; -40°C
Resistance to Solder Heat	MIL-STD-750: Method 2031 260°C, 10 seconds
Solderability	ANSI/J-STD-002, Category 3, Test A
Lead Bend	MIL-STD-750: Method 2036, Condition E

Dimensions — TO-220AB (L-Package) — Isolated Mounting Tab



Note: Maximum torque to be applied to mounting tab is 8 in-lbs. (0.904 Nm).

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.380	0.420	9.65	10.67
B	0.105	0.115	2.67	2.92
C	0.230	0.250	5.84	6.35
D	0.590	0.620	14.99	15.75
E	0.142	0.147	3.61	3.73
F	0.110	0.130	2.79	3.30
G	0.540	0.575	13.72	14.61
H	0.025	0.035	0.64	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.91
M	0.085	0.095	2.16	2.41
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.045	0.060	1.14	1.52
R	0.038	0.048	0.97	1.22

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Teccor® brand Diodes

15 / 20 / 25 Amp Rectifiers

Product Selector

Part Number	Voltage				Type	Package
	400V	600V	800V	1000V		
Dxx15L	X	X	X	X	Rectifier	TO-220L
Dxx20L	X	X	X	X	Rectifier	TO-220L
Dxx25L	X	X	X	X	Rectifier	TO-220L

Note: xx = Voltage

Packing Options

Part Number	Marking	Weight	Packing Mode	Base Quantity
Dxx15LTP	Dxx15L	2.2 g	Tube	500 (50 per tube)
Dxx20LTP	Dxx20L	2.2 g	Tube	500 (50 per tube)
Dxx25LTP	Dxx25L	2.2 g	Tube	500 (50 per tube)

Note: xx = Voltage

Part Numbering System

D 60 15 L 59

DEVICE TYPE
D: Rectifier

VOLTAGE RATING
40: 400V
60: 600V
80: 800V
K0: 1000V

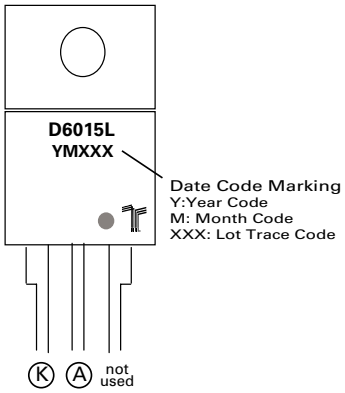
CURRENT RATING
15: 15A
20: 20A
25: 25A

PACKAGE TYPE
L: TO-220 (Isolated)

LEAD FORM DIMENSIONS
xx: Lead Form Option

Part Marking System

TO-220AB - (L Package)



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