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White paper

Modelling High Speed Semiconductor Fuses in Maritime DC Microgrids



A technical white paper on aR fuse representation, DC interruption, discrimination and assembly withstand



Author: Peter van den Berg
E-mail: p.vandenberg@astrolkwx.com

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Author	Peter van den Berg, Senior technical consultant power electronics
Organisation	Astrolkwx B.V.
Contributor	László Kristóf, Senior field applications engineer
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Primary application	Maritime low-voltage DC distribution and converter systems
Reference bus voltage	1,000 V DC
Emerging voltage class	Toward 1,500 V DC, with nominal, maximum operating and recovery voltage defined per project
Typical effective fault time constant	Below 3 ms
Fuse class	High-speed semiconductor fuse-links, principally aR
Audience	Power-system engineers, protection specialists, model developers, equipment manufacturers and classification reviewers

Executive summary

This technical white paper addresses the representation of high-speed semiconductor fuse-links, principally utilisation category aR, in dynamic simulations of maritime DC microgrids. The application is centred on nominal 1,000 V DC systems and considers the emerging equipment and system class extending toward 1,500 V DC. The maximum operating and recovery voltages remain project-specific, and effective fault-current time constants are frequently below 2 to 3 ms. Under these conditions, conventional AC time-current characteristics and standardised DC test assumptions do not necessarily describe the actual fault waveform or post-melting interruption duty.

Pre-arcing behaviour should be assessed from the actual simulated current waveform. For a fast event, the catalogue cold pre-arcing I^2t is an adiabatic minimum and can be used as a conservative earliest-melting bound. A more realistic estimate uses the applicable time-current characteristic or a calibrated electrothermal model, including initial loading, temperature and tolerance. The fuse should therefore be represented as a hybrid electrothermal component: a low-resistance conducting state with an I^2t or thermal melting criterion, followed by a nonlinear arcing state and finally an open circuit. Catalogue data generally do not define a unique electrical equivalent for the arcing interval. Accurate prediction of clearing time, peak let-through current and arc voltage requires manufacturer-validated parameters, applicable test results or conservative verified bounds.

The required model fidelity should be determined by whether the post-melting interval can materially alter the engineering conclusion. Detailed clearing behaviour may be non-decisive for switchboard structural verification where independently demonstrated DC short-circuit withstand comfortably exceeds the prospective duty. It remains relevant where interruption capability, semiconductor survival, cable protection, selectivity, transient voltage or conditional assembly withstand depends on fuse current limitation. The approximately 25% withstand-rating headroom encountered during marine classification reviews is therefore treated as project experience, not as a universal class or IEC threshold.

Purpose. This paper defines a defensible method for representing high-speed semiconductor fuses in dynamic DC-microgrid studies. It separates pre-arcing prediction, DC interruption verification, system discrimination and assembly withstand verification. The intended result is a model whose fidelity is matched to the engineering decision being made.

Principal conclusion. The actual simulated fault-current waveform should drive the pre-arcing assessment. Catalogue AC time-current curves and total-clearing data are not, by themselves, sufficient to reconstruct the post-melting behaviour of a fuse in a low-time-constant DC network. Detailed arcing representation is necessary only where that interval can change a compliance, coordination or component-survival conclusion; otherwise a bounded or manufacturer-validated representation is more defensible than an unverified detailed model.

1 Scope and engineering basis

This note addresses system studies in which high-speed semiconductor fuses are used as local protection for converters, drives, battery branches or other power-electronic equipment, and as elements in distribution discrimination. It is centred on nominal 1,000 V DC maritime systems and also considers systems and equipment extending toward the 1,500 V DC class. The method applies provided that the available fuse data and equipment ratings are valid for the actual operating and recovery voltages, prospective current, circuit energy and fault topology.

The note does not provide a generic type-selection table for individual fuse part numbers. Product suitability remains dependent on the specific fuse series, current rating, maximum DC voltage, minimum breaking current, time constant, mounting, preloading and tested interruption capability. Nor does the note replace the short-circuit study or the approval basis agreed with the applicable classification society.

1.1 Status of information

Category	Basis used in this note	Treatment
Established	IEC scope and definitions; manufacturer-published dependencies of pre-arcing and clearing performance	Referenced to IEC and manufacturer guidance
Project input	Nominal 1,000 V DC reference; project-specific operating and recovery voltages; emerging equipment and systems extending toward the 1,500 V DC class; typical effective time constants below 2 to 3 ms	Used as application boundary conditions
Observed practice	Review scrutiny reduces where distribution-assembly withstand has substantial margin; about 25% rating headroom has been encountered repeatedly	Presented as experience, not a class rule
Derived	Waveform integrals and utilisation factors	Equations are traceable and suitable for model implementation
Engineering judgement	Choice of model level and manufacturer-validation trigger	Applied through explicit decision criteria

1.2 Terminology

Clearing time is used for the interval from fault initiation until interruption, comprising pre-arcing time and arcing time. Clearance time is avoided because it can be confused with insulation clearance. Breaking capacity applies to the protective device. Busbars, supports and switchgear assemblies are assessed by short-circuit withstand quantities such as rated short-time withstand current, rated peak withstand current or a conditional short-circuit rating.

2 Why catalogue data do not define a DC transient model

Published fuse data are performance descriptors measured under defined conditions. They normally include a time-current characteristic, minimum pre-arcing I^2t, total-clearing I^2t at one or more voltages, cut-off current and peak arc-voltage information. These data constrain a model, but do not uniquely determine its internal thermal state or dynamic arc resistance.

The distinction is particularly important for AC-rated square-body fuses considered for DC use. Eaton states that DC interrupting capability depends on the combined applied DC voltage, circuit L/R, minimum prospective short-circuit current and fuse pre-arcing I^2t, and recommends proof after the selection procedure because the procedure is a guideline [1]. Littelfuse similarly treats DC interruption as dependent on the DC circuit and test conditions rather than as a direct transfer of the AC rating [2].

A conventional AC time-current curve also uses prospective symmetrical RMS current and virtual pre-arcing time. A maritime DC fault can be a composite transient with no single prospective RMS current, no periodic current zero and no single meaningful L/R. Fitting a detailed electrical equivalent circuit to one AC curve can therefore create numerical precision without physical validity.

2.1 The time constant belongs to the circuit

The 10 ms value frequently encountered in application literature is primarily a characteristic of the DC test circuit, not an inherent fuse time constant. The project range below 2 to 3 ms is therefore not a correction factor to the fuse itself. It changes the current rise, stored magnetic energy and arc-extinction duty experienced by the fuse.

A short L/R generally produces a rapid rise toward the resistively limited current. For comparable resistance and current, it also implies lower inductance and less stored magnetic energy. It can accelerate melting and increase early peak stress, yet reduce one component of the post-melting interruption burden. This does not prove interruption capability: recovery voltage, minimum prospective current, capacitor energy, source persistence and the fuse's arc-voltage capability remain decisive.

2.2 Composite DC faults

In a DC microgrid, the fuse current may include parallel or sequential contributions from DC-link capacitors, batteries, rectifiers, controlled converters, rotating machines and adjacent sections through bus ties. The relevant waveform is therefore:

$$i_fuse(t) = i_C(t) + i_battery(t) + i_converter(t) + i_machine(t) + i_adjacent(t)$$

Some terms can reverse or cease when control or protection acts. The waveform can contain a steep initial impulse, a limited plateau and a slower sustained tail. A triangular approximation may be useful for a conservative screening case, but it should not replace the simulated waveform when the stated purpose is discrimination or equipment verification.

IEC 61660-1 and IEC 61660-2 provide useful background for separating DC source contributions and assessing short-circuit effects [6, 7]. Their formal scope is DC auxiliary installations in power plants and substations, so they are supporting references rather than a direct maritime application standard.

3 Required modelling outputs

The model should be judged by the outputs required for the protection decision, not by how closely it resembles a physical fuse internally. The minimum output set is listed below.

Output	Purpose	Required evidence
Pre-arcing time	Determine whether and when the element melts	Actual i(t), initial thermal state and applicable pre-arcing threshold
Accumulated pre-arcing I^2t	Coordinate with upstream fuses and protected components	Numerical integral of the actual waveform
Peak let-through current	Check semiconductor and electrodynamic stress	Dynamic or conservative bounded clearing representation
Total-clearing I^2t	Check semiconductor, cable and conditional assembly duty	Manufacturer data corrected for the relevant voltage or validated dynamic model
Peak fuse voltage	Check insulation and semiconductor overvoltage	Arc-voltage data plus network transient model
Final interruption	Confirm that current reaches zero and remains interrupted	Valid DC interruption capability at the actual recovery voltage and source duty

4 Pre-arcing model

For sufficiently fast high-current faults, pre-arcing can be represented by an energy accumulator. The catalogue cold pre-arcing I^2t corresponds to the ideal adiabatic limit; measured melting integrals can be higher because some heat transfers from the restrictions to the remainder of the element and the surrounding filler. The primary state is:

$$J(t) = \int_0^t i_fuse^2(\xi)\, d\xi$$

For sampled simulation data, trapezoidal integration avoids imposing an artificial fault shape:

$$J_k = J_{k-1} + \tfrac{1}{2}(i_k^{\,2} + i_{k-1}^{\,2})\,\Delta t$$

For a conservative earliest-melting check, the model changes state when J reaches the applicable cold minimum pre-arcing I^2t. For a realistic waveform-driven estimate, derive the cumulative RMS current-time locus from the actual prospective waveform and compare it with the applicable time-current curve; at the intersection, $I^2t = I_RMS^2t$. Any threshold or curve should be parameterised by fuse type and should retain tolerance, initial loading and temperature as explicit inputs. Catalogue total-clearing I^2t must not be used as the melting trigger.

4.1 Analytic check for a simple RL source

A single-source RL fault can be used as a unit test. For a DC step E applied to R and L:

$$i(t) = I\infty(1 - e\text{^}(-t/\tau)) \quad with \quad I\infty = E/R \quad and \quad \tau = L/R$$

The corresponding integral is:

$$J(t) = I\infty^2[t - 2\tau(1 - e\text{^}(-t/\tau)) + \tfrac{1}{2}\tau(1 - e\text{^}(-2t/\tau))]$$

Agreement between this expression and the numerical integrator is a useful software-verification test. It is not a substitute for the multi-source network model.

4.2 Thermal memory

A pure I^2t trigger is appropriate only in the adiabatic region. Repetitive overloads, cycling and events approaching the thermal time scale require a thermal-memory state, for example a first-order or manufacturer-calibrated network driven by i^2R. The short-circuit model should import this state at fault initiation. Resetting J to zero at every event can overstate the available pre-arcing margin.

5 Arcing and clearing representation

At melting, the fuse ceases to be a low-value conductor and becomes a nonlinear interruption device. Arc voltage, source voltage, inductive energy, capacitor energy and network commutation jointly determine the subsequent current. An I^2t accumulator alone cannot predict this interval.

The recommended implementation is a state-based component with four externally visible states:

$$NORMAL \rightarrow PRE\text{-}ARC \rightarrow ARCING \rightarrow OPEN$$

NORMAL and PRE ARC may share the same electrical resistance while retaining different diagnostic states. ARCING should use a controlled voltage or nonlinear resistance model that has been calibrated against manufacturer data or test results. OPEN is entered only after current has reached the defined extinction criterion and the model has verified that restrike is not being represented.

5.1 Three levels of model fidelity

Level	Representation	Appropriate use	Not sufficient for
1	Actual-waveform pre-arcing model followed by ideal opening or conservative delay	Melting assessment where post-melting behaviour cannot change the design conclusion and DC interruption capability is independently established	Predicting peak arc voltage, detailed current limitation or uncertain DC interruption
2	Pre-arcing model plus bounded arcing interval using verified limits for total I^2t, peak let-through and peak arc voltage	Compliance screening and coordination where conservative bounds preserve the conclusion	Optimising small margins or extrapolating beyond the verified data envelope
3	Manufacturer-validated or test-calibrated dynamic arc model using the actual waveform and network	Small margins, non-standard waveforms, conditional assembly ratings, semiconductor survival and critical selectivity	Use outside the validated voltage, current, L/R and topology envelope

5.2 Numerical implementation

- Use a solver maximum step substantially shorter than the smallest relevant pre-arcing or commutation feature. Demonstrate time-step convergence rather than specifying one universal sample time.
- Include fuse cold resistance where it materially affects a low-resistance fault path. For parallel fuses, model branch resistances and tolerances individually.
- Avoid an instantaneous resistance jump to an arbitrarily large value. It can create non-physical voltage impulses and solver-dependent results.

- Log state transition time, J, peak current, total I²t, peak fuse voltage and extinction time for every case.
- Run at least nominal, conservative-high source and conservative-low interruption-current cases. The lowest sustainable fault current can be more critical to DC interruption than the maximum fault current.

5.3 Electrical equivalent for Simulink and equivalent tools

There is no single, universally correct lumped electrical equivalent for an aR fuse that can be reconstructed from normal catalogue data. The defensible equivalent is a hybrid electrothermal behavioural component. It retains a low-resistance conducting branch until a melting criterion is reached, changes to a product-specific nonlinear arcing branch, and becomes open only after current extinction. This representation is electrically causal and makes the boundary between calculated and manufacturer-validated behaviour explicit.

Model state	Electrical representation	State variable or transition evidence
NORMAL	Temperature-dependent fuse resistance Rf(Tf); include allocated connection or fuse inductance only if it is known	Initial temperature, loading and thermal history
PRE-ARC	Same conducting branch; the separate state is primarily diagnostic	Accumulated ∫i²dt or a calibrated electrothermal melting criterion
ARCING	Controlled opposing voltage source or calibrated nonlinear arc resistance	Manufacturer calculation, applicable DC test data or conservative verified bounds
OPEN	Open switch or sufficiently high resistance after extinction	Current below the extinction criterion, with any restrike assumption stated

In the intact states, the minimum electrical relation is:

$$v_f = R_f(T_f)\, i_f$$

For short, approximately adiabatic faults, the melting state may be represented by:

$$dJ/dt = i_f^2 \quad with\ transition\ when \quad J \geq (I^2t)pre\text{-}arcing$$

For repetitive loading or longer events, thermal memory should replace or supplement the simple accumulator, for example:

$$C_th\, dT_f/dt = i_f^2\, R_f(T_f) - (T_f - T_a)/R_th$$

The thermal parameters in this illustrative first-order form still require calibration. It should not be inferred that a catalogue pre-arcing I²t value uniquely supplies Cth or Rth.

During arcing, a generic implementation can impose an opposing fuse voltage such as:

$$v_f = sgn(i_f)[V_0(x) + r_a(x, i_f)/i_f]$$

Here x represents one or more arc-progress states. This equation is a model structure, not a fuse law. The functions V_0 and ra cannot be uniquely identified from a time-current curve, pre-arcing and total-clearing I²t, one cut-off curve and one peak arc-voltage curve. A simple resistance ramp can be adjusted to match one of those quantities while still producing an incorrect peak current, clearing time or arc voltage under a different voltage or L/R. Accurate post-melting prediction therefore requires manufacturer-derived parameters or test calibration over the intended operating envelope.

A practical Simulink or Simscape implementation comprises the following elements:

1. A current sensor and numerical i^2 integrator, with the initial thermal or utilisation state supplied by the preceding load history.
2. A state machine implementing NORMAL, PRE-ARC, ARCING and OPEN, including explicit melting and extinction criteria.
3. A low-resistance branch for the intact fuse and a controlled voltage source or calibrated nonlinear resistance for the arcing interval.
4. An open-state switch entered after extinction, with numerical snubbers disclosed separately from the physical model.
5. Output logging for pre-arcing time, total I^2t, peak current, peak fuse voltage, clearing time and the final interruption state.

Fuse inductance requires particular care in low-L/R networks. Include only the inductance physically attributable to the fuse and its connections, and only once. If the busbar or cable model already contains that geometry, adding a second generic fuse inductance double-counts it and can materially reduce the calculated di/dt. Numerical snubbers and parasitic elements used for solver stability must be documented and demonstrated not to change the protection result.

For parallel installations, each fuse-link requires its own resistance, temperature or J state and manufacturing tolerance so that current redistribution after the first melting event can develop naturally. For series installations, each fuse-link requires its own arcing state; equal sharing of the recovery or arc voltage must not be imposed without manufacturer evidence for the arrangement.

Recommended statement. An aR fuse cannot be represented by one universally valid electrical equivalent derived from catalogue data. For system simulation it should be represented as a hybrid electrothermal component: a low-resistance conducting state with an I^2t or thermal melting criterion, followed by a product-specific nonlinear arcing state and finally an open circuit. Use the actual simulated current waveform for pre-arcing assessment. The cold catalogue I^2t gives a conservative adiabatic bound; the applicable time-current curve or a calibrated electrothermal model gives the more realistic melting estimate. Accurate DC clearing, current limitation and arc voltage require manufacturer-validated data or conservative verified bounds.

6 Voltage application and the 1500 V DC class

The worked baseline in this paper is a nominal 1,000 V DC maritime bus. Actual voltage can be lower or higher depending on the source configuration, battery state of charge, converter control, regeneration and operating condition. The fuse study shall therefore use the maximum credible voltage appearing across each fuse during interruption rather than the nominal bus label. It should also determine whether pole-to-pole and pole-to-ground faults, source commutation or unequal voltage sharing produce different recovery duties.

Systems and power-conversion equipment extending toward the 1,500 V DC class are emerging, particularly in combination with battery energy-storage systems. Public developments include dedicated 1,500 V DC converter technology and a 1,500 V DC power-conversion system for BESS applications [11, 12]. IEC 60269-4:2024 and IEC 60092-302-2:2025 extend their respective low-voltage scopes to 1,500 V DC [3, 4]. These facts establish a relevant future equipment and standards envelope; they do not establish 1,500 V DC as a universally used nominal maritime bus voltage or assign that rating to an individual fuse or assembly. In a so-called 1,500 V system, the study shall identify whether 1,500 V is nominal voltage, maximum operating voltage or equipment rating.

6.1 AC-rated fuse-links used in DC

The fact that a fuse belongs to an AC series commonly applied in DC systems is not sufficient evidence for a specific DC duty. Eaton's published method for selected 660, 690, 1,000 and 1,250 V AC square-body series relates DC capability to applied voltage, L/R, minimum prospective current and pre-arcing I^2t, and explicitly recommends proof of the selected fuse [1]. The model file should therefore identify the exact part number and the manufacturer's accepted DC operating envelope.

For aR fuse-links, minimum breaking current also matters. The network must either ensure that every credible fault entering the arcing state remains within a demonstrated interruption range or provide backup protection for lower sustained currents. High maximum short-circuit capacity does not establish low-current DC interruption capability.

6.2 Series and parallel arrangements

Arrangement	Required modelling treatment	Invalid shortcut
Series	Model the actual fault path and manufacturer-supported voltage sharing; include tolerances and simultaneous or sequential arcing	Dividing the system recovery voltage equally by the number of series fuses without evidence
Parallel	Use one fuse model per branch with resistance, temperature and I^2t tolerance; allow current transfer after the first branch melts	Multiplying one fuse's current or I^2t capability by the number of parallel paths
Two-pole fault path	Identify whether both pole fuses carry and interrupt the same fault and whether either can see the full recovery voltage	Assuming two fuses always share arc voltage equally because both are in the schematic fault path

6.3 Case study Eaton 180D dedicated DC fuse series

This case study examines Eaton Bussmann series 180D size 3 fuse-links as a dedicated DC example. The evidence comprises public Technical Data TD135027EN, the supplied engineering datasheet 180K0028 Revision A, the associated UL report and certificates, Eaton technical clarification, customer-version proving reports DHK-4054 and DHK-4070, and a manufacturer-supplied 3 ms peak let-through characteristic [8-10, 13-15]. DHK-4054 tested prototype NPDHU733, identified as the development code for saleable 180D8734; DHK-4070 tested 180D8734. The confidential draft circuit drawings are not reproduced. The 3 ms graph is reproduced in Figure 1, while its underlying engineering data remain proprietary. Product selection and conformity remain subject to current controlled Eaton documents.

Item	Supplied documentation	Engineering relevance
Product scope	Size 3, 1,500 V DC, utilisation categories aR and aBat, 350 to 1,400 A	The voltage rating is directly stated for DC; no AC-to-DC voltage conversion is needed for initial screening
Maximum interruption	100 kA at L/R = 10 ms and 250 kA at L/R = 3 ms	The two stated duties establish product-envelope validation points; they do not define a general conversion between time constant and interruption capacity

Item	Supplied documentation	Engineering relevance
Pre-arcing data	Cold pre-arcing I^2t from 25,000 to 1,420,000 A^2s across the range, plus a pre-arcing time-current curve; the cold values are adiabatic minima	Use the cold value as a conservative earliest-melting bound and the time-current curve with the actual waveform's cumulative RMS profile for a realistic estimate
Minimum interruption	Rating-specific values in the datasheet; the UL report gives 800% for the homogeneous range	Use the rating-specific datasheet minimum for engineering studies and apply current UL conditions separately where UL recognition is required
Let-through data	The published datasheet includes a peak let-through curve for L/R = 10 ms. Eaton has also supplied an accurate rating-specific peak let-through characteristic at L/R = 3 ms for 350 to 1,400 A. The 1,400 A proving tests record 66.8 to 67.2 kA peak cut-off at 256 kA prospective current.	Use the 3 ms characteristic as manufacturer-supplied Level 2 validation data for peak current within its stated voltage, L/R, current and fuse-rating envelope. It does not define clearing time, total I^2t, arc voltage or a universal arc model.
Conformity wording	UL wording on current limitation and let-through remains part of the recognition file; Eaton intends to raise the terminology with UL	Do not infer the transient model from the UL wording; use the datasheet and proving reports as technical evidence and verify UL conformity separately

6.3.1 Fit with low time constant maritime systems

The direct 1,500 V DC rating places the 180D series within the emerging voltage class considered in this paper. Voltage utilisation shall nevertheless be calculated for the maximum credible recovery voltage in each project rather than for a fixed assumed system maximum:

$$K_V = V_{recovery,max} / V_{fuse,rated}$$

A direct 1,500 V DC rating gives a clearer application basis than an AC-origin product requiring a DC conversion procedure. Eaton documents a 250 kA class interruption duty at approximately 3 ms and a 100 kA class duty at approximately 10 ms [13, 14]. The 3 ms duty is relevant to the target maritime systems, but each result remains tied to its prospective current, recovery voltage and rectifier-fed test circuit. It is a product-envelope validation point, not a general arc law.

Eaton confirms that L/R describes the effective RL test-circuit condition. For a comparable RL source, a shorter time constant means less inductance and less stored magnetic energy for the fuse to absorb during arcing. Eaton's application position is therefore that capacitor- and BESS-dominated faults with a faster rise than the 3 ms duty do not require additional assessment solely because their effective time constant is shorter. This conclusion remains conditional on the selected part number staying within its DC voltage and recovery-voltage limits, minimum and maximum interruption currents, installation conditions and topology. Persistent converter, battery or multi-source contributions must still be represented in the system study.

6.3.2 Consequences for simulation

Modelling task	What becomes more direct	What remains unresolved
Voltage application	Use the stated 1,500 V DC product rating and the actual recovery voltage	Transient overvoltage and unequal voltage sharing still require a network model
Melting prediction	Integrate actual i(t); use cold pre-arcing I^2t as an adiabatic minimum and the time-current curve with the cumulative RMS profile for a realistic estimate	Initial loading, tolerance, temperature and thermal memory still require treatment
Interruption screening	Compare the defined case with the documented 3 ms and 10 ms rectifier-fed test envelopes; Eaton accepts faster-rise capacitor and BESS duties without extra review solely because of time constant	Recovery voltage, rating-specific minimum breaking current, maximum interrupting current and persistent multi-source contributions remain project-specific
Detailed clearing	Use the manufacturer-supplied 3 ms characteristic to validate rating-specific peak let-through and use the measured 3 ms and 10 ms current, voltage, time and Joule-integral results as duty-specific validation points.	The characteristic does not define the current waveform or residual tail-current duration, and no general dynamic arc law is supplied.
Model implementation	A Level 1 melting model and a Level 2 model constrained by the 3 ms peak characteristic and test-based energy and voltage data can be created without AC-to-DC voltage extrapolation.	A Level 3 arc model still requires manufacturer parameters or project-specific calibration.

The 180D series makes product application more direct, but does not provide a universal arc model. The new 3 ms peak let-through characteristic adds a rating-specific target for validating the simulated peak current. The proving reports add measured current, voltage, pre-arcing time, arcing time, cut-off current, fuse voltage and Joule integral at specific 3 ms and 10 ms duties. Together, these data support Level 2 validation of peak current and bounded behaviour within the documented envelope. Eaton's explanation of the low-amplitude tail current also confirms that final extinction time cannot be predicted from the catalogue melting data, the peak let-through characteristic or a fixed resistance ramp.

6.3.3 Test evidence and modelling implications

The proving reports identify the applied voltage, prospective current, L/R, recovery voltage and measured fuse current and voltage for each operation [13, 14]. Eaton also supplied draft test-circuit drawings to clarify the source arrangement and measurement locations, together with the 3 ms peak let-through characteristic [15]. The confidential drawings are not reproduced. Figure 1 reproduces the supplied characteristic, but the proprietary data used to construct it are not disclosed. The conclusions below use the report results, the characteristic and Eaton's written technical explanation.

The 1,400 A 180D8734 passed three high-current operations at 256 kA prospective current, 1,587 V applied voltage and 3.01 ms L/R. Recovery voltage was approximately 1,580 V. Peak cut-off current was

66.8 to 67.2 kA and maximum recorded fuse voltage was 1,885 to 1,921 V [14]. The 1,400 A trace in the supplied 3 ms characteristic is consistent with this measured high-current anchor. The elevated proving voltage is a test condition and does not increase the product's 1,500 V DC application rating.

The 3 ms characteristic relates prospective DC current to peak let-through current for each size 3 rating from 350 to 1,400 A [15]. Eaton regards the characteristic as accurate application data, although its construction uses proprietary engineering information and not every plotted point is a separately disclosed test result. In a simulation workflow, the characteristic can be digitised as a rating-specific Level 2 lookup or acceptance target for peak current. Its use remains limited to a compatible 1,500 V DC, 3 ms RL duty and to the selected link's documented current envelope. A plotted line must not be treated as evidence of interruption above the 250 kA maximum breaking capacity or below the rating-specific minimum breaking current. The characteristic also cannot provide total-clearing I^2t, peak fuse voltage, clearing time or the detailed current waveform.

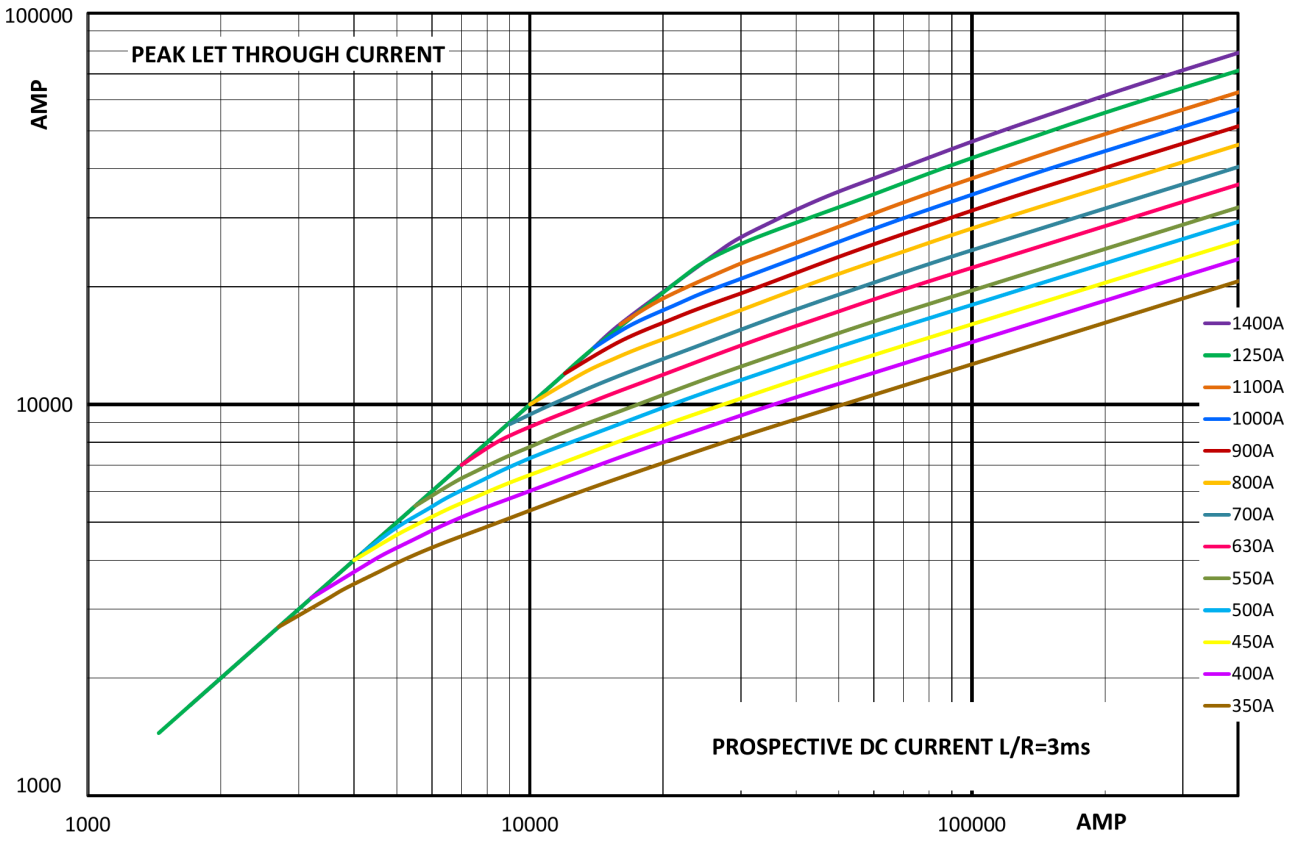


Figure 1. Eaton 180D size 3 peak let-through characteristic at 1,500 V DC and L/R = 3 ms [15]. The graph is manufacturer-supplied application data; its underlying proprietary data are not disclosed.

Pre-arcing time in the three 3 ms operations was 0.950 to 0.980 ms. Arcing time ranged from 9.57 to 26.2 ms and total clearing time from 10.6 to 27.2 ms; measured total Joule integral was approximately 5.65 to 5.79 million A^2s [14]. Eaton attributes the arcing-time spread to a low-amplitude oscillatory tail after the main current has been strongly limited. The tail follows recovery-voltage ripple and is likely associated with final inductive-energy discharge through weakly conductive residual arc plasma. Its duration can be estimated only roughly. A deterministic clearing-time law cannot be inferred from these tests.

For comparison, the 10.5 ms development-link tests at 100.5 kA and 1,595 V applied voltage gave pre-arcing times of 5.10 to 5.22 ms and total times of 21.5 to 28.0 ms [13]. A subsequent 180D8734 operation at 105 kA, 1,535 V and 10.2 ms L/R cleared in 18.6 ms [14]. Because prospective current and voltage differ from the 3 ms tests, the results should not be used to derive a direct L/R-to-clearing-time conversion.

For the 1,400 A link, the datasheet gives a cold pre-arcing integral of 1.42 million A²s [8]. The measured values were approximately 1.51 to 1.54 million A²s at the 3 ms duty and 2.48 to 2.64 million A²s at the 10.5 ms high-current duty [13, 14]. Eaton explains that the catalogue value is the ideal adiabatic minimum, calculated from the total element cross-sectional area and a material-specific factor. Real tests are higher because heat transfers to the rest of the element and the filler. For a realistic melting estimate, Eaton recommends intersecting the fuse time-current curve with the cumulative RMS profile of the actual prospective waveform and calculating $I^2t = I_RMS^2t$ at the intersection; Eaton notes that this estimate is normally slightly above the measured value.

For duties below 3 ms, Eaton considers the faster current rise less severe for the fuse and does not require additional review solely on that basis, including capacitor- and BESS-fed applications. In the system model, the actual waveform remains necessary to determine melting, selectivity and stress on adjacent components. The check must also retain maximum recovery voltage, the rating-specific minimum breaking current, maximum interrupting current and any sustained or delayed contribution from other sources.

No technical interpretation is assigned here to the UL report statements concerning current limitation or let-through values. Eaton has confirmed that UL witnessed the tests and received the results, and intends to address the wording in a future UL project. This case study therefore uses the datasheet and proving reports as its technical evidence for measured current limitation. UL recognition remains a separate conformity matter and should be applied according to the current UL file when UL approval is required.

The datasheet publishes a minimum breaking current for each rating. The 1,400 A link is listed at 11.1 kA, while the 350 A link is listed at 1.4 kA [8]. Eaton explains that the 800% value in the UL file represents the highest-rated link in the homogeneous range unless each rating is individually supported. Engineering studies should therefore use the rating-specific datasheet minimum; the applicable UL conditions should be checked separately for installations requiring UL recognition.

The available Eaton evidence is sufficient to conclude this case study at the present model-fidelity level. A Level 1 melting model can be parameterised from the rating-specific cold minimum and time-current curve. A Level 2 model can use the manufacturer-supplied 3 ms characteristic for rating-specific peak let-through and the measured 3 ms and 10 ms results for duty-specific energy, voltage and timing checks. A general Level 3 dynamic arc model is not justified because the available data do not identify an arc law and the residual tail-current duration cannot be predicted reliably. Where detailed extinction behaviour is decisive, the study should use a manufacturer-validated model or project-specific test evidence.

7 Discrimination and local equipment protection

A local fuse recommended or mandated by a drive or converter supplier should still be assessed in the complete DC network. The supplier recommendation may address protection of the local power stage under a defined source impedance but not the energy available from a common DC bus, adjacent capacitors, batteries or another feeder.

The familiar fuse-to-fuse criterion remains a useful starting point: the downstream fuse's maximum total-clearing I²t should remain below the upstream fuse's minimum pre-arcing I²t for the relevant condition. In a DC microgrid, both quantities must be applicable to the actual voltage, initial loading and waveform. If the downstream clearing interval changes the upstream current through network commutation, both fuse states must be solved in the same time-domain model.

$$(I^2t)_{downstream\ total\ maximum} < (I^2t)_{upstream\ pre\text{-}arcing\ minimum}$$

This inequality is necessary for many coordination claims but is not universally sufficient. Peak let-through current, arc voltage, minimum breaking current, branch current transfer and protection action

by controlled converters can alter the outcome. Selectivity should be reported by fault location and operating state rather than as a single property of two catalogue fuse ratings.

8 Assembly withstand and the depth of clearing analysis

The passive distribution structure is verified by withstand, not by breaking capacity. If the switchgear assembly has an independent DC short-time and peak withstand rating that covers the prospective fault duty, its structural survival does not depend on current limitation by the fuse. If the assembly rating is conditional on a specified protective device, peak let-through and clearing I^2t form part of the withstand evidence and the clearing model becomes decisive [5].

8.1 Utilisation factors

Three screening factors make this distinction explicit. The ratings used must apply to DC and to the relevant duration and test basis:

$$K_I = I_PSC / I_cw$$

$$K_pk = i_peak\ actual / I_pk$$

$$K_th = \int i^2(t)dt / (I_cw^2\, t_rated)$$

K_I is a current-headroom indicator; K_pk and K_th address the mechanical and thermal duties more directly. These ratios do not replace the assembly's verified rating conditions, and I^2t scaling should not be extrapolated outside the applicable time range or used to convert an AC rating into a DC rating.

8.2 Interpretation of the observed 25 percent margin

Repeated project experience indicates that classification reviewers tend to request less detailed clearing evidence when the prospective short-circuit current is comfortably below an independently verified assembly withstand rating. Approximately 25% rating headroom has been encountered as a region in which the clearing interval may cease to be decisive for the switchboard structure. No universal IEC or marine-class rule establishing this numerical threshold has been identified.

If I_cw = 1.25 I_PSC, then K_I = 0.8. With comparable geometry and waveform, electrodynamic force varies approximately with current squared, so the corresponding force utilisation is about:

$$K_F \approx K_I^2 = 0.8^2 = 0.64$$

This explains why 25% current-rating headroom can feel materially larger to a reviewer: the calculated fault corresponds to about 64% of the force associated with the rated current. It does not create a physical discontinuity at 25%, and it does not prove thermal withstand, DC interruption, selectivity or component survival.

Withstand rating above PSC	K_I	Approximate I^2 stress utilisation
5%	0.952	0.907
10%	0.909	0.826
20%	0.833	0.694
25%	0.800	0.640
30%	0.769	0.592

8.3 Correct decision statement

The defensible formulation is not that clearing time can be skipped below a chosen L/R or above a chosen withstand margin. It is:

For fast DC fault studies, deriving arcing or clearing time from conventional AC characteristics is often neither necessary nor justified. Pre-arcing behaviour should be evaluated from the actual simulated current waveform. Post-melting behaviour should be represented only to the fidelity required by the verification objective and should otherwise be bounded or validated by the fuse manufacturer.

9 Model selection and validation workflow

Step	Engineering question	Required action
1	What is being verified	State whether the objective is fuse operation, semiconductor protection, selectivity, cable protection, assembly withstand, interruption or transient voltage
2	What current reaches each fuse	Simulate all credible sources, operating modes, fault locations and protection actions
3	Does the fuse melt	Integrate actual $i^2(t)$; use the cold minimum as a conservative bound and the applicable time-current curve or calibrated thermal model for realistic melting
4	Can the exact arcing interval change the conclusion	If no, use Level 1 or conservative Level 2; if yes, use Level 3
5	Is DC interruption already demonstrated	Verify exact part number against maximum recovery voltage, L/R or actual waveform, current range and topology
6	Does assembly survival depend on fuse limitation	Compare DC-valid Icw, Ipk and conditional rating data with actual peak and thermal duty
7	Is discrimination preserved	Check downstream total-clearing stress against upstream pre-arcing threshold in the coupled network model
8	Is the evidence auditable	Archive model version, parameters, waveforms, solver settings, tolerance cases and manufacturer correspondence

9.1 Minimum validation matrix

- Integrator verification against an analytic RL case and an independent numerical integration of exported waveform data.
- Time-step convergence for pre-arcing time, peak current, total I^2t and peak fuse voltage.
- Cold and normally preloaded fuse states, plus relevant ambient and mounting conditions.
- Maximum and minimum prospective fault-current cases, because interruption can be difficult at both boundaries for different reasons.
- Nominal 1,000 V DC baseline cases and, where applicable, cases extending toward the 1,500 V DC equipment class, including the maximum credible operating and recovery voltage across each fuse.

- Tolerance study for fuse I^2t, source impedance, capacitor ESR and ESL, cable or bus inductance, and parallel-path resistance.
- Comparison with manufacturer clearing I^2t, cut-off current and peak arc-voltage data wherever those data apply.

10 Manufacturer data request

When the available catalogue information does not cover the case, the most useful manufacturer submission is the simulated waveform and network duty rather than a single prospective current. The submission should contain:

- exact fuse part number, quantity and series or parallel arrangement;
- nominal bus voltage, maximum operating voltage and maximum recovery voltage across each fuse, with the meaning of any stated 1,500 V DC system or equipment rating made explicit;
- current waveform through each fuse from fault inception until the end of the simulated interval, preferably in CSV format;
- prospective current without fuse limitation, source contributions and fault location;
- equivalent circuit parameters where meaningful, including resistance, inductance and any stated L/R, while noting where no single L/R exists;
- capacitor values, ESR and ESL, battery or rectifier characteristics and converter current-limiting actions;
- initial fuse current, ambient, conductor size, cooling and mounting;
- required outputs: pre-arcing time, clearing time or bounds, peak let-through, total I^2t, peak arc voltage, interruption confirmation and acceptable tolerance;
- the protection or compliance decision that depends on the result.

Manufacturer recalculation is particularly appropriate when the actual waveform or source persistence is outside the demonstrated product envelope, when the system operates near the fuse's voltage or current limits, when series or parallel operation is proposed, or when assembly withstand depends on fuse current limitation. A shorter time constant alone is not a referral trigger where the manufacturer has explicitly confirmed that the selected fuse covers that duty.

11 Limitations and failure modes

Potential error	Consequence	Mitigation
Using nominal rather than recovery voltage	Underestimates arcing duty and peak fuse voltage	Solve voltage across the fuse for every fault topology
Treating 10 ms as a fuse constant	Applies an invalid correction to low-L/R networks	Keep circuit and fuse parameters separate
Using total I^2t as the melting threshold	Delays melting and corrupts coordination	Use the cold pre-arcing I^2t only as a conservative bound; use the time-current curve or a calibrated thermal model for realistic melting
Ideal opening at pre-arcing	Suppresses arc voltage and may misstate let-through current	Use only when post-melting behaviour is proven non-decisive

Potential error	Consequence	Mitigation
Unvalidated detailed arc model	Produces persuasive but non-traceable results	Calibrate to manufacturer or test data and restrict its validity envelope
Ignoring low-current interruption	An aR fuse may melt yet fail to interrupt safely	Check minimum breaking current and backup protection
Equal sharing in series or parallel	Understates individual fuse duty	Use individual models and tolerance cases
Single-source fault model	Misses multi-stage or reverse contributions	Retain source-specific branches and controls
Comparing DC duty with an AC-only assembly rating	Creates an unsupported withstand claim	Obtain a DC-valid verified rating or agreed equivalence

12 Reusable technical conclusion

High-speed aR fuse modelling in a maritime DC microgrid should begin with the actual time-domain current through the fuse, not with an imposed AC-equivalent or triangular waveform. For the pre-arcing interval, an I^2t or thermal-state model can be made traceable and robust. After melting, fuse behaviour is governed by a manufacturer-specific nonlinear arc interacting with the DC source and stored network energy; catalogue data normally do not define a unique electrical equivalent.

For nominal 1,000 V DC systems, and for emerging applications extending toward the 1,500 V DC class, a typical effective fault time constant below 2 to 3 ms can reduce inductive interruption energy while increasing early current rise. It does not remove the need to establish DC interruption capability at the maximum credible recovery voltage and at both the minimum and maximum relevant fault currents.

The required model fidelity should be set by the sensitivity of the engineering conclusion to the arcing interval. Where independently verified DC assembly withstand comfortably exceeds the prospective duty, detailed clearing behaviour may be non-decisive for the busbar and enclosure verification. Where selectivity, semiconductor survival, cable protection, transient voltage, conditional assembly withstand or interruption success depends on clearing, manufacturer-validated dynamic behaviour or conservative verified bounds are required. An observed 25% withstand-rating headroom may be documented as project experience corresponding to $K_I = 0.8$, but not as a universal class threshold.

Use and limitations

This white paper presents an engineering methodology and does not constitute product approval, fuse selection confirmation or evidence of compliance for a specific installation. Fuse suitability and DC interruption capability remain dependent on the exact part number, applied recovery voltage, prospective current, circuit time constant or actual waveform, minimum breaking current, initial loading, mounting conditions and system topology. Manufacturer confirmation, applicable test evidence and the requirements of the relevant flag administration and classification society take precedence where they define more restrictive conditions. Any simulation model derived from this methodology should be validated for its stated operating envelope before it is used for equipment certification or safety-critical design decisions.

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Standards should be applied in the edition required by the contract, flag administration and classification society. The references above establish scope and engineering context; they do not substitute for access to the normative clauses or product-specific manufacturer confirmation.