IXYS
INTEGRATED CIRCUITS DIVISION

IXD_609
9-Ampere Low-Side Ultrafast MOSFET Drivers

Features

- 9A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10μA Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver

Description

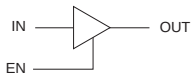
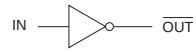
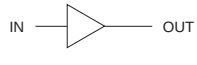
The IXDD609/IXDI609/IXDN609 high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. The IXD_609 high-current output can source and sink 9A of peak current while producing voltage rise and fall times of less than 25ns. The input is CMOS compatible, and is virtually immune to latch up. Proprietary circuitry eliminates cross-conduction and current "shoot-through." Low propagation delay and fast, matched rise and fall times make the IXD_609 family ideal for high-frequency and high-power applications.

The IXDD609 is configured as a non-inverting driver with an enable, the IXDN609 is configured as a non-inverting driver, and the IXDI609 is configured as an inverting driver.

The IXD_609 family is available in a standard 8-pin DIP (PI); an 8-pin SOIC (SIA); an 8-pin Power SOIC with an exposed metal back (SI); an 8-pin DFN (D2); a 5-pin TO-263 (YI); and a 5-pin TO-220 (CI).

Pb RoHS e3

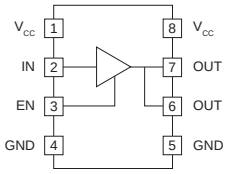
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD609D2TR		8-Pin DFN	Tape & Reel	2000
IXDD609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDD609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDD609SIA		8-Pin SOIC	Tube	100
IXDD609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDD609PI		8-Pin DIP	Tube	50
IXDD609CI		5-Pin TO-220	Tube	50
IXDD609YI		5-Pin TO-263	Tube	50
IXDI609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDI609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDI609SIA		8-Pin SOIC	Tube	100
IXDI609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDI609PI		8-Pin DIP	Tube	50
IXDI609CI		5-Pin TO-220	Tube	50
IXDI609YI		5-Pin TO-263	Tube	50
IXDN609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDN609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDN609SIA		8-Pin SOIC	Tube	100
IXDN609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDN609PI		8-Pin DIP	Tube	50
IXDN609CI		5-Pin TO-220	Tube	50
IXDN609YI		5-Pin TO-263	Tube	50

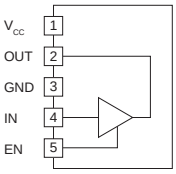
1 Specifications

1.1 Pin Configurations

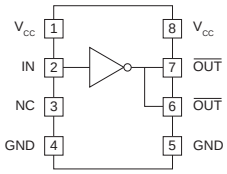
IXDD609 D2 / PI / SI / SIA



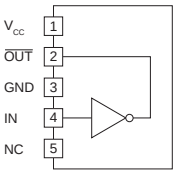
IXDD609 CI / YI



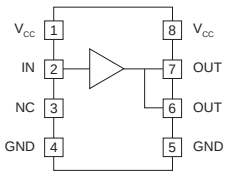
IXDI609 PI / SI / SIA



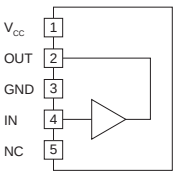
IXDI609 CI / YI



IXDN609 PI / SI / SIA



IXDN609 CI / YI



1.2 Pin Definitions

Pin Name	Description
IN	Logic Input
EN	Output Enable - Drive pin low to disable output, and force output to a high impedance state
OUT	Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
$\overline{OUT}$	Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	Not connected

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	40	V
Input Voltage	V_{IN}, V_{EN}	-5	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±9	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Range	Units
Supply Voltage	V_{CC}	4.5 to 35	V
Operating Temperature Range	T_A	-40 to +125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.0	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	-	±10	µA
EN Input Voltage, High	IXDD609 only	V_{ENH}	2/3V_{CC}	-	-	V
EN Input Voltage, Low	IXDD609 only	V_{ENL}	-	-	1/3V_{CC}	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	22	35	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	15	25	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	40	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	42	60	
Enable to Output-High Delay Time (IXDD609 Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609 Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	<1	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	<1	10	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V unless otherwise noted.

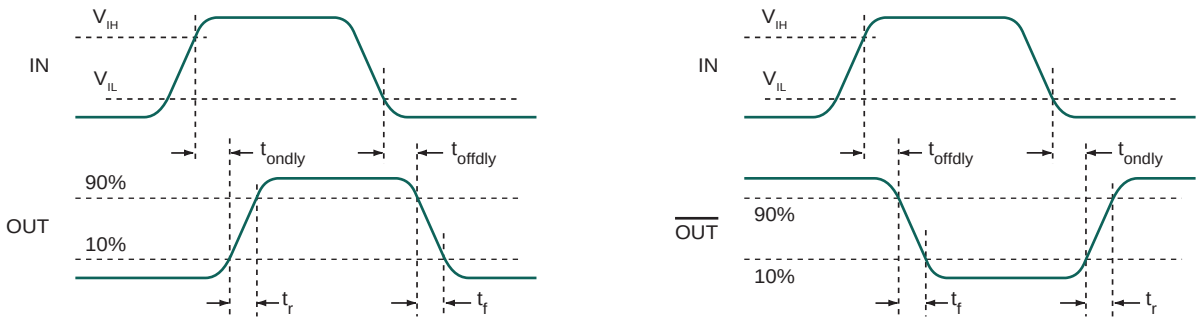
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.3	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	0.65	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	±10	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	2	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	1.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	±1	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	40	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	30	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	75	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	75	
Enable to Output-High Delay Time	IXDD609 only, V_{CC}=18V	t_{ENOH}	-	75	
Disable to High Impedance State Delay Time	IXDD609 only, V_{CC}=18V	t_{DOLD}	-	75	
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	2.5	mA
	V_{CC}=18V, V_{IN}=0V		-	150	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	150	

1.7 Thermal Characteristics

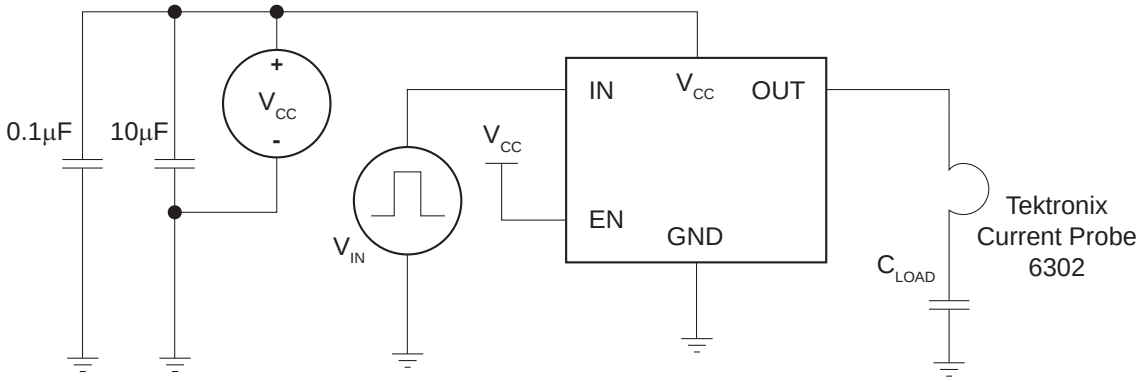
Package	Parameter	Symbol	Rating	Units
D2 (8-Pin DFN)	Thermal Impedance, Junction-to-Ambient	θ_{JA}	35	°C/W
CI (5-Pin TO-220)			36	
PI (8-Pin DIP)			125	
SI (8-Pin Power SOIC)			85	
SIA (8-Pin SOIC)			120	
YI (5-Pin TO-263)			46	
CI (5-Pin TO-220)	Thermal Impedance, Junction-to-Case	θ_{JC}	3	°C/W
SI (8-Pin Power SOIC)			10	
YI (5-Pin TO-263)			2	

2 IXD_609 Performance

2.1 Timing Diagrams

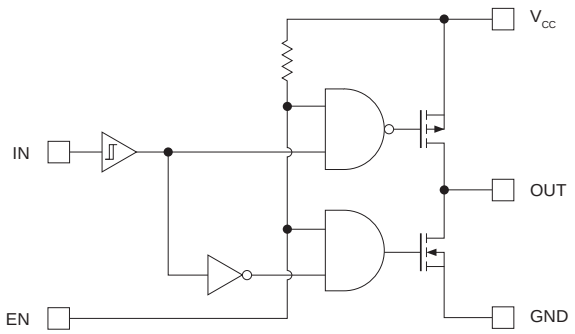


2.2 Characteristics Test Diagram



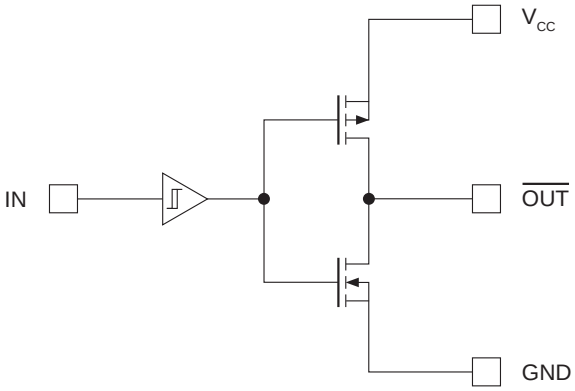
3 Block Diagrams & Truth Tables

3.1 IXDD609



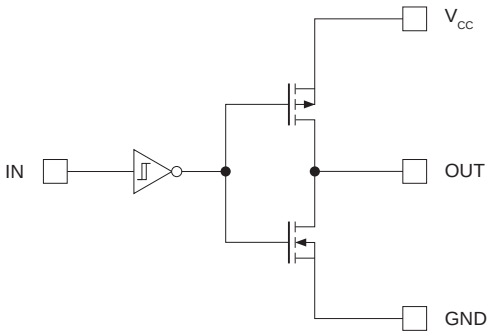
IN	EN	OUT
0	1 or open	0
1	1 or open	1
x	0	Z

3.2 IXDI609



IN	$\overline{OUT}$
0	1
1	0

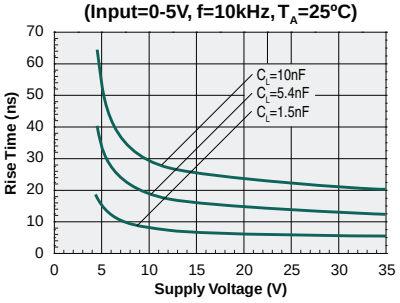
3.3 IXDN609



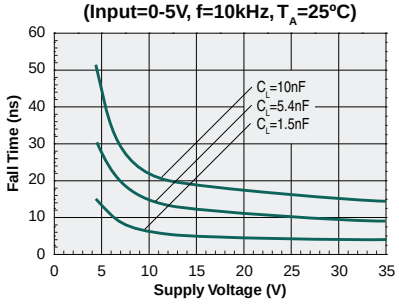
IN	OUT
0	0
1	1

4 Typical Performance Characteristics

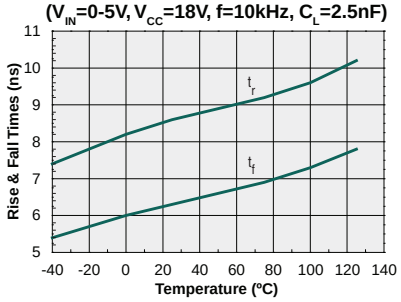
Rise Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



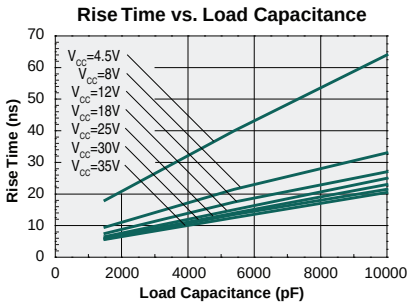
Fall Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



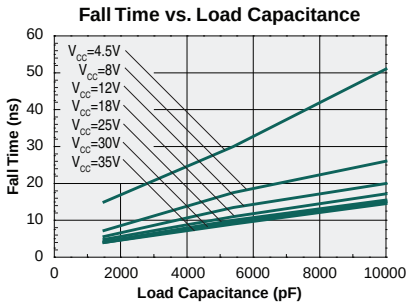
Rise and Fall Times vs. Temperature (V_{IN}=0-5V, V_{CC}=18V, f=10kHz, C_L=2.5nF)



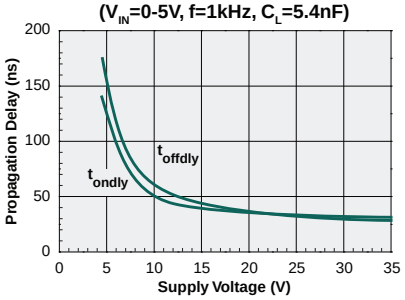
Rise Time vs. Load Capacitance



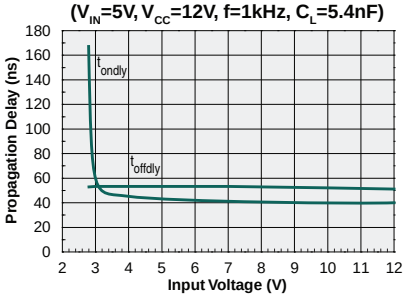
Fall Time vs. Load Capacitance



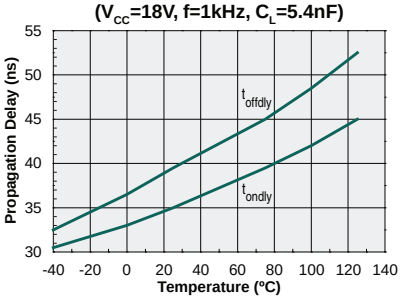
Propagation Delay vs. Supply Voltage (V_{IN}=0-5V, f=1kHz, C_L=5.4nF)



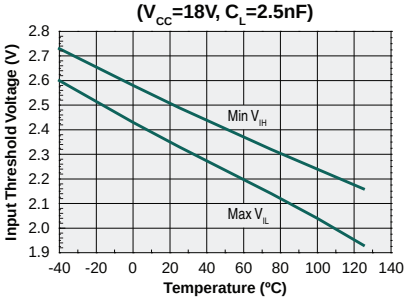
Propagation Delay vs. Input Voltage (V_{IN}=5V, V_{CC}=12V, f=1kHz, C_L=5.4nF)



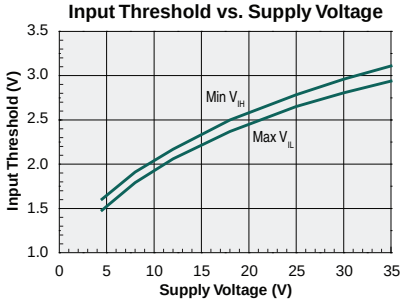
Propagation Delay vs. Temperature (V_{CC}=18V, f=1kHz, C_L=5.4nF)



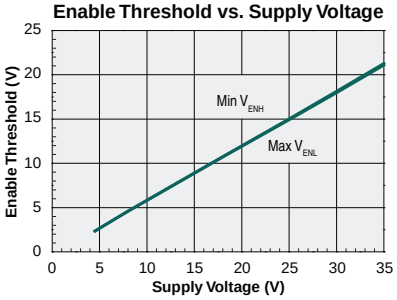
Input Threshold Voltage vs. Temperature (V_{CC}=18V, C_L=2.5nF)



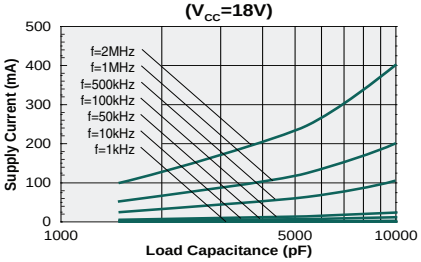
Input Threshold vs. Supply Voltage



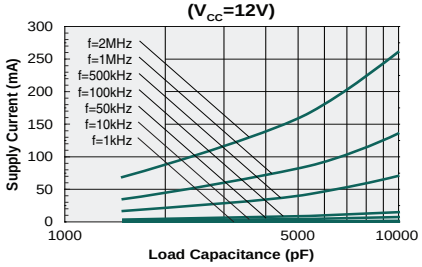
Enable Threshold vs. Supply Voltage



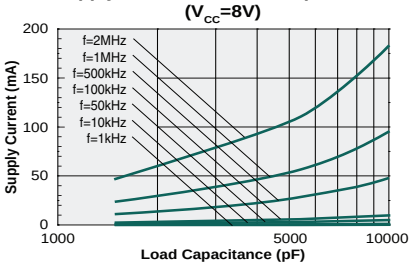
Supply Current vs. Load Capacitance (V_{CC}=18V)



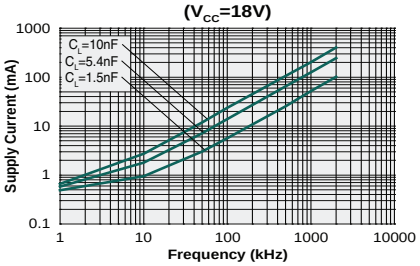
Supply Current vs. Load Capacitance (V_{CC}=12V)



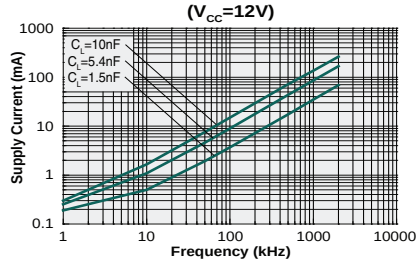
Supply Current vs. Load Capacitance (V_{CC}=8V)



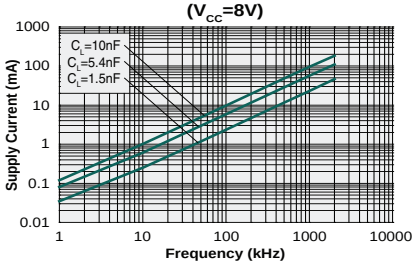
Supply Current vs. Frequency (V_{CC}=18V)



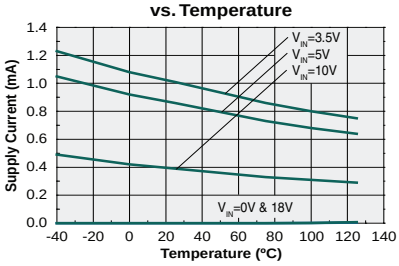
Supply Current vs. Frequency (V_{CC}=12V)



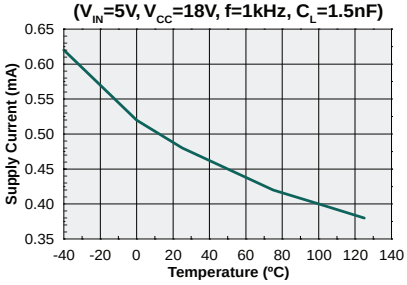
Supply Current vs. Frequency (V_{CC}=8V)



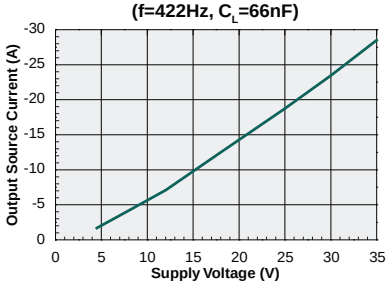
Quiescent Supply Current vs. Temperature



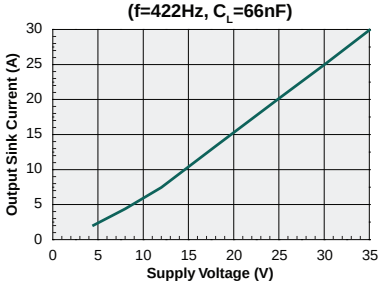
Dynamic Supply Current vs. Temperature (V_{IN}=5V, V_{CC}=18V, f=1kHz, C_L=1.5nF)



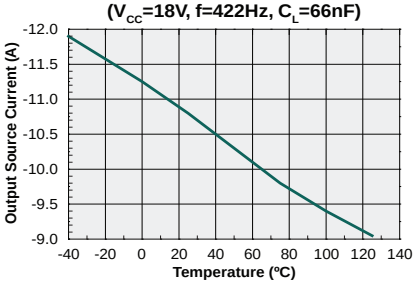
Output Source Current vs. Supply Voltage (f=422Hz, C_L=66nF)



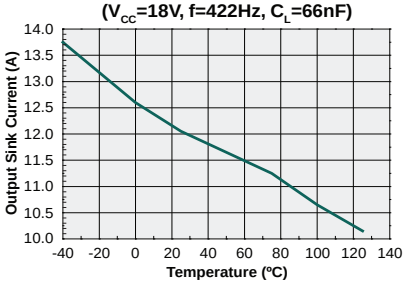
Output Sink Current vs. Supply Voltage (f=422Hz, C_L=66nF)



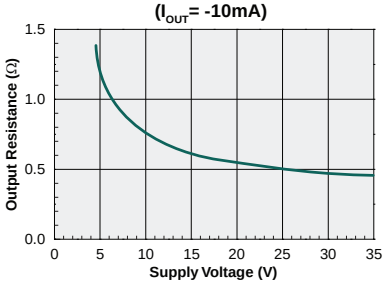
Output Source Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



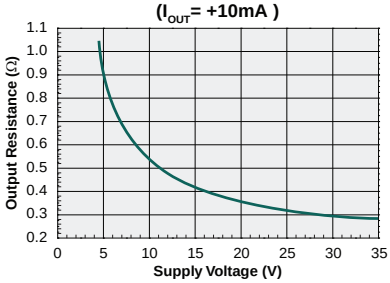
Output Sink Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



High State Output Resistance vs. Supply Voltage (I_{OUT}= -10mA)



Low State Output Resistance vs. Supply Voltage (I_{OUT}= +10mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD_609 All Versions except IXD_609YI	MSL 1
IXD_609YI	MSL 3

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

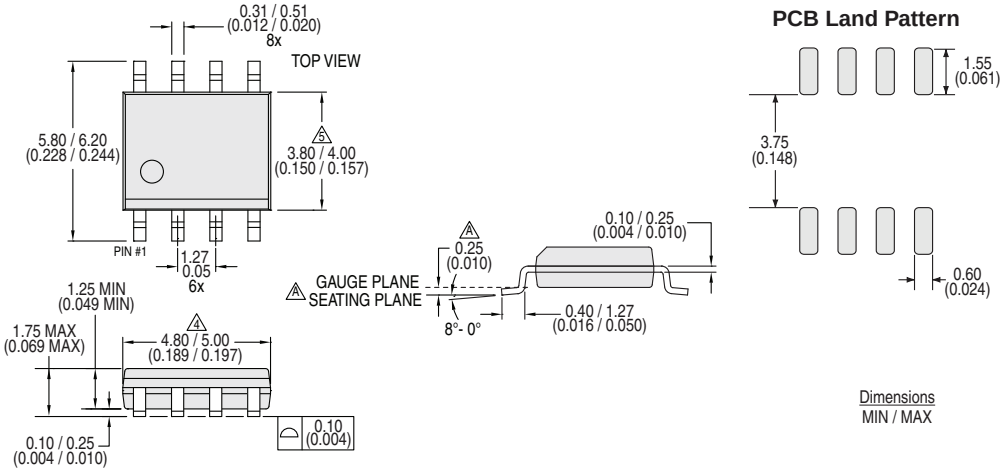
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Maximum Cycles
IXD_609CI	245°C for 30 seconds	30 seconds	1
IXD_609YI	245°C for 30 seconds	30 seconds	3
IXD_609PI	250°C for 30 seconds	30 seconds	3
IXD_609SI / IXD_609SIA / IXD_609D2	260°C for 30 seconds	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

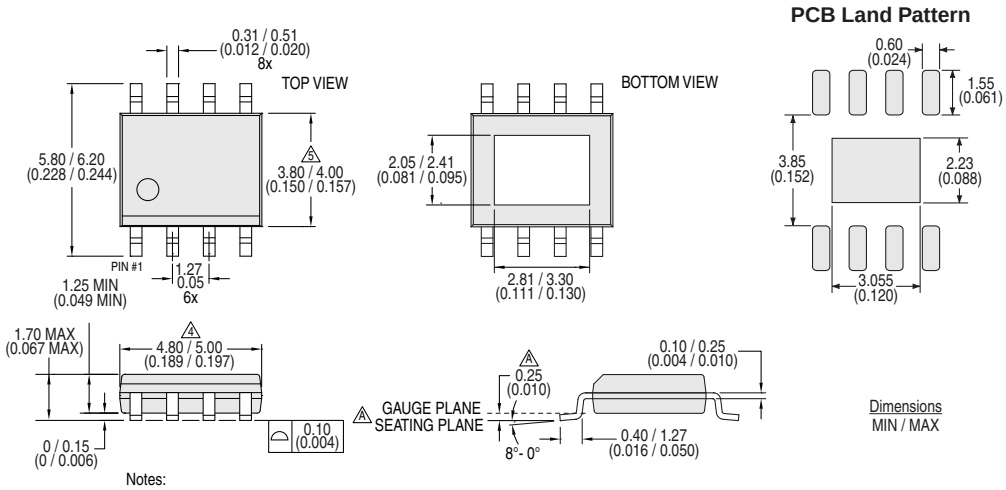
5.5 Mechanical Dimensions

5.5.1 SIA (8-Pin SOIC)



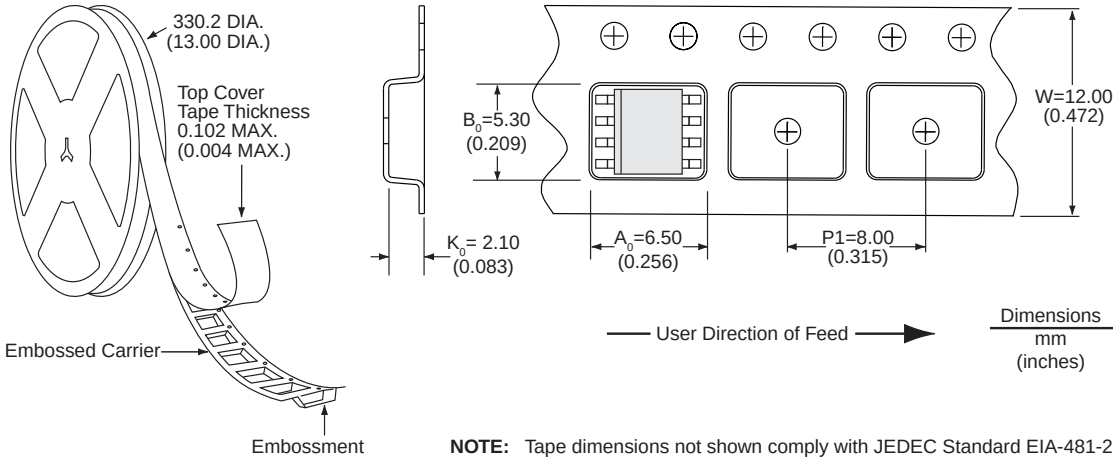
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

5.5.2 SI (8-Pin Power SOIC with Exposed Metal Back)



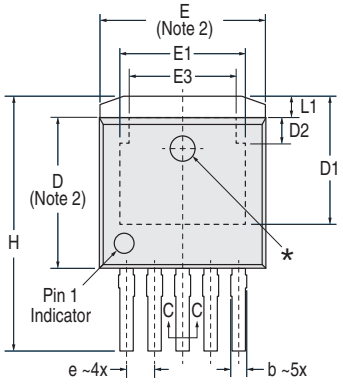
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.5.3 Tape & Reel Information for SI and SIA Packages



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

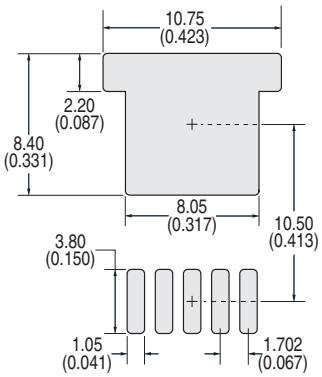
5.5.4 YI (5-Pin TO-263)

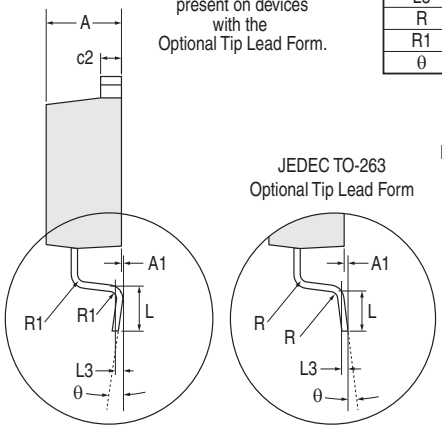


*Circular feature will be present on devices with the Optional Tip Lead Form.

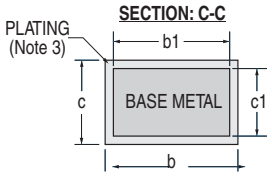
SYMBOL	MM		INCH	
	MIN	MAX	MIN	MAX
A	4.064	4.826	0.160	0.190
A1	0.000	0.254	0.000	0.010
b	0.508	0.991	0.020	0.039
b1	0.508	0.889	0.020	0.035
c	0.381	0.737	0.015	0.029
c1	0.381	0.584	0.015	0.023
c2	1.143	1.651	0.045	0.065
D	8.382	9.652	0.330	0.380
D1	6.858	7.700	0.270	0.303
D2	1.358	1.562	0.053	0.062
E	9.652	10.668	0.380	0.420
E1	6.223	8.000	0.245	0.315
E3	5.092	6.869	0.200	0.270
e	1.702 BSC		0.067 BSC	
H	14.605	15.875	0.575	0.625
L	1.778	2.794	0.070	0.110
L1	1.000	1.676	0.039	0.066
L3	0.254 BSC		0.010 BSC	
R	0.460 TYP		0.018 TYP	
R1	0.506 TYP		0.02 TYP	
θ	-	8°	-	8°

Recommended PCB Pattern



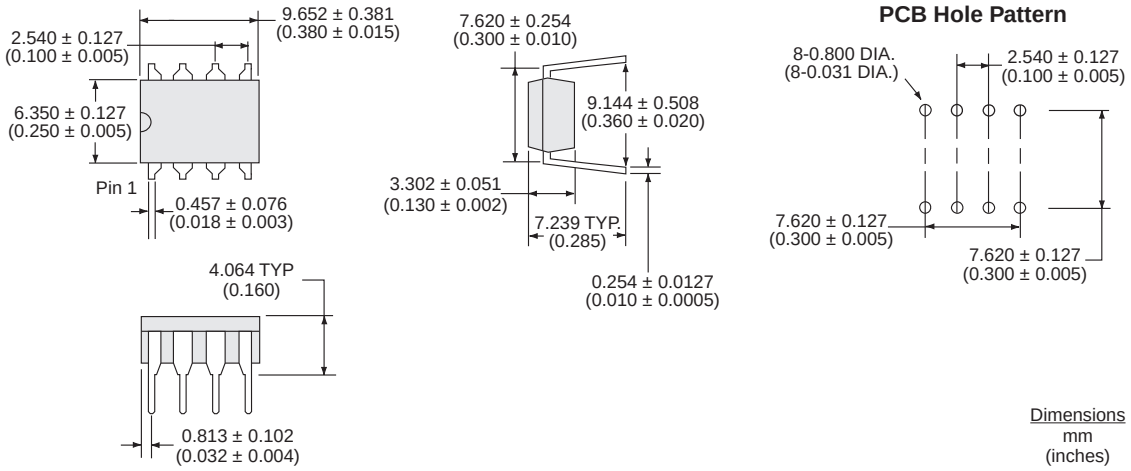


SECTION: C-C

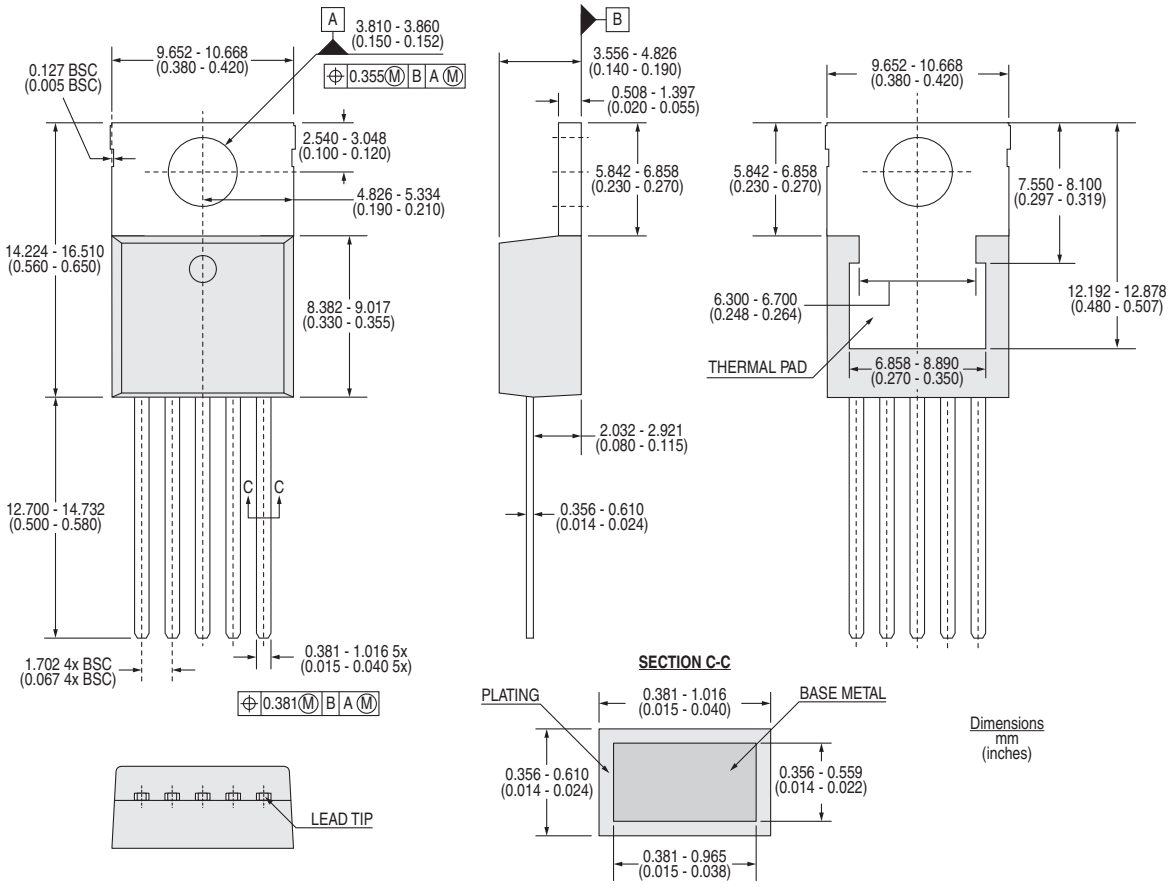


NOTES:
1. Reference JEDEC TO-263 Type "BA".
2. Dimension does not include mold flash; mold flash shall not exceed 0.127mm (0.005 inch) per side.
3. Minimum plating: 1000 microinches.
4. Controlling dimension: millimeters.

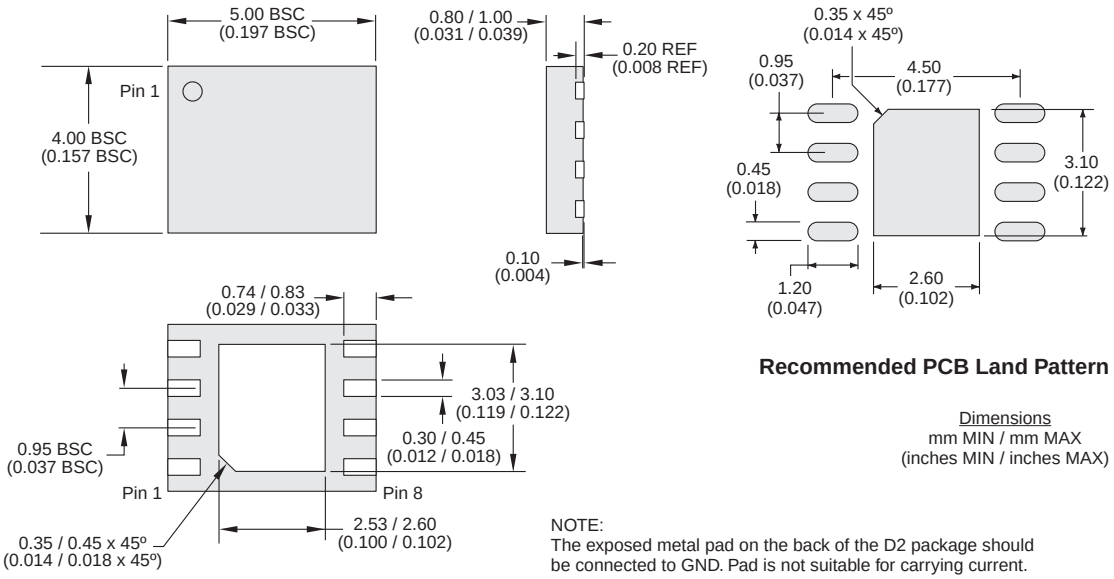
5.5.5 PI (8-Pin DIP)



5.5.6 CI (5-Pin TO-220)



5.5.7 D2 (8-Pin DFN)

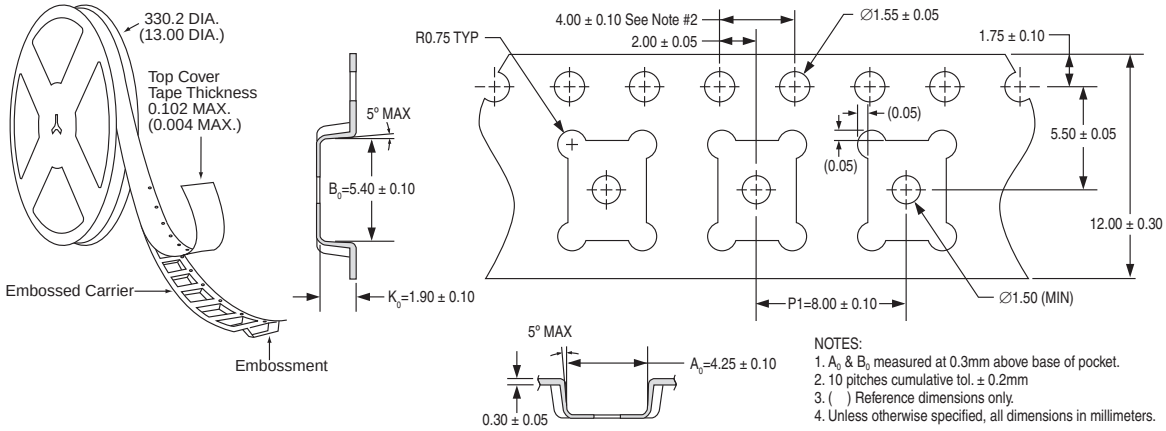


Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE:
The exposed metal pad on the back of the D2 package should be connected to GND. Pad is not suitable for carrying current.

5.5.8 Tape & Reel Information for D2 Package



NOTES:
1. A_0 & B_0 measured at 0.3mm above base of pocket.
2. 10 pitches cumulative tol. ± 0.2mm
3. ( ) Reference dimensions only.
4. Unless otherwise specified, all dimensions in millimeters.

For additional information please visit our website at: www.ixysic.com

Specification: DS-IXD_609-R09

10/25/2017

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

IXYS
A Littelfuse Technology

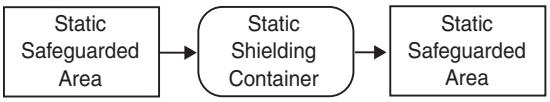
Handling MOS Devices

Static Discharge

Metal Oxide Semiconductor (MOS) devices have gained broad acceptance in telecommunications. This includes use of n-channel (NMOS) transistors, p-channel (PMOS) transistors, or both (complementary or CMOS) transistors. Most IXYS IC Division devices are fabricated using CMOS techniques, but some use PMOS. In any case, MOS circuits require special attention in design and handling because of their susceptibility to damage through buildup of static charges and the currents that occur during discharge.

Whether alone or mounted in circuit boards, MOS ICs are subject to buildup of static charges and damaging discharges. Voltage of several hundred volts can affect these devices, while one or two thousand volts will certainly cause harm. Five hundred volts can easily be generated by a person walking around or moving in a chair, and thousands of volts can be generated by the simple act of pulling out and tearing off a piece of transparent tape. Under these circumstances, precautions must be taken to limit the potential for damage to costly IC devices. MOS ICs should be handled in static-protected or “safeguarded” areas. Such areas include ionized air flow over nonconducting surfaces. When not in these areas, ICs should be kept in static shielded containers. ICs must be handled in safeguarded areas (receiving inspection, stores, assembly, and test) and, when moved from area to area, should be protected by shielded containers. Failure to implement procedures of this sort or relaxation of procedures can result in loss of valuable parts, increased production fallout, and higher repair costs.

Static Transmission



CMOS Latchup

Though all ICs are subject to static discharge damage, CMOS ICs can experience another kind of damaging event known as “latchup” or “SCR.” In this case, large currents can follow-through the part from the power supply, damaging transistors and interconnections. This occurs when currents are injected into the chip where they were not intended, usually through an I/O pin which has been driven to a voltage outside the supply range by some external device or event. This phenomenon is equivalent to four-layer conduction as used in SCRs, where a semiconductor device is “turned on” by injecting a current into a trigger layer. The device stays “on” until voltage is removed. This is useful in SCR control circuits, but in the case of CMOS ICs they may (1) recover completely after power has been cycled, (2) recover, but act very strangely, or (3) blow up completely. Causes can be inadequate power supply filtering, transient protection, or coincidences of PWB track layout. Static discharge may also trigger latchup.

For additional information please visit our website at: www.ixysic.com

Specification: AN-130-R04

4/10/2014

IXYS
INTEGRATED CIRCUITS DIVISION

IXD_609
9-Ampere Low-Side Ultrafast MOSFET Drivers

Features

- 9A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10μA Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver

Description

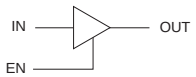
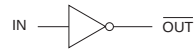
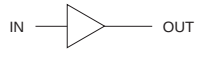
The IXDD609/IXDI609/IXDN609 high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. The IXD_609 high-current output can source and sink 9A of peak current while producing voltage rise and fall times of less than 25ns. The input is CMOS compatible, and is virtually immune to latch up. Proprietary circuitry eliminates cross-conduction and current "shoot-through." Low propagation delay and fast, matched rise and fall times make the IXD_609 family ideal for high-frequency and high-power applications.

The IXDD609 is configured as a non-inverting driver with an enable, the IXDN609 is configured as a non-inverting driver, and the IXDI609 is configured as an inverting driver.

The IXD_609 family is available in a standard 8-pin DIP (PI); an 8-pin SOIC (SIA); an 8-pin Power SOIC with an exposed metal back (SI); an 8-pin DFN (D2); a 5-pin TO-263 (YI); and a 5-pin TO-220 (CI).

Pb RoHS e3

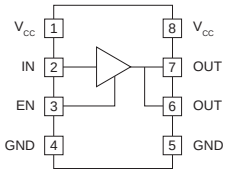
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD609D2TR		8-Pin DFN	Tape & Reel	2000
IXDD609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDD609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDD609SIA		8-Pin SOIC	Tube	100
IXDD609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDD609PI		8-Pin DIP	Tube	50
IXDD609CI		5-Pin TO-220	Tube	50
IXDD609YI		5-Pin TO-263	Tube	50
IXDI609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDI609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDI609SIA		8-Pin SOIC	Tube	100
IXDI609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDI609PI		8-Pin DIP	Tube	50
IXDI609CI		5-Pin TO-220	Tube	50
IXDI609YI		5-Pin TO-263	Tube	50
IXDN609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDN609SITR		8-Pin Power SOIC with Exposed Metal Back	Tape & Reel	2000
IXDN609SIA		8-Pin SOIC	Tube	100
IXDN609SIATR		8-Pin SOIC	Tape & Reel	2000
IXDN609PI		8-Pin DIP	Tube	50
IXDN609CI		5-Pin TO-220	Tube	50
IXDN609YI		5-Pin TO-263	Tube	50

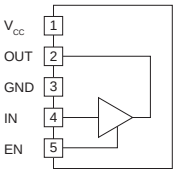
1 Specifications

1.1 Pin Configurations

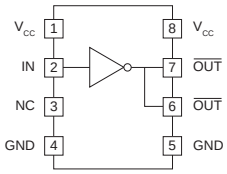
IXDD609 D2 / PI / SI / SIA



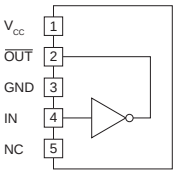
IXDD609 CI / YI



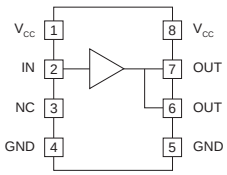
IXDI609 PI / SI / SIA



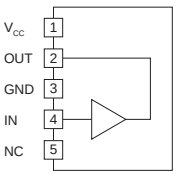
IXDI609 CI / YI



IXDN609 PI / SI / SIA



IXDN609 CI / YI



1.2 Pin Definitions

Pin Name	Description
IN	Logic Input
EN	Output Enable - Drive pin low to disable output, and force output to a high impedance state
OUT	Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
$\overline{OUT}$	Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	Not connected

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	40	V
Input Voltage	V_{IN}, V_{EN}	-5	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±9	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Range	Units
Supply Voltage	V_{CC}	4.5 to 35	V
Operating Temperature Range	T_A	-40 to +125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.0	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	-	±10	µA
EN Input Voltage, High	IXDD609 only	V_{ENH}	2/3V_{CC}	-	-	V
EN Input Voltage, Low	IXDD609 only	V_{ENL}	-	-	1/3V_{CC}	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	22	35	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	15	25	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	40	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	42	60	
Enable to Output-High Delay Time (IXDD609 Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609 Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	<1	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	<1	10	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V unless otherwise noted.

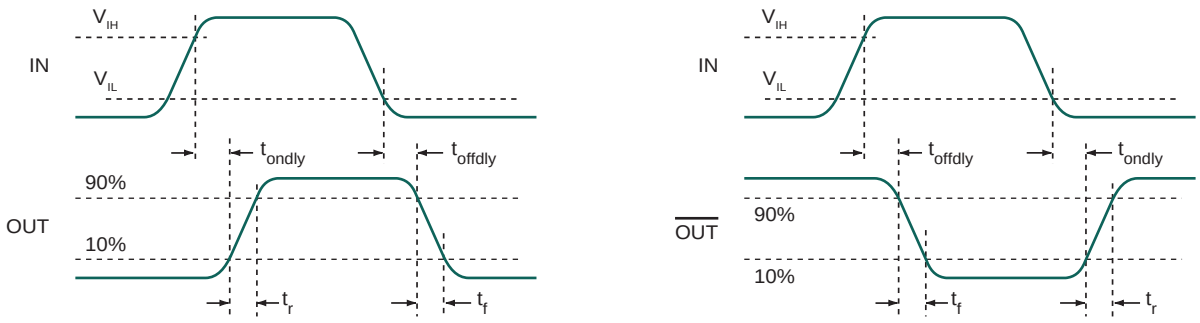
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.3	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	0.65	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	±10	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	2	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	1.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	±1	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	40	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	30	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	75	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	75	
Enable to Output-High Delay Time	IXDD609 only, V_{CC}=18V	t_{ENOH}	-	75	
Disable to High Impedance State Delay Time	IXDD609 only, V_{CC}=18V	t_{DOLD}	-	75	
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	2.5	mA
	V_{CC}=18V, V_{IN}=0V		-	150	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	150	

1.7 Thermal Characteristics

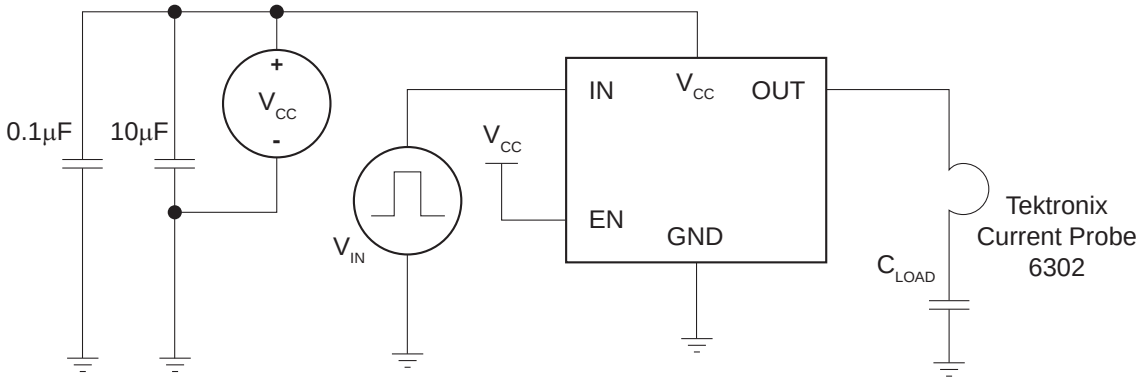
Package	Parameter	Symbol	Rating	Units
D2 (8-Pin DFN)	Thermal Impedance, Junction-to-Ambient	θ_{JA}	35	°C/W
CI (5-Pin TO-220)			36	
PI (8-Pin DIP)			125	
SI (8-Pin Power SOIC)			85	
SIA (8-Pin SOIC)			120	
YI (5-Pin TO-263)			46	
CI (5-Pin TO-220)	Thermal Impedance, Junction-to-Case	θ_{JC}	3	°C/W
SI (8-Pin Power SOIC)			10	
YI (5-Pin TO-263)			2	

2 IXD_609 Performance

2.1 Timing Diagrams

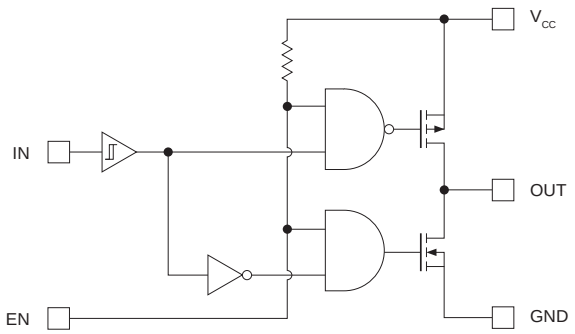


2.2 Characteristics Test Diagram



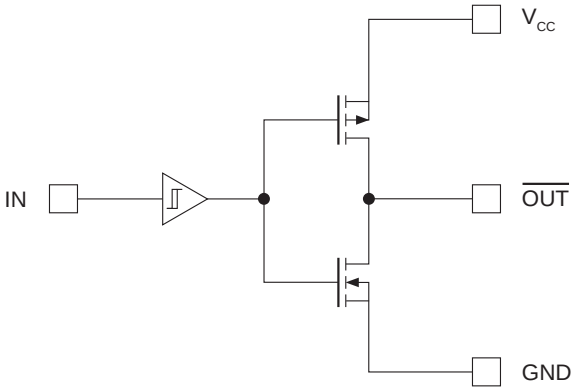
3 Block Diagrams & Truth Tables

3.1 IXDD609



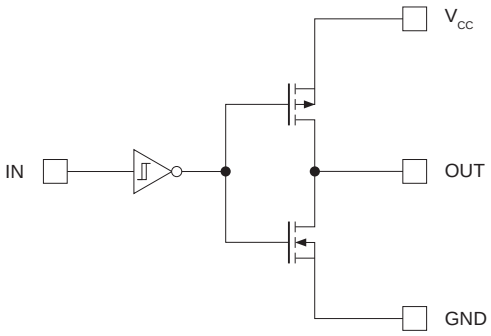
IN	EN	OUT
0	1 or open	0
1	1 or open	1
x	0	Z

3.2 IXDI609



IN	$\overline{OUT}$
0	1
1	0

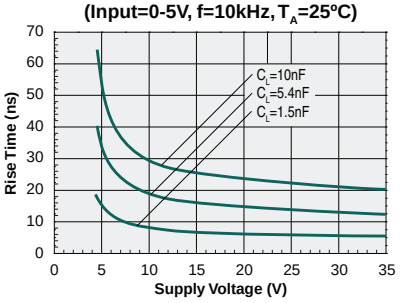
3.3 IXDN609



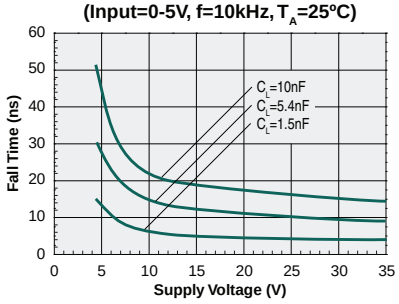
IN	OUT
0	0
1	1

4 Typical Performance Characteristics

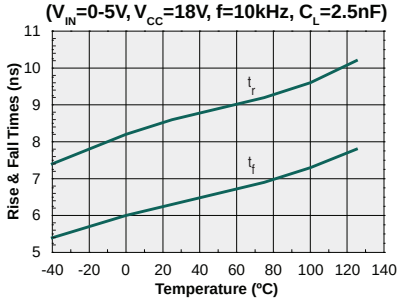
Rise Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



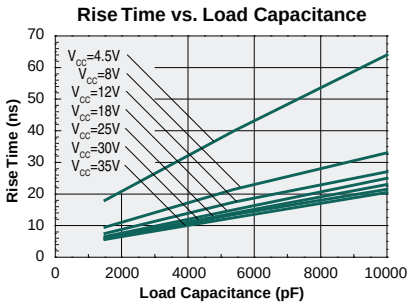
Fall Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



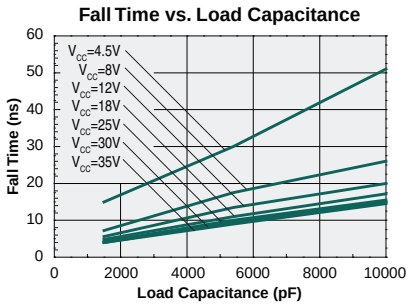
Rise and Fall Times vs. Temperature (V_{IN}=0-5V, V_{CC}=18V, f=10kHz, C_L=2.5nF)



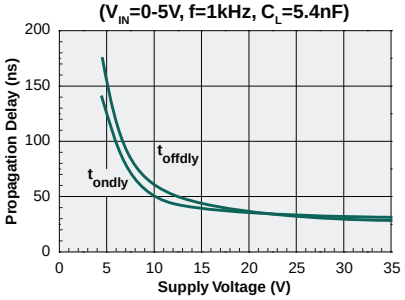
Rise Time vs. Load Capacitance



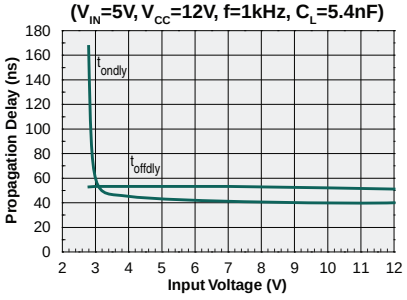
Fall Time vs. Load Capacitance



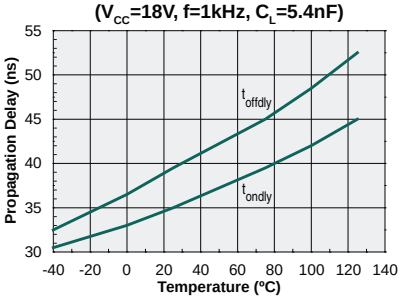
Propagation Delay vs. Supply Voltage (V_{IN}=0-5V, f=1kHz, C_L=5.4nF)



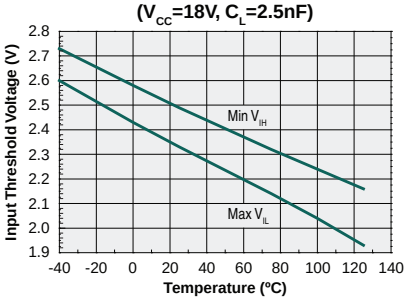
Propagation Delay vs. Input Voltage (V_{IN}=5V, V_{CC}=12V, f=1kHz, C_L=5.4nF)



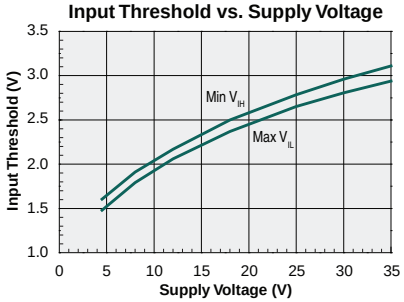
Propagation Delay vs. Temperature (V_{CC}=18V, f=1kHz, C_L=5.4nF)



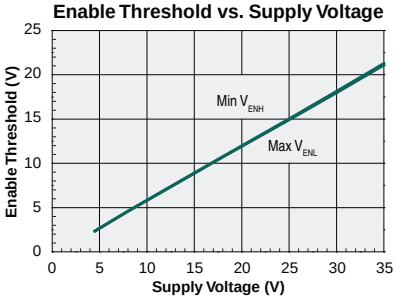
Input Threshold Voltage vs. Temperature (V_{CC}=18V, C_L=2.5nF)



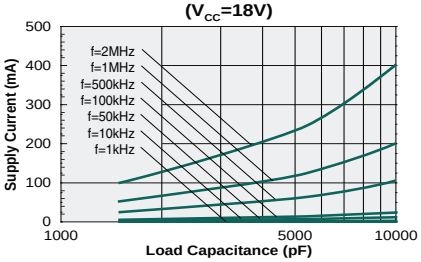
Input Threshold vs. Supply Voltage



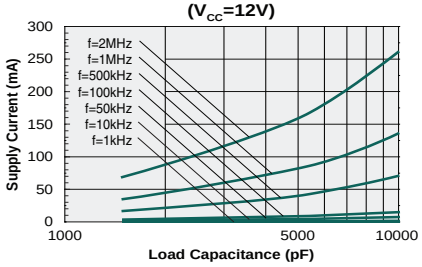
Enable Threshold vs. Supply Voltage



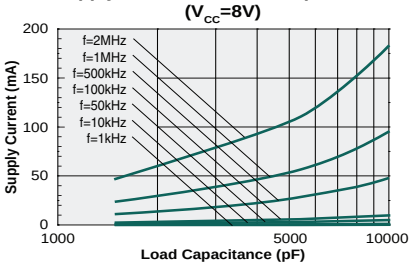
Supply Current vs. Load Capacitance (V_{CC}=18V)



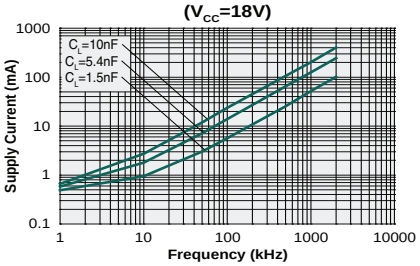
Supply Current vs. Load Capacitance (V_{CC}=12V)



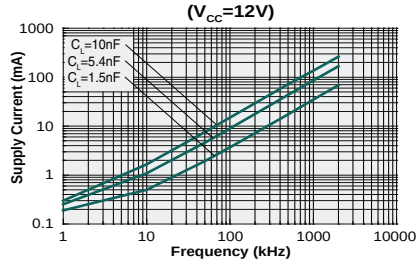
Supply Current vs. Load Capacitance (V_{CC}=8V)



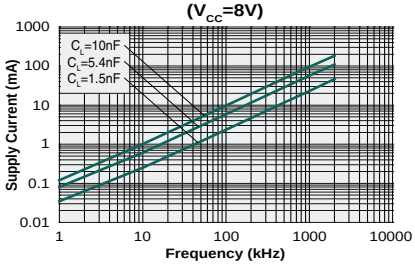
Supply Current vs. Frequency (V_{CC}=18V)



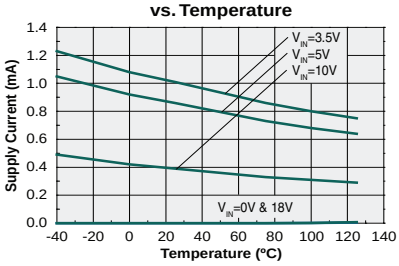
Supply Current vs. Frequency (V_{CC}=12V)



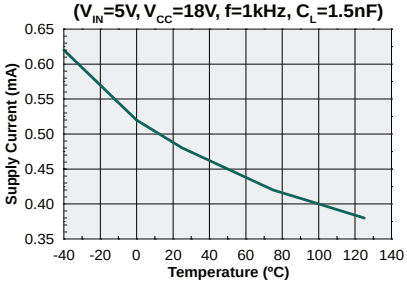
Supply Current vs. Frequency (V_{CC}=8V)



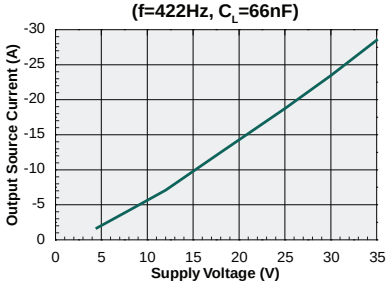
Quiescent Supply Current vs. Temperature



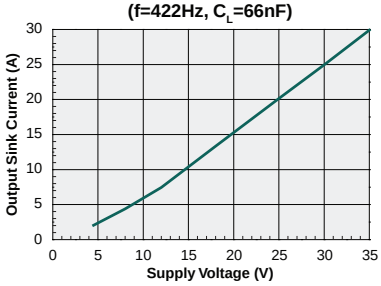
Dynamic Supply Current vs. Temperature (V_{IN}=5V, V_{CC}=18V, f=1kHz, C_L=1.5nF)



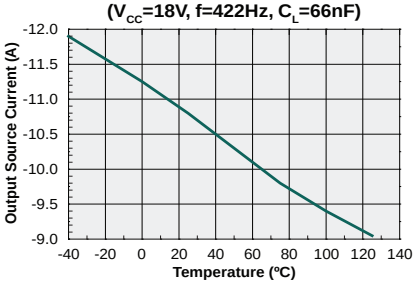
Output Source Current vs. Supply Voltage (f=422Hz, C_L=66nF)



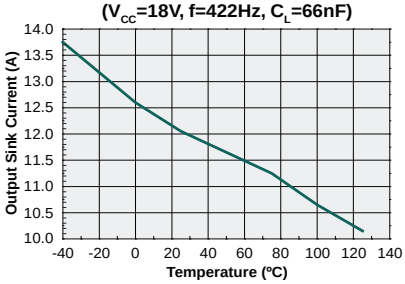
Output Sink Current vs. Supply Voltage (f=422Hz, C_L=66nF)



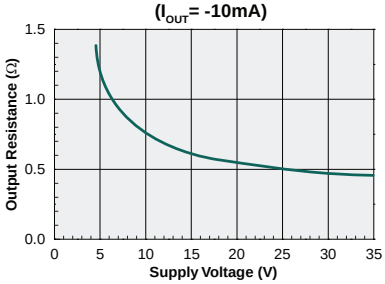
Output Source Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



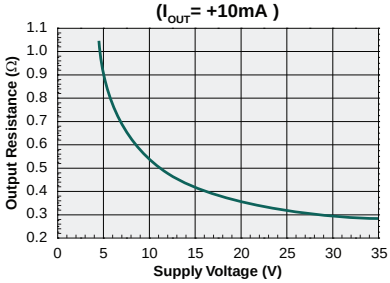
Output Sink Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



High State Output Resistance vs. Supply Voltage (I_{OUT}= -10mA)



Low State Output Resistance vs. Supply Voltage (I_{OUT}= +10mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD_609 All Versions except IXD_609YI	MSL 1
IXD_609YI	MSL 3

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

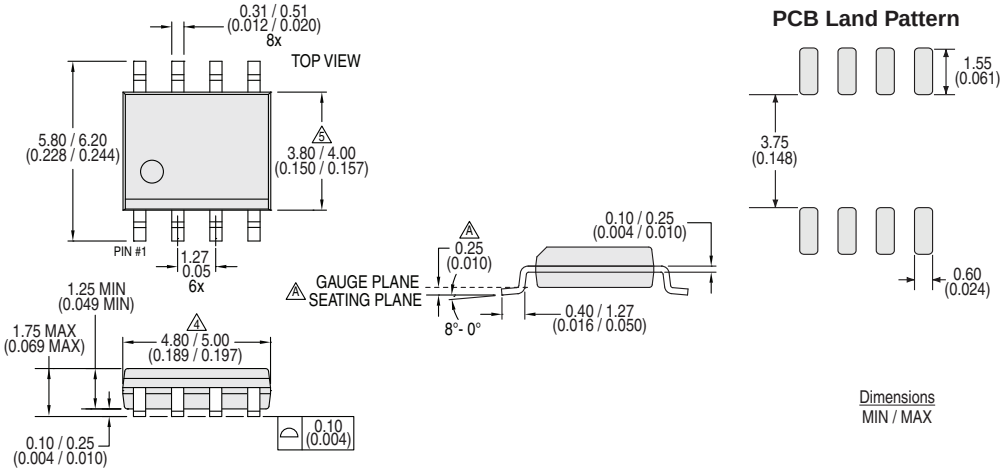
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Maximum Cycles
IXD_609CI	245°C for 30 seconds	30 seconds	1
IXD_609YI	245°C for 30 seconds	30 seconds	3
IXD_609PI	250°C for 30 seconds	30 seconds	3
IXD_609SI / IXD_609SIA / IXD_609D2	260°C for 30 seconds	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

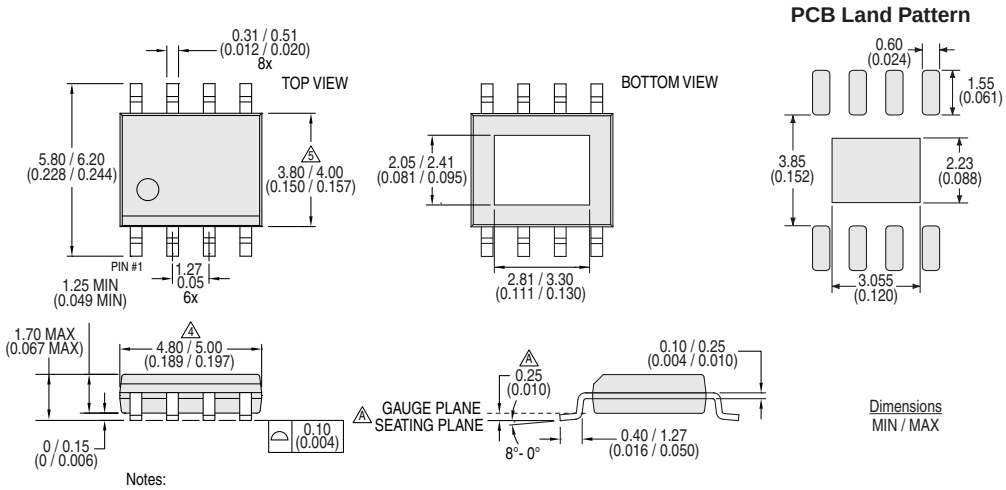
5.5 Mechanical Dimensions

5.5.1 SIA (8-Pin SOIC)



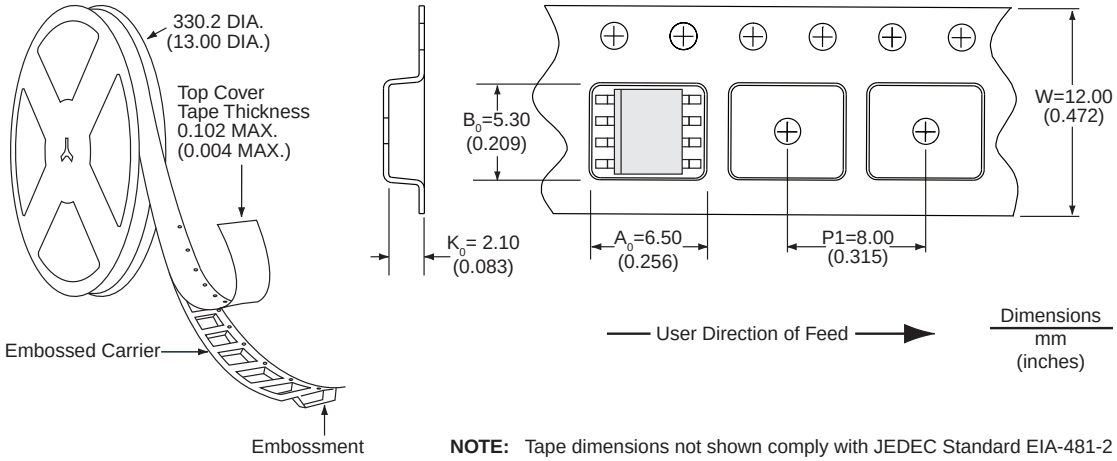
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

5.5.2 SI (8-Pin Power SOIC with Exposed Metal Back)



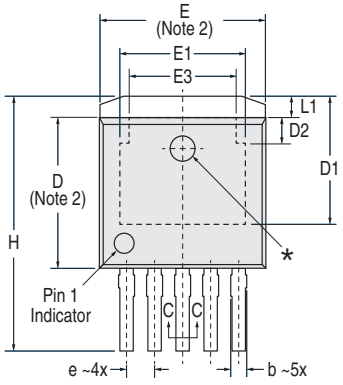
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.5.3 Tape & Reel Information for SI and SIA Packages



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

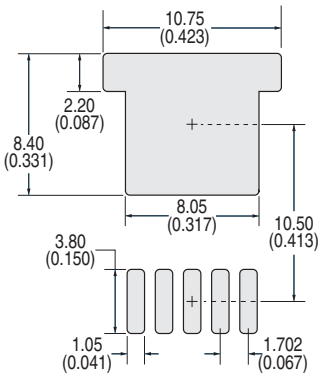
5.5.4 YI (5-Pin TO-263)

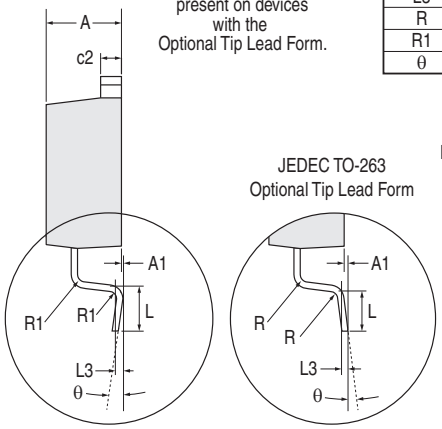


*Circular feature will be present on devices with the Optional Tip Lead Form.

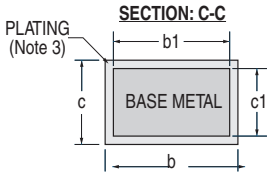
SYMBOL	MM		INCH	
	MIN	MAX	MIN	MAX
A	4.064	4.826	0.160	0.190
A1	0.000	0.254	0.000	0.010
b	0.508	0.991	0.020	0.039
b1	0.508	0.889	0.020	0.035
c	0.381	0.737	0.015	0.029
c1	0.381	0.584	0.015	0.023
c2	1.143	1.651	0.045	0.065
D	8.382	9.652	0.330	0.380
D1	6.858	7.700	0.270	0.303
D2	1.358	1.562	0.053	0.062
E	9.652	10.668	0.380	0.420
E1	6.223	8.000	0.245	0.315
E3	5.092	6.869	0.200	0.270
e	1.702 BSC		0.067 BSC	
H	14.605	15.875	0.575	0.625
L	1.778	2.794	0.070	0.110
L1	1.000	1.676	0.039	0.066
L3	0.254 BSC		0.010 BSC	
R	0.460 TYP		0.018 TYP	
R1	0.506 TYP		0.02 TYP	
θ	-	8°	-	8°

Recommended PCB Pattern



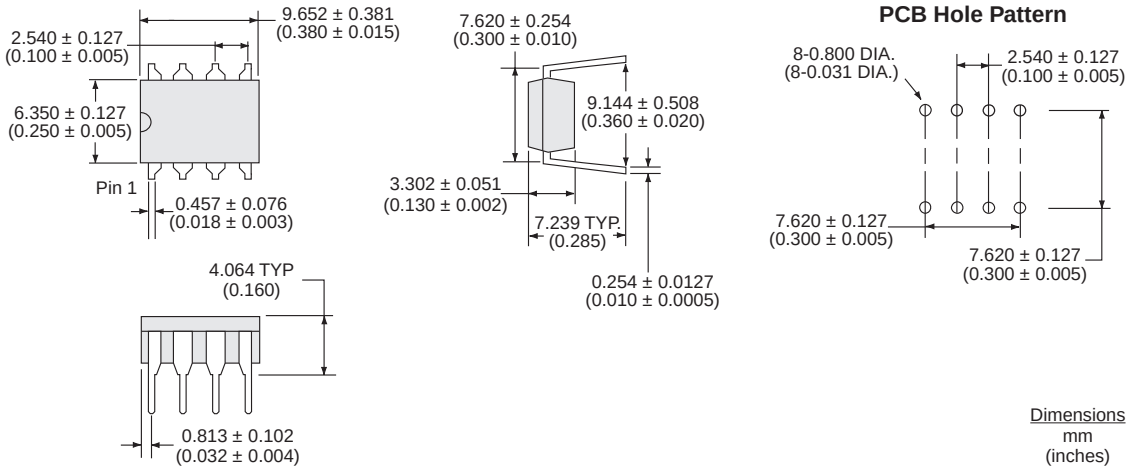


SECTION: C-C

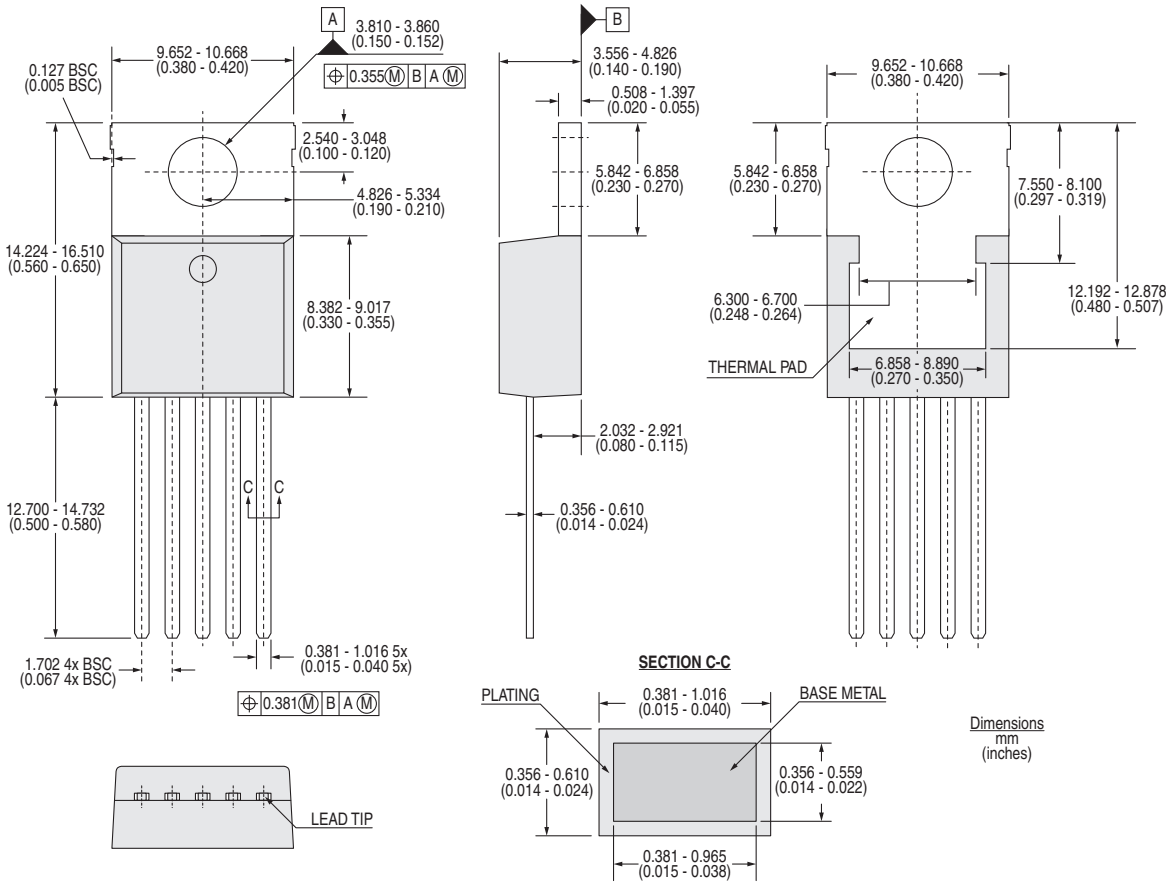


NOTES:
1. Reference JEDEC TO-263 Type "BA".
2. Dimension does not include mold flash; mold flash shall not exceed 0.127mm (0.005 inch) per side.
3. Minimum plating: 1000 microinches.
4. Controlling dimension: millimeters.

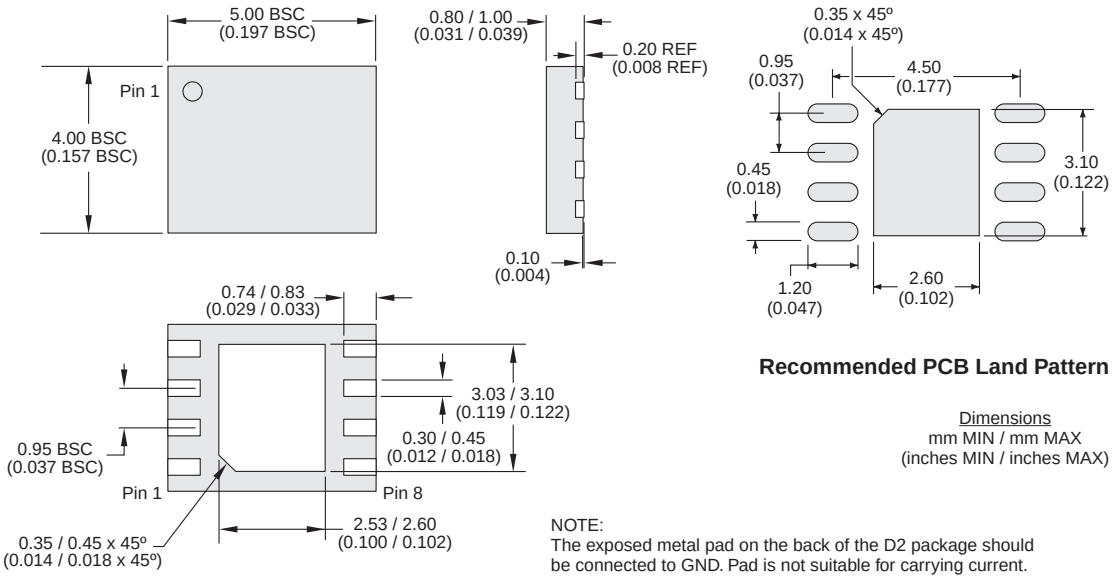
5.5.5 PI (8-Pin DIP)



5.5.6 CI (5-Pin TO-220)



5.5.7 D2 (8-Pin DFN)

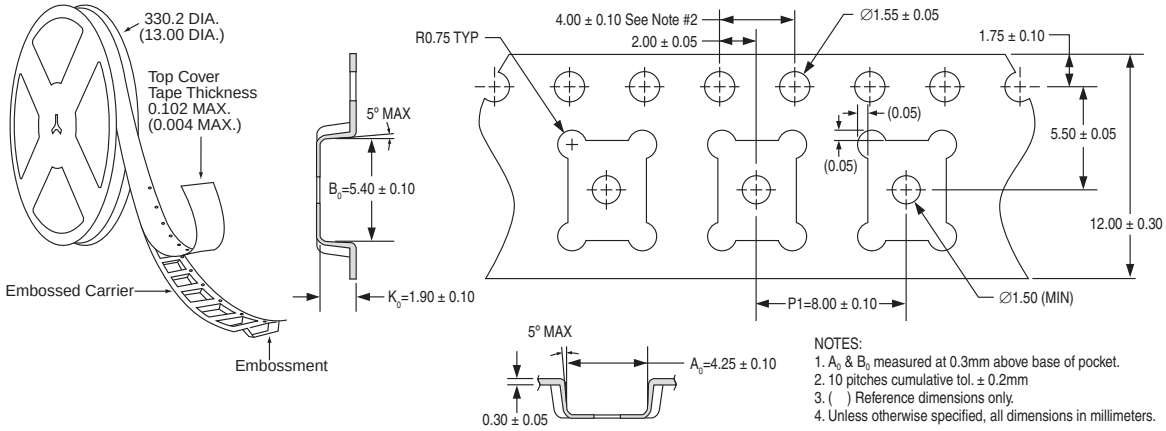


Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE:
The exposed metal pad on the back of the D2 package should be connected to GND. Pad is not suitable for carrying current.

5.5.8 Tape & Reel Information for D2 Package



NOTES:
1. A_0 & B_0 measured at 0.3mm above base of pocket.
2. 10 pitches cumulative tol. ± 0.2mm
3. ( ) Reference dimensions only.
4. Unless otherwise specified, all dimensions in millimeters.

For additional information please visit our website at: www.ixysic.com

Specification: DS-IXD_609-R09

10/25/2017

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

IXYS
A Littelfuse Technology

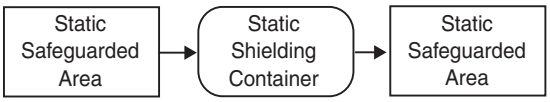
Handling MOS Devices

Static Discharge

Metal Oxide Semiconductor (MOS) devices have gained broad acceptance in telecommunications. This includes use of n-channel (NMOS) transistors, p-channel (PMOS) transistors, or both (complementary or CMOS) transistors. Most IXYS IC Division devices are fabricated using CMOS techniques, but some use PMOS. In any case, MOS circuits require special attention in design and handling because of their susceptibility to damage through buildup of static charges and the currents that occur during discharge.

Whether alone or mounted in circuit boards, MOS ICs are subject to buildup of static charges and damaging discharges. Voltage of several hundred volts can affect these devices, while one or two thousand volts will certainly cause harm. Five hundred volts can easily be generated by a person walking around or moving in a chair, and thousands of volts can be generated by the simple act of pulling out and tearing off a piece of transparent tape. Under these circumstances, precautions must be taken to limit the potential for damage to costly IC devices. MOS ICs should be handled in static-protected or “safeguarded” areas. Such areas include ionized air flow over nonconducting surfaces. When not in these areas, ICs should be kept in static shielded containers. ICs must be handled in safeguarded areas (receiving inspection, stores, assembly, and test) and, when moved from area to area, should be protected by shielded containers. Failure to implement procedures of this sort or relaxation of procedures can result in loss of valuable parts, increased production fallout, and higher repair costs.

Static Transmission



CMOS Latchup

Though all ICs are subject to static discharge damage, CMOS ICs can experience another kind of damaging event known as “latchup” or “SCR.” In this case, large currents can follow-through the part from the power supply, damaging transistors and interconnections. This occurs when currents are injected into the chip where they were not intended, usually through an I/O pin which has been driven to a voltage outside the supply range by some external device or event. This phenomenon is equivalent to four-layer conduction as used in SCRs, where a semiconductor device is “turned on” by injecting a current into a trigger layer. The device stays “on” until voltage is removed. This is useful in SCR control circuits, but in the case of CMOS ICs they may (1) recover completely after power has been cycled, (2) recover, but act very strangely, or (3) blow up completely. Causes can be inadequate power supply filtering, transient protection, or coincidences of PWB track layout. Static discharge may also trigger latchup.

For additional information please visit our website at: www.ixysic.com

Specification: AN-130-R04

4/10/2014

MOSFET/IGBT Drivers
Theory and Applications

1 Introduction

Modern Power Electronics makes generous use of MOSFETs and IGBTs in most applications, and, if the present trend is any indication, the future will see more and more applications making use of MOSFETs and IGBTs.

Although sufficient literature is available on characteristics of MOSFETs and IGBTs, practical aspects of driving them in specific circuit configurations at different power levels and at different frequencies require that design engineers pay attention to a number of aspects.

An attempt is made here to review this subject with some illustrative examples, and with a view to assist both experienced design engineers and those who are just initiated into this discipline.

1.1 MOSFET and IGBT Technology

Due to the absence of minority carrier transport, MOSFETs can be switched at much higher frequencies. The limit on this is imposed by two factors: transit time of electrons across the drift region and the time required to charge and discharge the input Gate and “Miller” capacitances.

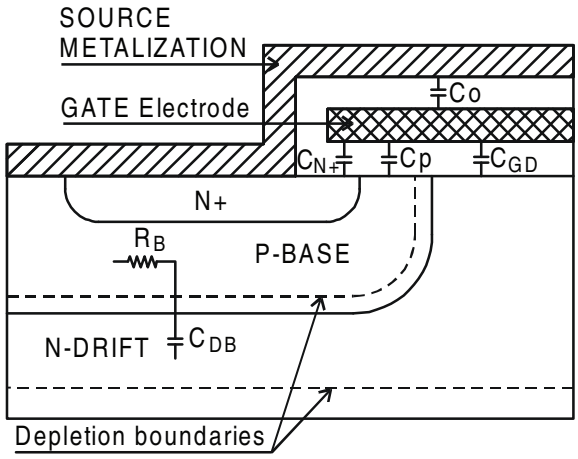
IGBT derives its advantages from MOSFET and BJT topologies. It operates as a MOSFET with an injecting region on its Drain side to provide for conductivity modulation of the Drain drift region so that on-state losses are reduced, especially when compared to an equally rated high voltage MOSFET.

As far as driving the IGBT is concerned, it resembles a MOSFET and hence all turn-on and turn-off phenomena comments, diagrams, and Driver circuits designed for driving MOSFET apply equally well to an IGBT. Therefore, what follows deals only with MOSFET models.

1.2 MOSFET Models and Critical Parameters

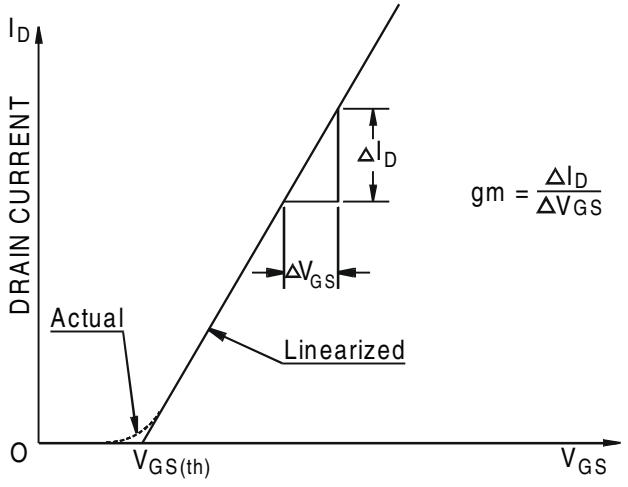
Figure 1 shows the internal cell structure of a DMOS MOSFET. As shown, the Gate to Source Capacitance consists of three components: C_P , the component created by the Gate Electrode over the P-base region; C_{N+}, created by the overlap of the Gate Electrode above the N+ source region; and C_O, arising due to the proximity of the Gate Electrode to the source metallization. In fact, all these are added to yield C_{GS}, which we call the Gate-to-Source Capacitance. It is this total value of capacitance that needs to be charged first to a critical threshold voltage level $V_{GS(th)}$, before Drain Current can begin to flow.

Figure 1 MOSFET Internal Structure



The Gate-to-Drain capacitance, C_{GD} is the overlap capacitance between the Gate electrode and the N-drift Drain region. C_{GD} is sometimes referred to as the “Miller” capacitance, and contributes most to the switching speed limitation of the MOSFET. The junction capacitance between the drain to the P-Base region is C_{DS}. The P-Base region of the MOSFET is shorted to the N+ source. **Figure 2** shows a curve of ID (Drain Current) versus V_{GS} (Gate Source Voltage). The graph has a slope (I_D/ V_{GS}) equal to gm, which is called transconductance.

Figure 2 Power MOSFET Transfer Characteristics



Please note that the actual relationship between V_{GS} and I_D is shown by the dotted line and it can be

observed that in the vicinity of $V_{GS(th)}$, the relationship between V_{GS} and I_D is parabolic in nature:

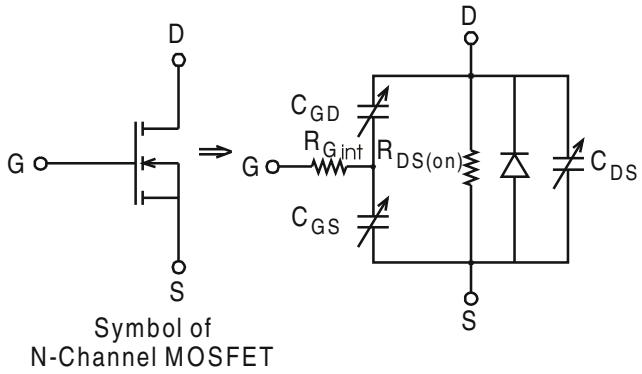
Equation 1.1

$$I_D = K [V_{GS} - V_{GS(th)}]^2$$

However, for Power MOSFETs, it is appropriate to consider the relationship to be linear for values of V_{GS} above $V_{GS(th)}$. The manufacturer's data sheet value of $V_{GS(th)}$ is specified at 25°C.

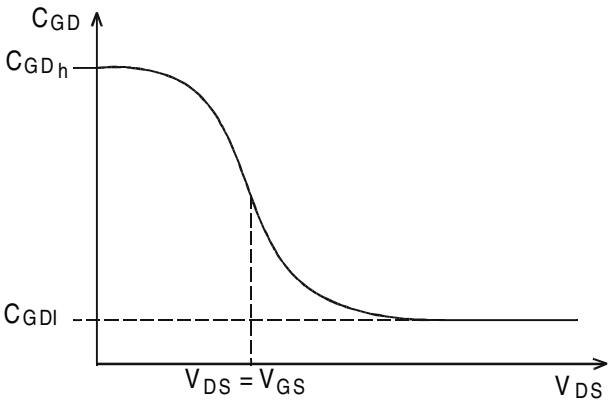
Figure 3 shows a symbol of a N-Channel MOSFET and an equivalent model of the same with three inter-junction parasitic capacitances, namely: C_{GS} , C_{GD} , and C_{DS} .

Figure 3 MOSFET Symbol and Equivalent Circuit



These are all shown as variable, as they indeed are. For example C_{GD} decreases rapidly as the Drain to Source voltage rises, as shown in **Figure 4**.

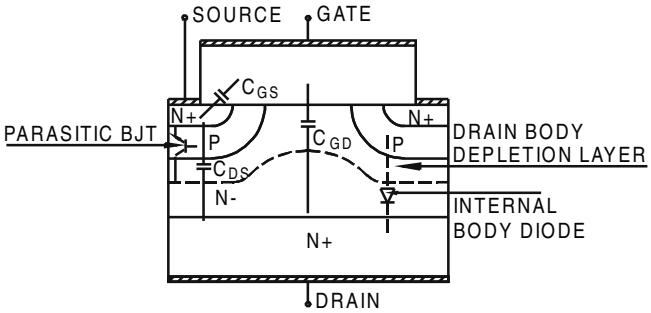
Figure 4 C_{GD} Variation With Respect to V_{DS}



In **Figure 4**, the high value of C_{GD} is called C_{GDh} , while the low value of C_{GD} is termed C_{GDl}.

Figure 5 shows another cross-sectional view of a MOSFET with all these capacitances. In addition, It also shows the internal body diode and the parasitic BJT.

Figure 5 N-Channel MOSFET Internal X-Section



1.3 turn-on and turn-off Phenomena

1.3.1 turn-on Phenomenon

To understand the turn-on and turn-off phenomena of the Power MOSFET, we will use a clamped inductive switching mode of operation, as it is the most commonly used.. This is shown in **Figure 6** and **Figure 7**. A model of the MOSFET is shown with all relevant components, which play a role in turn-on and turn-off events. As stated above, MOSFET's Gate to Source Capacitance C_{GS} needs to be charged to a critical voltage level to initiate conduction from Drain to Source. A few words of explanation will help understand **Figure 6** and **Figure 7**. The clamped inductive load is depicted by a current source with a diode, D, connected antiparallel across the inductor, and the MOSFET's intrinsic internal Gate resistance, R_{Gint} . As described above, the inter-junction parametric capacitances (C_{GS}, C_{GD}, and C_{DS}) are shown, and connected at their proper points. V_{DD} represents the DC Bus voltage applied to the Drain of the MOSFET through the clamped inductive load. The Driver is supplied by V_{CC} referenced by $V_{P,}$ and its ground is connected to the common ground of V_{DD} and is returned to the Source of the MOSFET. The output from the Driver is connected to the Gate of the MOSFET through a resistor R_{Gext}.

Figure 6 MOSFET Being Turned On by a Driver in a Clamped Inductive Load

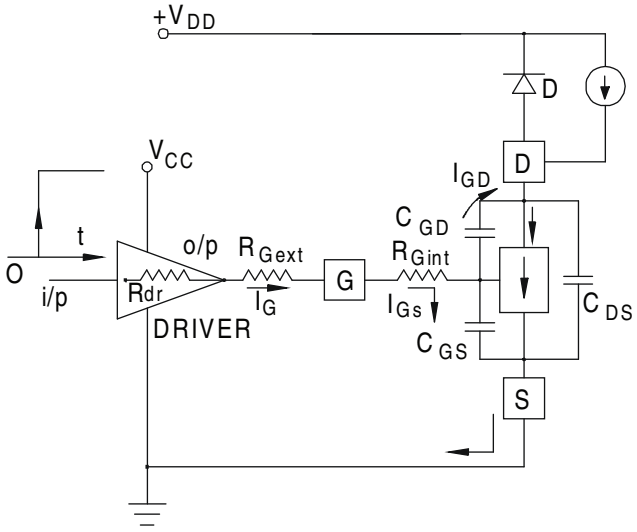
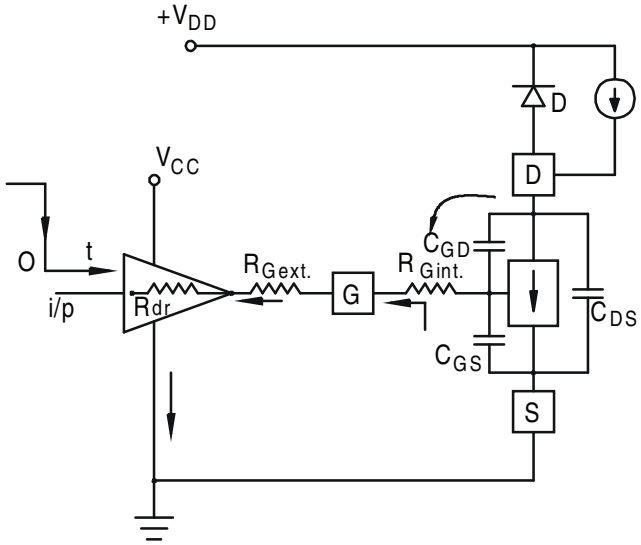


Figure 7 MOSFET Being Turned Off by a Driver in a Clamped Inductive Load



When a positive going pulse appears at the input terminal of the Driver, an amplified pulse appears at the output terminal of the Driver with an amplitude V_P. This is fed to the Gate of the MOSFET through R_{Gext} . As one can see, the rate of rise of voltage, V_{GS}, over the Gate and Source terminals of the MOSFET is governed by value of the total resistance in series (R_{dr}+R_{Gext}+R_{Gint}) and total effective value of capacitance (C_{GS}+C_{GD}). R_{dr} represents the output source impedance of the Driver. R_{Gext} is the resistance one generally puts in series with the Gate of a MOSFET to control the turn-on and turn-off speed of the MOSFET.

The waveforms shown in **Figure 8** depict the variation of these different parameters with respect to time, to help explain the entire turn-on sequence. In **Figure 6** and **Figure 7**, the free-wheeling diode, D, is assumed to be ideal with zero reverse recovery current. The waveforms shown in **Figure 8** are based on this assumption:

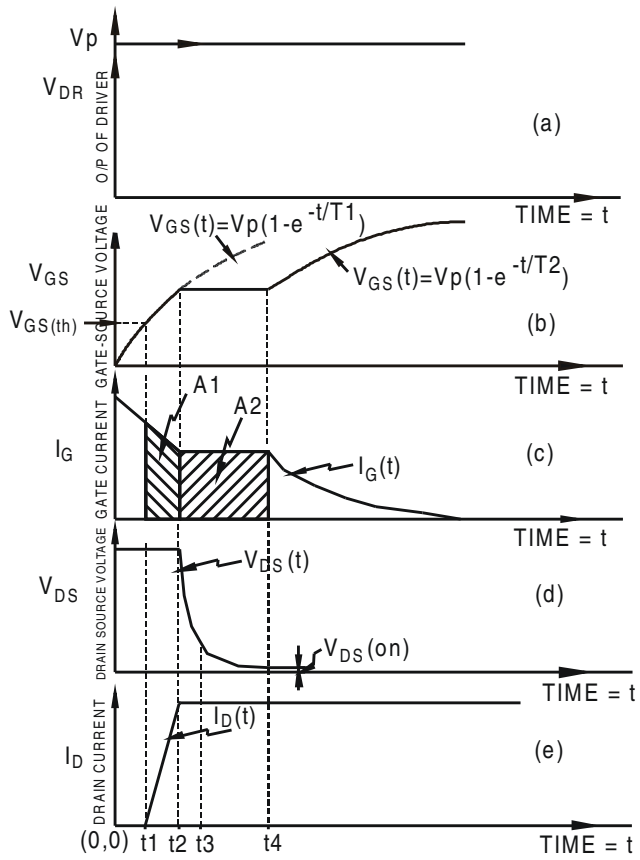
From time zero to t1, (C_{GS}+C_{GDI}) is exponentially charged with a time constant:

$$T1 = (R_{dr} + RG_{ext} + R_{Gint}) \times (C_{GS} + C_{GDI})$$

until the gate-to-source voltage reaches $V_{GS(th)}$. In this time period, neither the drain voltage nor the drain current are affected, i.e. drain voltage remains at V_{DD} and the drain current is zero. This is also referred to as the turn-on delay. Note that between 0 to t1, as V_{GS} rises, I_{GS} falls exponentially, , since it essentially functions as an RC Circuit.

After time t1, as the gate-to-source voltage rises above $V_{GS(th)}$, MOSFET enters a linear region as shown in **Figure 2**. At time t1, drain current starts flowing, and the drain to source voltage V_{DS}, is still at V_{DD} . From the time t1 to t2, I_D increases rapidly and as shown in **Figure 4**, C_{GD} increases from C_{GDl} to C_{GDh} and the current available from the driver is diverted to charge this increased value of C_{GDh} . As outlined in Figure 8, between t1 and t2, the drain current increases linearly with respect to V_{GS} . At time t2, the gate to source voltage enters the Miller Plateau level and the drain voltage begins to fall rapidly, while the MOSFET is carrying full load current. During the time interval, t2 to t4, V_{GS} remains clamped to the same value as does I_{GS} . This is referred to as the Miller Plateau Region. During this interval, most of the drive current available from the driver is diverted to discharge the C_{GD} capacitance followed by a rapid drop of drain to source voltage. Only the external impedance in series with V_{DD} limits the drain current.

Figure 8 MOSFET turn-on Sequence



Beyond t4, V_{GS} begins to rise exponentially again with a time constant:

$$T2 = (R_{dr} + RG_{ext} + R_{Gint}) \times (C_{GS} + C_{GDh})$$

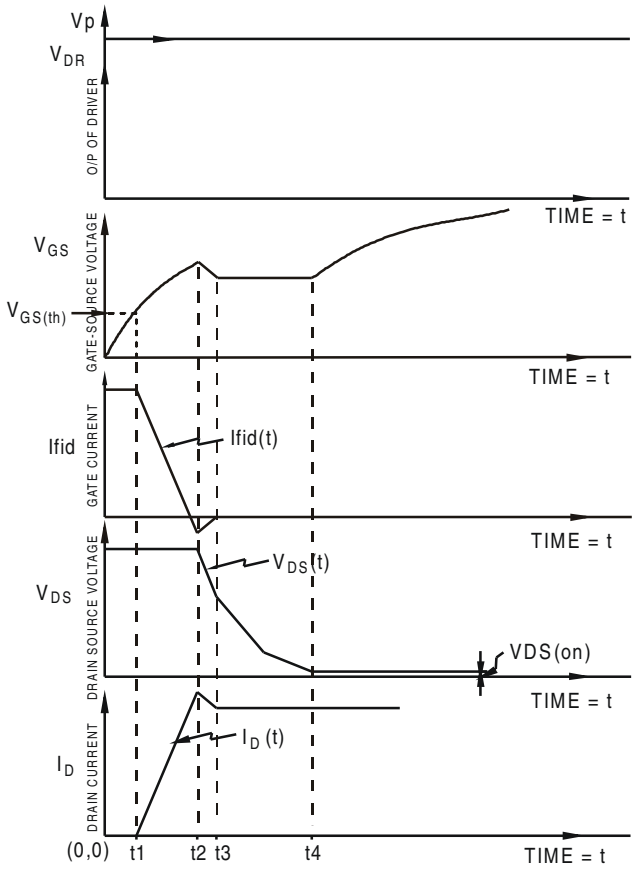
During this time interval the MOSFET approaches its final V_{GS} value effectively determining it's $R_{DS(on)}$. At this point V_{DS} attains its lowest value as determined by:

$$V_{DS} = I_{DS} \times R_{DS(on)}$$

In **Figure 8**, A1 outlines the area of the I_G curve from time t1 to t2. This represents the charge on (C_{GS} +C_{GD}), as it is the integration of the gate current I_G over a time period. Similarly, A2 represents the charge on $C_{GD}$from t2 to t3, during which time the Miller effect is predominant.

If one considers the diode D not to be ideal, then the reverse recovery of the diode will influence the turn on behavior. Thus, the waveforms would look like what is depicted in **Figure 9**. As the diode undergoes reverse recovery, you can see a hump in the waveform of V_{GS} as well as I_D which occurs at approximately time t2.

Figure 9 MOSFET turn-on Sequence Showing the Effect of Body Diode Reverse Recovery



1.3.2 turn-off Phenomenon

The turn-off phenomenon is shown in **Figure 10**. As can be expected, when the output from the driver drops to zero thereby turning off the MOSFET, V_{GS} initially decays exponentially from time 0 to t1 at the rate determined by time constant:

$$T2 = (R_{dr} + RG_{ext} + R_{Gint}) \times (C_{GS} + C_{GDh})$$

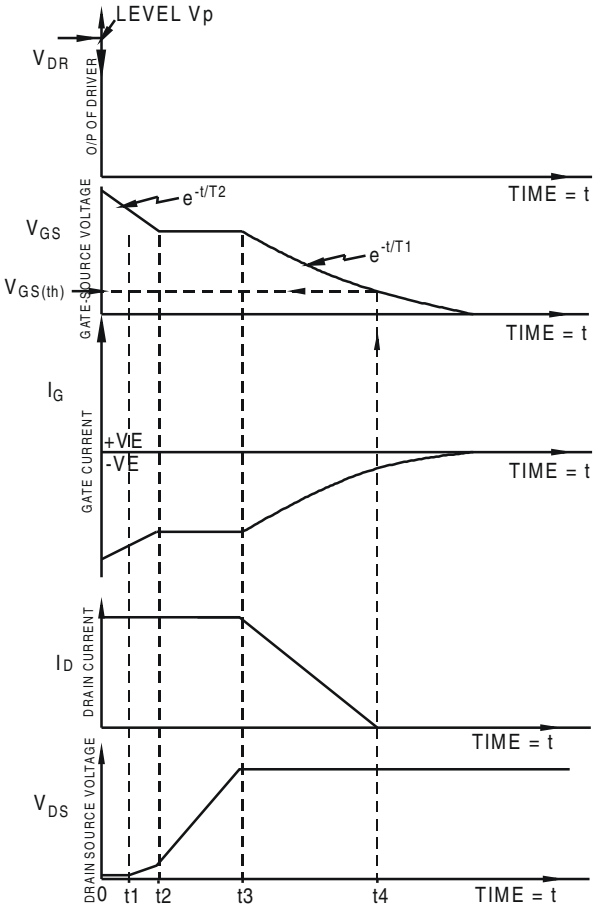
However, after t4, it decays exponentially at the rate determined by:

$$T1 = (R_{dr} + RG_{ext} + R_{Gint}) \times (C_{GS} + C_{GDl})$$

Please note that the first delay in the turn off process is required to discharge the C_{ISS} capacitance from its initial value to the Miller Plateau level. From t = 0 to t = t1, the gate current is flowing through the C_{GS} and C_{GD} capacitances of the MOSFET. Notice that the drain current I_D remains unchanged during this time interval, but the drain source voltage, V_{DS}, just begins to rise. From t1 to t2 , V_{DS} rises from I_D x $R_{DS(on)}$ towards its final off state value of $V_{DS(off)}$, where it is clamped to

the DC bus voltage level by the diode D. This time interval also corresponds to the Miller effect region as mentioned above in regards to the gate voltage, which results in a constant V_{GS}. During the time interval t2 to t3, the V_{GS} begins to fall further below $V_{GS(th)}$. C_{GS} discharges through any external impedance between the gate and source terminals. The MOSFET is in its linear region and the drain current I_D, drops rapidly towards a zero value. V_{DS} was already at its off state value, $V_{DS(off)}$ at the beginning of this interval therefore at t4, the MOSFET is fully turned off.

Figure 10 MOSFET turn-off Sequence



The manufacturer's Data Sheet for the MOSFET gives values of C_{ISS}, C_{RSS}, and C_{OSS}. The following relationships help relate these to inter-junction parasitic capacitances described so far:

Equation 1.2

$$C_{GD} = C_{RSS}$$
$$C_{GS} = C_{ISS} - C_{RSS}$$
$$C_{DS} = C_{OSS} - C_{RSS}$$

As C_{GD} and C_{DS} capacitances are dependent on V_{DS} , the data sheet values are valid only at specified test conditions. Equation 1.3 can be used to calculate the average effective values of these capacitances.

Equation 1.3

$$\text{Effective } C_{GD} = 2(C_{RSS\ specified})(V_{DS.specified}/V_{DS.off})^{1/2}$$
$$\text{Effective } C_{OSS} = 2(C_{OSS\ specified})(V_{DS.specified}/V_{DS.off})^{1/2}$$

1.4 Power Losses In Drivers And Driven MOSFET / IGBT

To determine the power loss in a Driver while driving a power MOSFET, refer to equation 1.4 and the gate charge Q_G vs. V_{GS} curve for different values of $V_{DS(off)}$ found in the MOSFET's data sheet.

Equation 1.4

$$P_{GATE} = V_{CC} \times Q_G \times f_{sw}$$

V_{CC} is the Driver's supply voltage, Q_G is the total gate charge of the MOSFET being driven, and f_{sw} is the switching frequency. Clearly then, it is prudent then to choose a MOSFET with lower value of Q_G.

As shown in **Figure 8, Figure 9**, and **Figure 10** in regards to MOSFET switching losses, there are some short time-intervals during which a finite V_{DS} and I_D co-exist. When this happens during turn-on, the actual integration:

Equation 1.5

$$\int V_{DS}(t) I_D(t) dt$$

is defined as turn-on switching energy loss. Likewise, during turn-off, when finite values of I_D and V_{DS} coexist, the integration of:

Equation 1.6

$$\int V_{DS}(t) I_D(t) dt$$

is called turn-off switching energy loss in a MOSFET. Amongst the responsible parameters in determining these switching energy losses, C_{ISS}, C_{OSS}, and C_{RSS} affect the turn-on and turn-off delays as well as the turn-on and turn-off times.

For an IGBT, it would be similarly shown that:

Equation 1.7

$$\int V_{CE}(t) I_C(t) dt$$

represents the switching energy loss. The time interval for these integrals would be the appropriate time during which finite values of I_D and V_{DS} or V_{CE} and I_C coexist

in a MOSFET or IGBT respectively. Average switching energy lost in the device can be computed as follows:

Equation 1.8

$$\text{MOSFET: } Ps = 1/2 \bullet V_{DS} \bullet I_D \bullet f_{sw} \bullet (t_{on} + t_{off})$$

Equation 1.9

$$\text{IGBT: } Ps = 1/2 \bullet V_{CE} \bullet I_C \bullet f_{sw} \bullet (t_{on} + t_{off})$$

The main emphasis in modern Power Electronics is to reduce the total losses dissipated in devices and subsystems, strive for higher operating efficiency and achieving more compact designs, thereby reducing volume and weight of resultant systems.Since operation at higher and higher switching frequencies is now a necessity, and, as a result, switching losses predominate in the power-loss-budget in semiconductor switches. Reducing switching losses then becomes the single most crucial goal. Keeping this goal in mind, the entire line of IXYS MOSFET/IGBT Drivers are designed to facilitate the design of drive circuits that yield fast rise and fall times.

2 Types of Drivers

2.1 IC Drivers

Although there are many ways to drive MOSFETs and IGBTs using hard wired electronic circuits, IC Drivers offer convenience and features that attract designers. The foremost advantage is compactness. IC Drivers intrinsically offer lower propagation delay. As all important parameters are specified in an IC Driver, designers need not go through the time-consuming process of defining, designing, and testing circuits to drive MOSFET/IGBTs.

2.2 Techniques Available to Boost Current Outputs

A totem-pole stage, with N-Channel and P-Channel MOSFETs, can be used to boost the output from an IC Driver. The disadvantage is that the signal is inverted, and a “shoot-through” condition may exist when the common gate voltage is in transition.

A totem-pole arrangement using matched NPN-PNP transistors, on the other hand, offers many advantages, while boosting the output currents from IC Drivers. The shoot-through phenomenon is absent in this case. The pair of transistors protects each other’s base-emitter junctions and handles current surges quite well. One such arrangement is shown in **Figure 17**. Here Q1 is a NPN transistor, while Q2 is a matched PNP transistor with appropriate collector current rating and switching speed to satisfy the drive requirement for the high-power IGBT. Another feature added is a negative Ve bias (-Ve) for guaranteed fast switch turn-off even in an electrically noisy environment. This is done by utilizing a power supply with +15 and –5 Volts outputs, whose common ground is connected to the IGBT emitter.

IXDD609 is a very high speed IC Driver with extremely short rise and fall times and propagation delays. Its V_{CC} rating is $35V_{DC}$ and can actually deliver 9A peak output current. The arrangement shown in **Figure 17** does a few more things in addition to boosting the output current still higher. It allows one to choose different turn-on and turn-off times by selecting different values of Rg_{on} and Rg_{off}. It allows for incorporating –Ve bias for reasons explained above. A pair of 18V Zener diodes with their cathodes connected together protects the gate-emitter junction of the IGBT from voltage spikes.

2.3 Techniques To Generate –Ve Bias During turn-off

The importance of –Ve bias during turn-off for practically all semiconductor switches cannot be overemphasized, as one may recall from the days of Bipolar transistors. This helps to quickly remove any charge on the C_{GS} and C_{GD} in the case of MOSFETs and IGBTs, thus considerably accelerating turn-off.

It is important to understand that turn-on speed of a MOSFET or IGBT can be increased only up to a level matched by the reverse recovery of rectifiers or diodes in a power supply, because in an inductive clamped load (most common), the turn-on of a MOSFET or IGBT coincides with the turn-off (or reverse recovery completion) of the rectifier diode. Any turn-on faster than this does not help. Too fast a turn-on could also cause oscillation in the drain or collector current. However, it is always beneficial to have a driver with an intrinsic low turn-on time, and then being able to tailor this with a series gate resistor.

The turn-off phenomenon, on the other hand, does not have to wait for any other component in the subsystem. It is here that any enhancement technique can be utilized. Although IXYS drivers by themselves feature extremely low turn-on and turn-off times, an arrangement to provide –Ve bias during turn-off helps provide for a faster turn-off, and also prevents a false turn on even in an electrically noisy environment.

Figure 21 shows how to generate –Ve bias in a transformer coupled drive circuit arrangement. Here a Zener diode can be chosen of appropriate voltage for giving that much –Ve bias (plus one diode drop) during turn-off. Another unique feature of the circuit in **Figure 21** is its ability to maintain an exact pulse waveform across the gate and source. As shown in **Figure 19**, an isolated DC to DC converter with outputs of +15V and –5V is used to power the IXDD614. When the isolated ground of this DC to DC Converter in connected to the emitter of the IGBT being driven, –5V of –Ve bias voltage during provides for a faster turn-off time.

2.4 Need for Under-Voltage Protection

Figure 2 shows depicts a typical transfer characteristics (I_D vs. V_{GS}) of a MOSFET. As can be seen for values of V_{GS} below $V_{GS(th)}$ the drain current is negligible, but in this vicinity, the device is in its linear (Ohmic) region and concurrent application of large

values of V_{DS} could cause a considerable amount of localized heating of the junction. In short, when a MOSFET is being used as a switch, any operation in its linear region could cause overheating or device failure. Bringing the MOSFET quickly into saturation from its off-state is the driver's function. If V_{CC} falls below the minimum required value, linear operation can ensue to the disadvantage of the MOSFET. Note, however that most PWM ICs, controller ICs and microcomputer ICs have this protection feature built-in, and, if sharing the same V_{CC} bus, the driver IC gets the benefit of this function being implemented elsewhere in the subsystem.

2.5 Overload / Short Circuit Protection

Any operation of the MOSFET/IGBT outside the Safe Operating Area (SOA) could cause overheating and eventual device failure, and should be prevented by an electronic active monitoring and corrective arrangement.

Load or current sensing could be done by either a Hall Effect Sensor or by a Shunt resistor in series with source/ emitter terminal. The voltage picked up, which is proportional to current, is low pass filtered and then compared to a preset limit. The comparator output could initiate turn-off of MOSFET/IGBT. A circuit to detect an overload/short circuit is shown in **Figure 19**, where the output FAULT will go low when it occurs.

All IXDD-series drivers have an ENABLE pin, which, when driven low, say, by the FAULT output from this comparator, puts the final N-channel and P-channel MOSFETs of the IXDD Driver in their TRISTATE mode. This not only stops any output from the driver, but also provides an environment for implementing a "soft turn-off". To accomplish this,a resistor of sufficient value is connected from the gate to the source/emitter of the MOSFET. As a result, the C_{GS} gets discharged through this resistor and, depending on the value of the connected resistor, a soft turn-off of any duration can be achieved. Another way, as shown in **Figure 12**, is to use a signal MOSFET, Q1, to pull down the gate when a short circuit is detected. The resistor in series with this signal MOSFET determines the time duration of this soft turn-off. Soft turn-off helps protect the IGBT/ MOSFET from any voltage transients generated due to LdI_C/dt (or LdI_D/dt) that could otherwise bring about avalanche breakdown. The PC board layout for this circuit is shown in **Figure 13**.

For an IGBT, de-sat detection (de-sat = desaturation of forward voltage drop) is a method used for short circuit/ overload protection. When a short circuit/overload occurs, the forward voltage drop of the IGBT (V_{CE}) rises to disproportionately high values. One must ignore the initial turn-on rise in V_{CE}, when output from the driver has still not risen to a high enough value. Nevertheless, when V_{CE} rises to a level of, say, 7 Volts, in presence of sufficient gate drive voltage, it means the collector current I_C has risen to a disproportionately high value, signaling overload. When a voltage level higher than 6.5V is detected, resulting in soft turn-off of the IGBT. **Figure 19** shows how the de-sat feature can be wired into a total driver circuit, using also other features, such as opto-isolation and –Ve turn-off bias.

3 High Side Driving Techniques

3.1 Employing Charge-Pump and Bootstrap Methods

The Bootstrap Technique as shown in **Figure 15**. The basic bootstrap building elements are the level shift circuit; bootstrap diode, DB; level shift transistor, Q1; bootstrap capacitor, CB; and IXDD609 or IXDD614. The bootstrap capacitor, IXDD609/IXDD614 driver, and the gate resistor are the floating, source-referenced parts of the bootstrap arrangement. The disadvantages of this technique are longer turn-on and turn-off delays, and 100% duty cycle is not possible. Also, the driver has to overcome the load impedance and negative voltage at the source of the device during turn-off.

3.2 Achieving Galvanic Isolation By Using Optocouplers To Drive Upper MOSFET/IGBT

For driving high-side MOSFET/IGBT in any topology, optocouplers can be used with the following advantages:

- Optocouplers provide a very high isolation voltage: 2500V to 5000V of isolation is achievable with careful selection.
- Optocouplers can handle signals from DC to several MHz.
- Optocouplers are easily interfaced to controller ICs, micro-computers, or any PWM IC.

One disadvantage is that the optocoupler adds its own propagation delay. Another disadvantage is that a separate, isolated power supply is required to feed the output side of the optocoupler and the driver connected to it. However, isolated DC to DC Converters with a few thousand Volts of isolation are readily available. These can be used to supply isolated and regulated +Ve 15V and –Ve 5V to the output side of the optocoupler and the driver IC for driving upper MOSFET/IGBT as is shown in **Figure 19** and **Figure 20**. As can be seen, an identical chain of optocouplers, drivers, and DC to DC converters are used for even lower IGBTs. This is done to guarantee identical propagation delays for allincoming IGBT gate signals.

3.3 Use Of Transformers To Obtain Galvanic Isolation in Driving Upper MOSFET/IGBT

Using transformers to achieve galvanic isolation is a very old technique. Depending on the range of frequencies being handled and power rating (voltage and current ratings and ratios), transformers can be designed to be quite efficient. The gate drive transformer carries very small average power, but delivers high peak currents at turn-on and turn-off of the MOSFET/IGBT.

While designing or choosing a gate drive transformer, keep the following points in mind:

- The average power of the transformer can accept should be used as a design guideline. A margin of safety should be taken into account, keeping in mind the maximum volt-second product and allowing for worst case transients with maximum duty ratio and maximum input voltage possible.
- Employing bifilar winding techniques to eliminate any net DC current in any winding. This is to avoid core saturation.
- If operation in any one quadrant of B-H loop is chosen, care should be taken for resetting the core.

Advantages of employing transformers for Gate Drive are:

- There is no need for any isolated DC to DC Converter for driving an upper MOSFET/IGBT .
- There is practically no propagation delay time in a transformer to carry signals from primary side to the secondary side.
- Several thousand volts of isolation can be built-in between windings by proper design and layouts.

The disadvantages of using transformers for Gate Drive are:

- They can be used only for AC signals.
- Large duty ratios cannot be handled by the transformer without being saturated by net DC, unless AC coupling capacitors are employed in series.

Two examples of gate Drive circuits, using transformers follow. In **Figure 18**, a phase shift controller outputs its signals to the IXDD604 dual drivers, which in turn, feed the transformers. The secondary windings of these transformers are coupled to the Gates of upper and lower MOSFETs in an “H” Bridge topology. **Figure 21** shows another transformer coupled gate drive circuit employing a DC restore technique to maintain the same waveshape as the original signal with the added feature of -Ve bias offered using a Zener in series with a fast diode across the secondary.

4 IXYS Line of MOSFET and IGBT Drivers

IXYS offers the following MOSFET/IGBT drivers:

- IXD_602: Dual 2A, Ultrafast Driver
- IXD_604: Dual 4A, Ultrafast Driver, w/Enable
- IXD_609: 9A, Ultrafast Driver, w/Enable
- IXD_614: 14A, Ultrafast Driver, w/Enable
- IXD_630: 30A, Ultrafast Driver, w/Enable

4.1 General Remarks About IXD_600 Series Of Drivers

The most important strength of these drivers is their ability to provide the high currents needed to adequately drive today's and tomorrow's large size MOSFETs and IGBTs. This is made possible by devoting a large portion of the silicon die area to creating a high current (NMOS and PMOS) output stage. Another important feature of these drivers is that there is no cross conduction, thus giving almost 33% lower transition power dissipation.

In addition, some of these Drivers incorporate a unique facility to disable the output by using an ENABLE pin. When this pin is driven LOW in response to detecting an abnormal load current, the driver output enters its tristate (high impedance state) mode, and a soft turn-off of the MOSFET/IGBT can be achieved. This helps prevent damage that could occur to the MOSFET/IGBT due to a LdI/dt overvoltage transient, if it were to be switched off abruptly, "L" representing the total inductance in series with Drain or Collector. A suggested circuit to accomplish this soft turn off upon detecting overload or short circuit is shown in **Figure 12**. It is also possible to do this by an independent short circuit/overload detect circuit, which could be a part of the PWM or other controller IC. All one needs to do is to take an output signal (FAULT) from such a circuit, and feed it into the ENABLE pin of the driver. A resistor, R_P ,connected across gate and source or gate and emitter (as the case may be) would ensure soft turn-off of the MOSFET/IGBT, turn-off time being equal to $R_P(C_{GS} + C_{GD})$

Detailed specifications of these IXD_600 series of drivers are available on IXYS's web site:

http://www.ixysic.com/Products/IGBT-MOSFETDvr.htm

4.1.1 IXD_604

IXD_604 is a dual 4A driver, which is useful in many circuits employing two MOSFETs or IGBTs. It could also be used for two MOSFETs/IGBTs connected ina phase leg configuration. While using high voltage DC supplies for driving the phase leg, H-Bridge, or 3-phase bridge circuits, some technique for achieving galvanic isolation of the upper MOSFET/IGBT drivers is required, in addition to making a provision for the isolated power supplies.

Figure 18 shows an interesting application for IXDD604 in a phase shift PWM controller application, in which galvanic isolation is obtained by using ferrite core gate drive transformers. Note that this controller operates at a fixed frequency. Turnoff enhancement is achieved by using local PNP transistors.

IXDD604 provides a simple answer for driving a vast number of low and medium current MOSFETs and IGBTs.

4.1.2 IXD_609 AND IXD_614

The IXD_609 is eminently suitable for driving higher current MOSFETs and IGBTs, howeverthe IXD_614 can drive larger size MOSFET/IGBT Modules. Many circuit schematics applying these in various topologies are possible, and some of these are shown at the end of this application note.

The 5-pin TO-263 surface mount version can be soldered directly on to a copper pad on the printed circuit board for better heat dissipation. It is possible then to use these high current drivers for very high frequency switching application, driving high current MOSFET modules for a high power converter/inverter.

Figure 11 shows a basic low side driver configuration using the IXDD609 or IXDD614. C1 is used as a bypass capacitor placed very close to pins #1 and #8 of the driver IC. **Figure 16** shows a method to separately control the turn-on and turn-off times of the MOSFET/IGBT. turn-on time can be adjusted by Rg_{on}, while the turn-off time can be varied by Rg_{off}. The diodes in series are fast diodes with a low forward voltage drop. The 18V, 400mW Zener diodes protect the gate-emitter junction of the IGBT. When laying out a PCB, the trace length between pins #6 and #7, and the IGBT gate pins should be as short as possible. Also, providing a generous copper surface for a ground plane helps achieve fast turn-on and turn-off times without creating oscillation in the drain/collector current.

Figure 16 also shows another arrangement, and includes a method for faster turn-off using a PNP transistor placed very close to the MOSFET gate and source. It is a good practice to tie the ENABLE pin of

drivers to V_{CC} through a 10kΩ resistor. This ensures that the driver always remains in its ENABLED mode, except when driven low due to a FAULT signal. Again, this FAULT signal puts these two drivers into their TRISTATE output mode.

Figure 17 shows a method to boost output from IXDD609 to a much higher level for driving a very high power IGBT module. Here the turn-on and turn-off times can be varied by choosing different values of resistors, Rg_{on} and Rg_{off}. To provide a –Ve bias of 5V, the IGBT emitter is grounded to the common of +15V and
-5V power supplies, which feeds +15V and –5V to the IXDD609. Notice that the incoming signals must also be level shifted.

Figure 19 shows an IXDD614 driving one IGBT of a Converter Brake Inverter (CBI) module. Here all protection features are incorporated. For high temperature cutoff, a bridge circuit is used with the CBI module's thermistor. Comparator U3 compares the voltage drop across the thermistor to the stable voltage from the Zener diode. P1 can be used to preset the cutoff point at which the comparator's output goes low. This is fed into the microcomputer as an OVERTEMP signal.

Short circuit protection is provided by continuously monitoring the voltage drop across a SHUNT. Note that one end of SHUNT is connected to the power supply ground GND1. The voltage picked up from this SHUNT is amplified by a low noise op-amp, and is then compared to the stable voltage from the same Zener. When a short circuit occurs, the comparator output (FAULT) goes low. 1% metal film resistors are used throughout in both these circuits to ensure precision and stability. C3 and C4 help in offering low-pass filtering to avoid nuisance tripping.

Principle of DESAT sensing for detecting overload on an IGBT has been explained before, **see "Overload / Short Circuit Protection" on page 9**. In the case of an AC Motor Drive, each IGBT has to be protected from overload using separate DESAT sensing. **Figure 19** and **Figure 20** show the connection for each IGBT. DESAT sensing is done on the isolated side of each optocoupler, while the resultant FAULT signal is generated on the common input side with respect to GND1. Each FAULT signal is open-collector type and hence can be tied together with other FAULT signals from other optocoupler or from other comparators. The microcomputer will stop output drive signals when either the FAULT or the OVERTEMP signal goes low. When this happens, notice that IXDD614 offers a -Ve bias of -5V to guarantee turn-off conditions, even in the presence of electrical noise. -5V is applied to the gate of each IGBT during turn-off even under normal operating conditions. After the fault is cleared, the microcomputer can issue a RESET signal for resuming normal operation.

5 Practical Considerations

When designing and building driver circuits for MOSFETs and IGBTs, several practical aspects have to be taken into consideration to avoid prevent voltage spikes, oscillation or ringing, and false turn-on. More often than not, these are a result of improper or inadequate power supply by-passing, layout and mismatch of driver to the driven MOSFET/IGBT.

As we now understand, turning a MOSFET or an IGBT on and off amounts to charging and discharging large capacitive loads. Suppose we are trying to charge a capacitive load of 10,000 pF from $0V_{DC}$ to $15V_{DC}$ (assuming we are turning on a MOSFET) in 25 ns, using the IXDD614, which is a 14A, ultra high speed driver.

Equation 5.1

$$I = \Delta VxC / \Delta t$$
$$I = [(15-0)x10000x10^{-12} / 25x10^{-9}] = 6A$$
$$I = 6A$$

What this equation tells us is that current output from the driver is directly proportional to the voltage swing and/or the load capacitance, and inversely proportional to rise time. Actually the charging current would not be steady, but would peak around 9.6A, well within the capability of IXDD614. However, IXDD614 will have to draw this current from its power supply in just 25 ns. The best way to guarantee this is by putting a pair of by-pass capacitors (of at least 10 times the load capacitance) of complementary impedance characteristics in parallel, very close to the V_{CC} pin of IXDD614. These capacitors should have the lowest possible ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). One must keep the capacitor lead lengths to the bare minimum.

Another very crucial point is proper grounding. Drivers need a very low impedance path for current return to ground, to avoid ground loops. The three paths for returning current to ground are:

- Between IXDD614 and the logic driving it.
- Between IXDD614 and its own power supply.
- Between IXDD614 and the source/emitter of the MOSFET/IGBT being driven.

All these paths should be extremely short in length to reduce inductance and be as wide as possible to reduce resistance. Also, these ground paths should be kept distinctly separate to avoid returning ground current from the load to affect the logic line driving the IXDD614. A good method is to dedicate one copper plane in a multilayered PCB to provide a ground surface. All ground points in the circuit should return to the same physical point to avoid generating differential ground potentials.

With desired rise and fall times in the range of 25 to 50ns, extreme care is required to keep lengths of current carrying conductors to the bare minimum. Since every inch of length adds approximately 20 nH of inductance, a dI/dt of 240 Amps/microsecond (used in the example calculation for Equation 5.1) generates a transient LdI/dt voltage of 4.8V per inch of wire length, which subtracts from the driver's output. The real effect will be a significant increase in rise time for every tiny increase in conductor length from the output pin of the driver to the gate lead of the MOSFET/IGBT. For example, one extra inch of conductor length could increase rise time from 20ns to 70ns in an ultra high speed gate drive circuit. Another detrimental effect of longer conductor length is transmission line effect and resultant RFI/EMI.

It is prudent to also keep in mind the fact that every MOSFET/IGBT has some inductance depending on the package style and design. The lower this value, the better is the switching performance, as this inductance is, in effect, in series with the source/emitter, and the resulting negative feedback increases switching times. IXYS MOSFETs and IGBTs are housed in packages that have extremely low intrinsic inductance.

When using a driver IC for any application, it is also necessary to compute the power dissipated in the driver for a worst-case scenario. The total power dissipated in the driver IC is the sum of the following:

- Capacitive load power dissipation;
- Transition power dissipation;
- Quiescent power dissipation.

For all members of the IXD_609 series of drivers, transition power dissipation is absent due to a unique method (patent pending) of driving the output N-channel and P-channel MOSFETs that practically eliminates cross conduction.

As described earlier, **see "Power Losses In Drivers And Driven MOSFET / IGBT" on page 6**, a MOSFET/IGBT driver incurs losses. The formula to calculate the power loss in a driver is:

Equation 5.2

$$P_{D(on)} = \frac{D \times R_{OH} \times V_{CC} \times Qg \times fsw}{R_{OH} + R_{Gext} + R_{Gint}}$$

Equation 5.3

$$P_{D(off)} = \frac{(1-D) \times (R_{OL} \times V_{CC} \times Qg \times fsw)}{R_{OL} + R_{Gext} + R_{Gint}}$$

where:

- R_{OH} = Output resistance of driver @ output High
- R_{OL} = Output resistance of driver @ output Low
- fsw = Switching frequency
- R_{Gext} = resistance kept externally in series with gate of MOSFET/IGBT
- R_{Gint} = Internal mesh resistance of MOSFET/IGBT
- D = Duty Cycle (Value between 0.0 to 1.0)
- Qg= Gate Charge of MOSFET/IGBT

Total loss $P_D = P_{D(on)} + P_{D(off)}$

Note also that, in general, R_{Gint} is small and can be neglected, and that $R_{OH} = R_{OL}$ for all IXD_600 series drivers. Consequently, if the external turn-on and turn-off gate resistors are identical, then the total driver power dissipation formula simplifies to:

Equation 5.4

$$P_D = P_{D(on)} + P_{D(off)} = \frac{R_{OH} \times V_{CC} \times Qg \times fsw}{R_{OL} + R_{Gext}}$$

As an example:

- Assume that we are driving an IXFN200N10P for a telecom power supply application or for a UPS/Inverter application at a switching frequency of 20 kHz.
- R_{Gext} = 4.7 Ohms and gate supply voltage is 10V.

In the IXDD609 Data sheet, we read the value of R_{OH}=2Ω(max) and R_{OL}=1.5Ω(max). For Qg, refer to the data sheet for the IXFN200N10P from www.ixys.com, and go to its Gate Charge vs. V_{GS} curve. Look for the value of Qg at V_{GS}=10V. You can read it as approximately 235nC. Substituting these values into Equation 5.4 yields:

$$P_D = \frac{2 \times 15 \times 235 \times 10^{-9} \times 20000}{1.5 + 4.7}$$

$$P_D = 22.74mW$$

Assuming an ambient temperature of 50°C in the vicinity of the IXDD609PI, the power dissipation capability of IXDD609PI must be derated by 8mW/°C, which is 200mW. The maximum allowable power dissipation at this temperature becomes 1000-200=800mW. However, as calculated above, we will be dissipating only 22.74mW, so we are well within the dissipation limit of 777.26mW.

If one increases fsw to 500kHz for a DC to DC converter application, keeping other parameters the same as above, now the dissipation would be 569mW. Again we are still within the dissipation limit of 231mW.

Another example: A boost converter, using IXFK55N50 at V_{DS}=250V_{DC} and at I_D=27.5A. Assume that fsw=500kHz and V_{CC}=12 V. From the curve of Gate Charge for the IXFK55N50 in its data sheet, one can determine that Qg=370nC. Set R_{Gext}=1Ω . We use IXDD614YI or IXDD614CI here, both of which can dissipate 12W. Here, the maximum value of R_{OH}=1.5Ω, R_{OL}=1.2Ω . Substituting the above values in the equation, the power dissipation is computed to be:

$$P_D = \frac{1.5 \times 12 \times 370 \times 10^{-9} \times 500000}{1.2 + 1}$$

$$P_D = 1.51W$$

For the third example, consider driving the large size MOSFET module, VMO 580-02F with IXD_630YI, at fsw=250kHz. Let V_{CC}=10V, R_{OH}=0.17Ω,R_{OL}=0.16Ω, R_{Gext}=0Ω. From the data sheet: Qg=2750nC at V_{CC}=10 V. Substituting:

$$P_D = \frac{0.17 \times 10 \times 2750 \times 10^{-9} \times 250000}{0.16 + 0}$$

$$P_D = 7.3W$$

IXDD630YI (TO-263) or IXDD630CI (TO-220) can easily drive this load provided adequate heatsinking and proper air flow are maintained. Comments above for mounting TO-263 and TO-220 packages apply here as well. For derating use 0.1W/°C. So for an ambient temperature of 50°C, the answer is 2.5 W. As the limit of IXDD630YI or IXDD630CI is 12 W, subtracting 2.5W from this yields 9.5W; therefore, 7.3W is possible with or without a proper heat sink. Thermal impedance (junction to case) is 0.55°C/W for TO-263 and TO-220, hence a rise in case temperature should be within limit. If we increase V_{CC} to 15V, then conduction losses in the MOSFET could reduce due to lower $R_{DS(on)}$, but obtaining the same rise and fall times will incur more power loss in the driver due to increased V_{CC} and Qg. If that happens, the approach described in **Figure 17** can be employed.

6 Conclusion

With proliferating applications of modern power electronics worldwide, faster, more efficient and more compact MOSFETs and IGBTs are replacing older solid state and mechanical devices. The design of newer and more efficient techniques to turn these solid state devices on and off is a subject that requires thorough study and understanding of the internal structure and dynamic processes involved in the working of MOSFET/IGBTs.

With the advent of IC drivers for these fast MOSFET/IGBTs, the designer is relieved of the tedious task of designing elaborate driver circuits. Nevertheless, understanding these newer ICs, their strengths and limitations, is of paramount importance. Different configurations for particular topologies call for specific application knowledge. Illustrations are the best way to explain theory and applications of these IC drivers. Practical use of these IC drivers calls for great care for achieving near theoretical results.

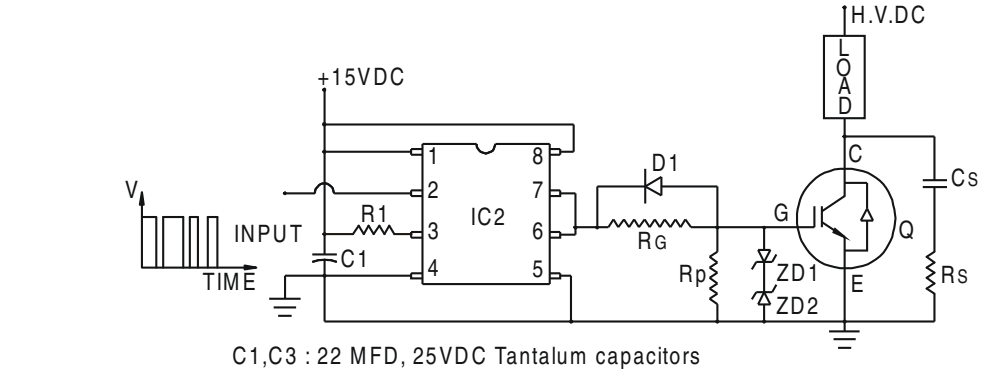
7 References:

1. B. Jayant Baliga, “Power Semiconductor Devices”, PWS Publishing Company, Boston, MA (1996)

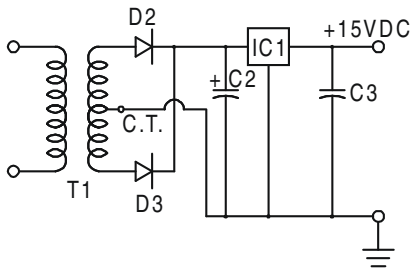
2. Ned Mohan, Tore M. Undeland, William P. Robbins: “POWER ELECTRONICS: Converters, Applications and Design”, John Wiley & Sons, New York (1994)

3. Power Supply Design Seminar - 2001 series, Unitrode Products from Texas Instruments.

Figure 11 Using IXDD609 or IXDD614 to Drive an IGBT

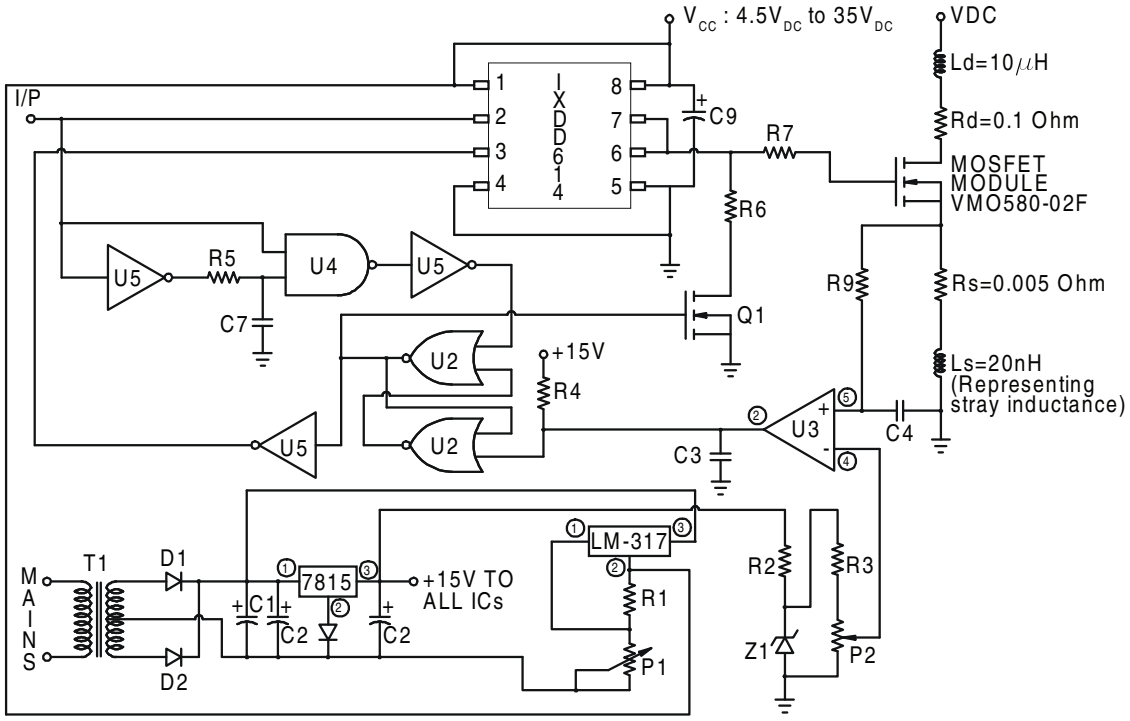


C1,C3 : 22 MFD, 25VDC Tantalum capacitors
C2 : 2200 MFD, 35VDC Electrolytic capacitors
T1 : 220 VAC to 15-0-15 VAC, 15VA control transformer
110VAC TO 15-0-15
Q : IXLF19N250A



IC1 : 7815 Regulator
IC2 : IXDD609 or IXDD614
D1 : IN5817
D2,D3 : IN4002
ZD1,ZD2 : 18V, 400MW ZENERS
RG1 : 3.3 ohms to 27 ohms
depending on Turn-ON speed
Rp : 2K2, ¼ W, 5%
Cs,Rs : Snubber network to reduce IGBT switching losses. Value depends upon fsw. Suggest:
Cs=0.1 MFD, Rs=10 to 33 ohms
R1 : 10K, ¼ w

Figure 12 Soft turn-off Evaluation Circuit for IXDD609 and IXDD614



Bill of Materials for Figure 12

Resistors:

R1: 240

R2: 560

R3: 10K

R4: 5K

R5: 1Meg

R6: 1K5

R7: Rg-T.B.D.

R8: 1Meg

Capacitors:

C1: 1000mF;35VWDC

C2: 22mF, 63 VWDC

C3: 1pF, silver dipped mica

C4: 100pF silver dipped mica

C5: 0.1mF, 35WDC Tantalum

C6: 0.1mF, 35VWDC Tantalum

C7: 1pF silver dipped mica

C8: 0.1mF, 35VWDC Tantalum

C9: 0.1mF, 35VWDC Tantalum

C10: 0.1mF, 35VWDC Tantalum

Diodes:

D1: 1N4002 or BA 159

D2: 1N4002 or BA 159

Zener Diodes:

1. Z1: 1N821

Voltage Regulators:

1. 7815

2. LM317T

Transistors:

1. Q1: 2N7000

ICs:

U1: IXDD609SI or IXDD614SI

U2: CD4001

U3: LM339

U4: CD4011

U5: CD4049

U6: IXDD609YI or IXDD614YI

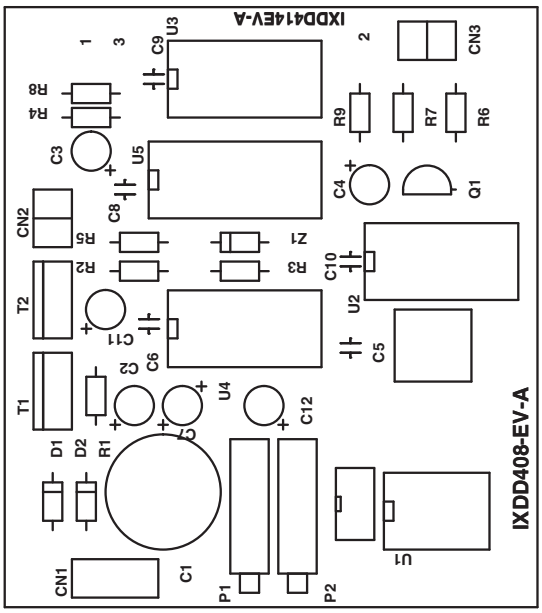
Note: Use either U1 or U6 but not both.

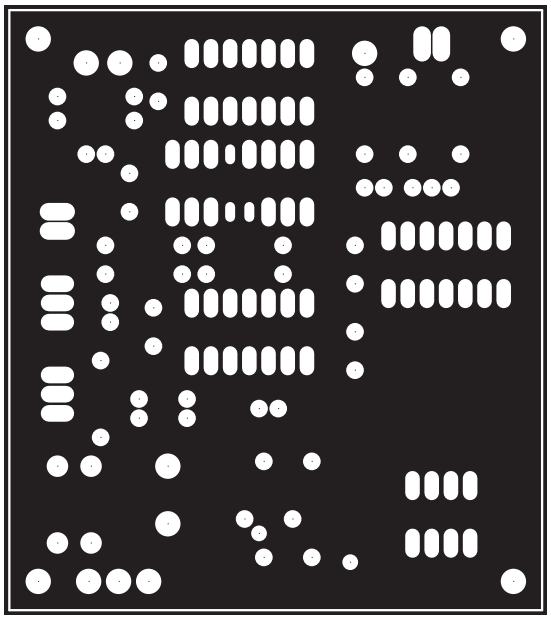
Trimmers:

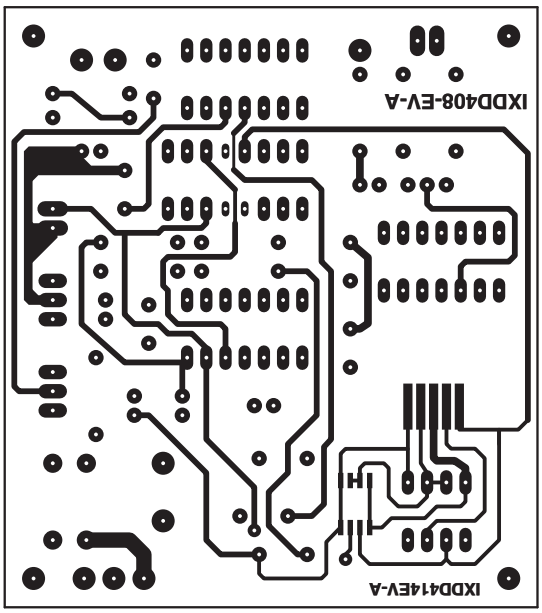
P1: 5K, 3006P Bourns or Spectrol

P2: 1K, 3006P Bpurns or Spectrol

Figure 13 +VE and -VE and Component Layout with Silk-Screen Diagram







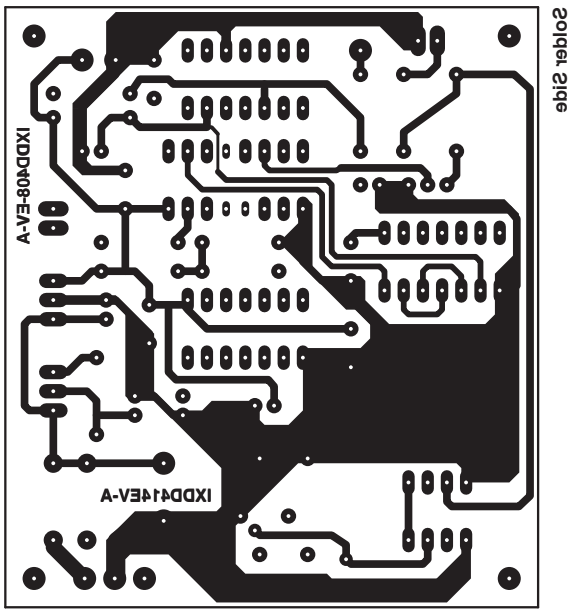


Figure 14 Basic Charge Pump Doubler

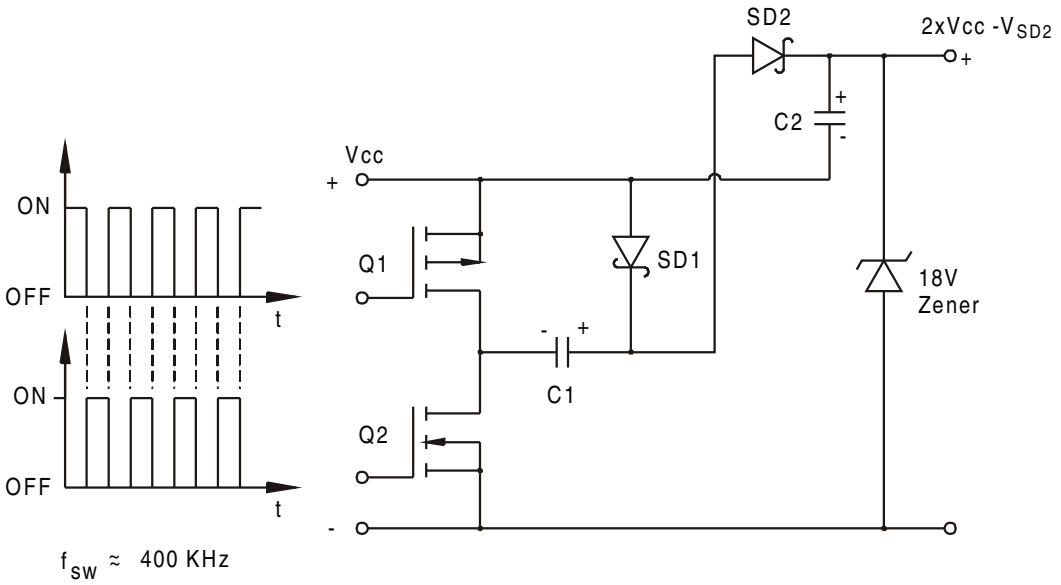
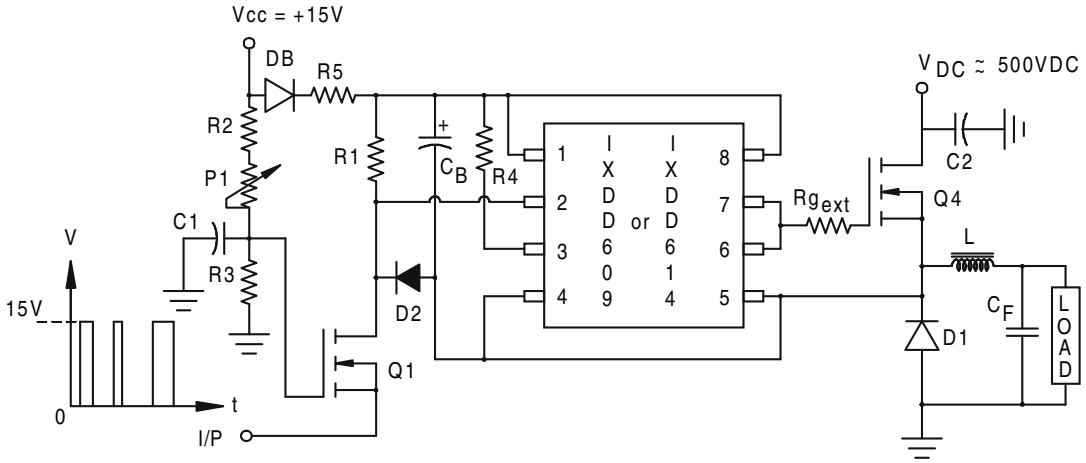


Figure 15 Basic Bootstrap Gate Drive Technique



Q1 : IXTU01N100
DB : DSEP9-06CR
D1 : DSEC60-12A
D2 : 1N5817
C1 : 20MFD,25V
C2 : 20MFD,1000 Volts,CSI 10DC0020
CB : 10MFD,25VDC
P1 : 5K Trim pot

Rgext: 1.0 Ohm to 4.7 Ohm
CF : GE A28F5601
0.1MFD,1000 Volts
R1 : 1K
R2 : 10K
R3 : 2K
R4 : 10K
R5 : 1 Ohm
L : 5µH,DALE IH-5

Figure 16 turn-off Enhancement Methods

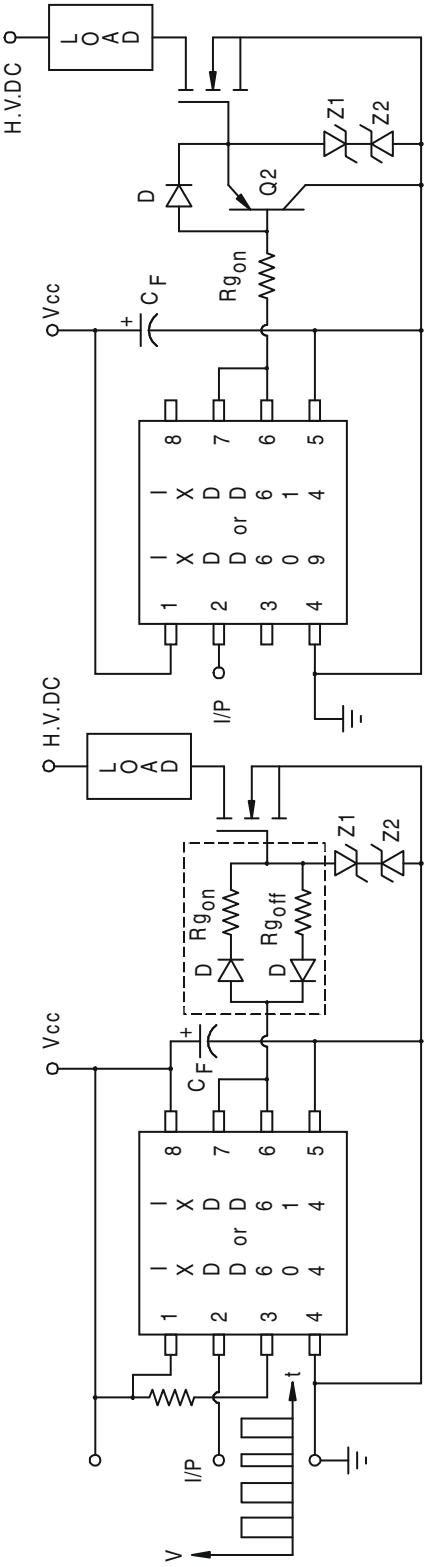


Figure 17 Technique To Boost Current Output and Provide -VE Bias To Achieve Faster turn-off For High Power MOSFET And IGBT Modules

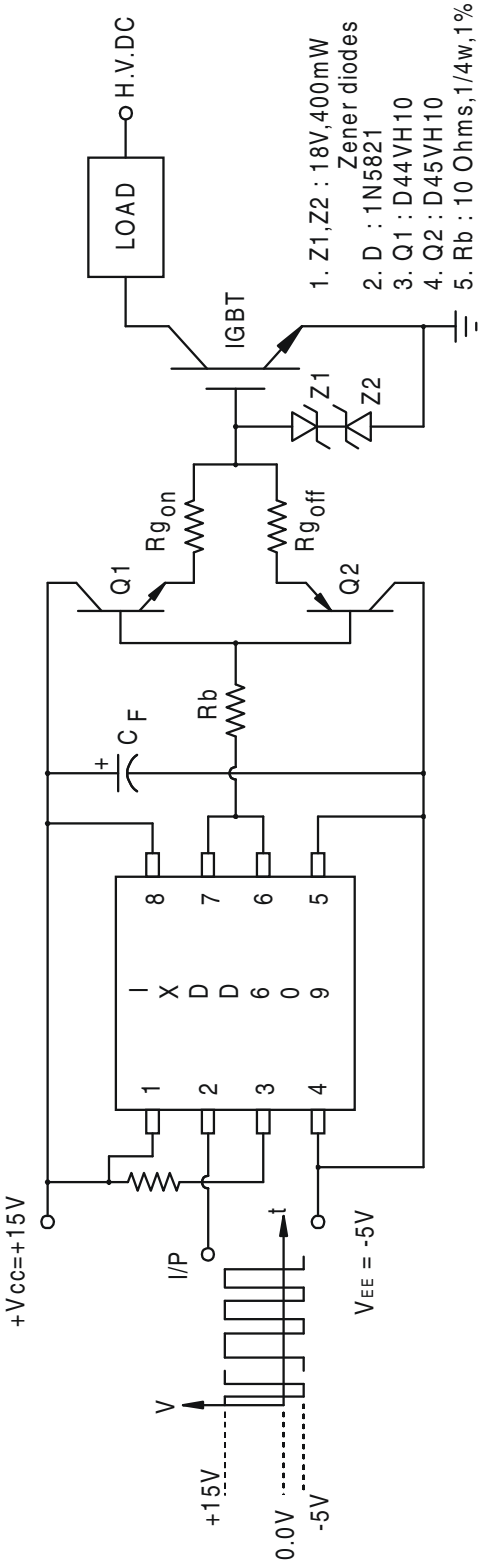
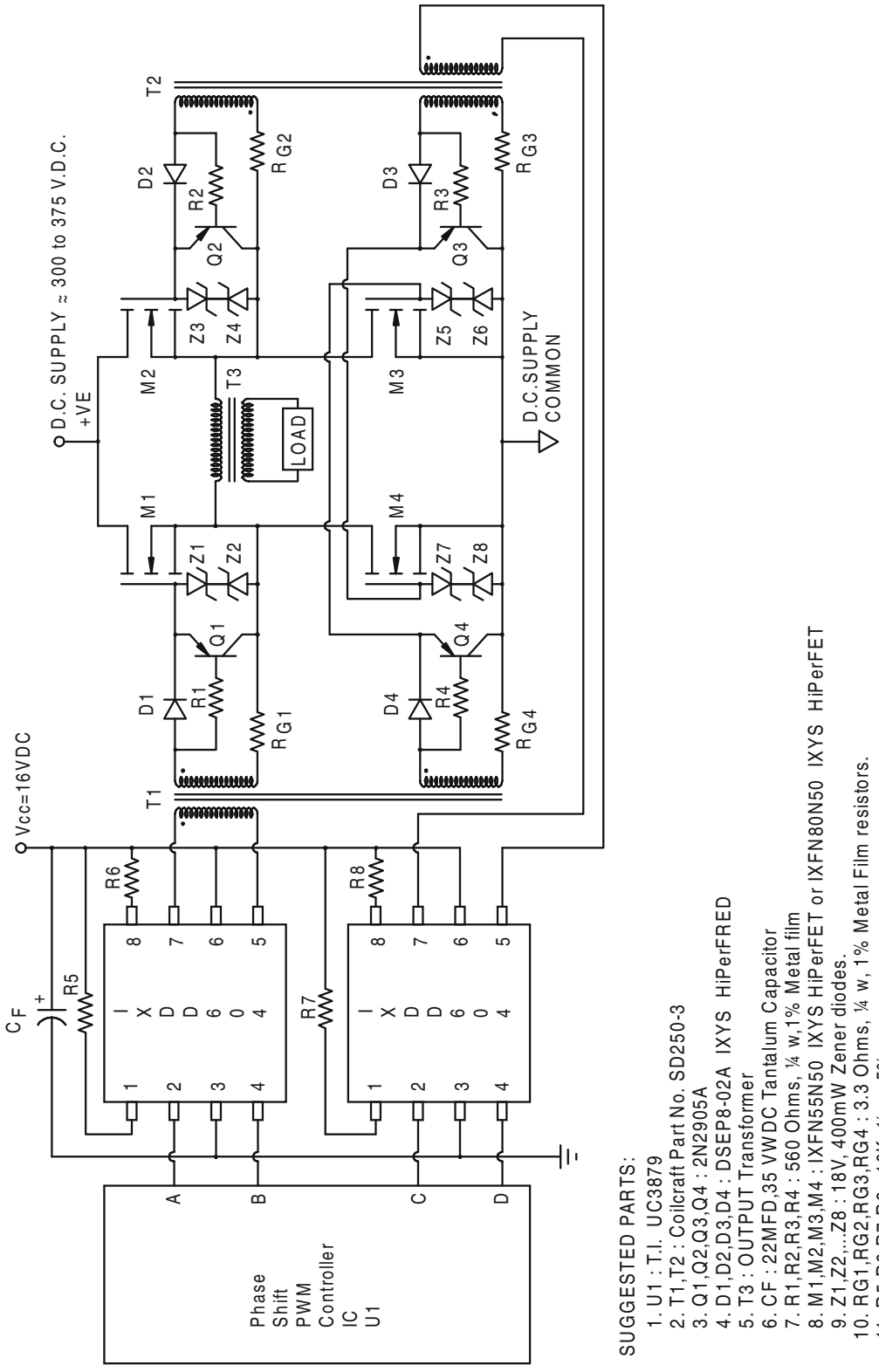


Figure 18 Transformer Coupled Gate Drive Arrangement For "H" Bridge In a Phase Shift PWM Controller at Fixed Switching Frequency



SUGGESTED PARTS:

1. U1 : T.I. UC3879
2. T1,T2 : Coilcraft Part No. SD250-3
3. Q1,Q2,Q3,Q4 : 2N2905A
4. D1,D2,D3,D4 : DSEP8-02A IXYS HiPerFRED
5. T3 : OUTPUT Transformer
6. CF : 22MFD,35 VWDC Tantalum Capacitor
7. R1,R2,R3,R4 : 560 Ohms, ¼ w,1% Metal film
8. M1,M2,M3,M4 : IXFN55N50 IXYS HiPerFET or IXFN80N50 IXYS HiPerFET
9. Z1,Z2,...Z8 : 18V, 400mW Zener diodes.
10. RG1,RG2,RG3,RG4 : 3.3 Ohms, ¼ w, 1% Metal Film resistors.
11. R5,R6,R7,R8 : 10K, ¼ w, 5%

Figure 19 3-Phase AC Motor Drive Schematic Showing How IXYS CBI (Converter-Brake-Inverter) Module Can Be Driven By IXDD614 Using Optocouplers - All Protection Features Are Incorporated

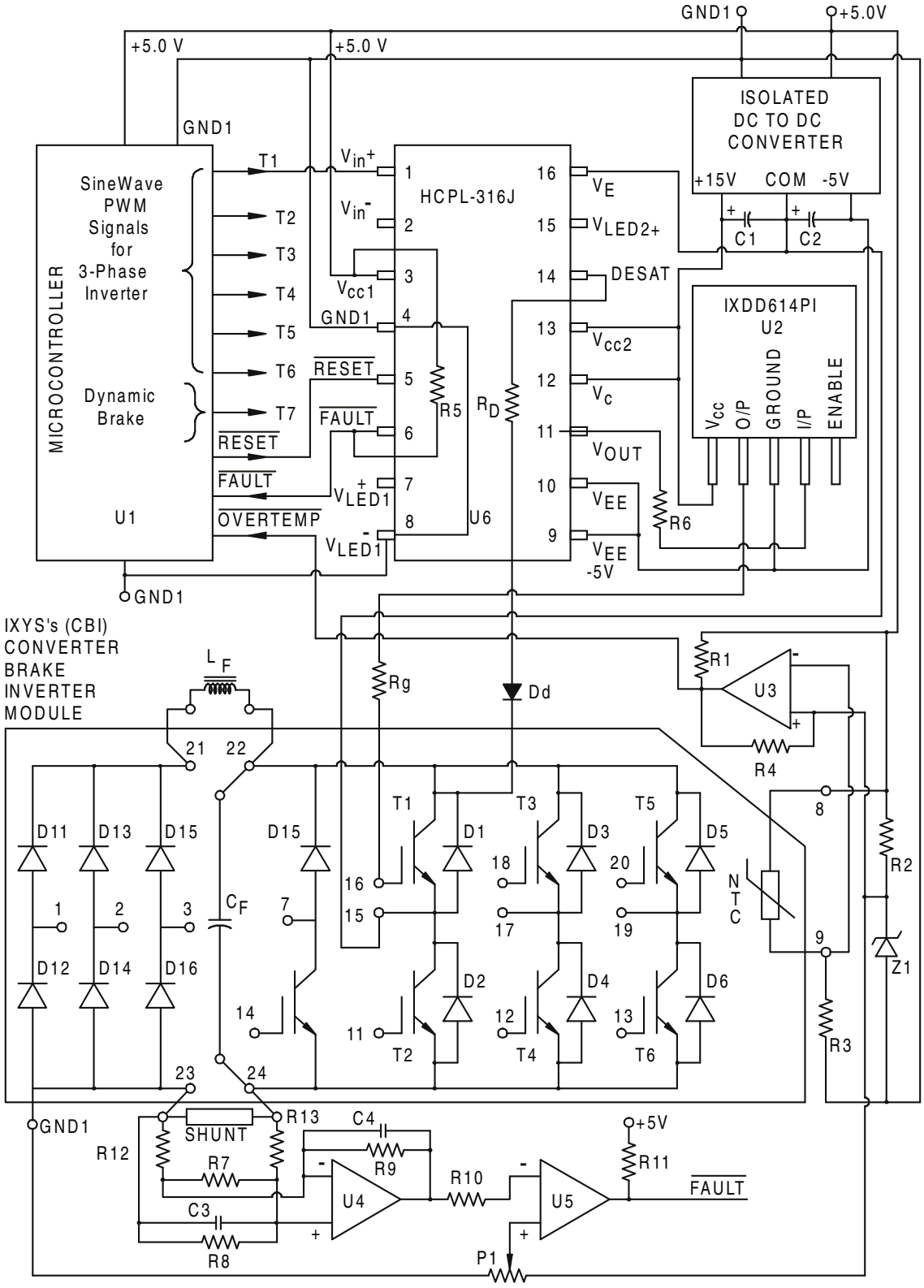
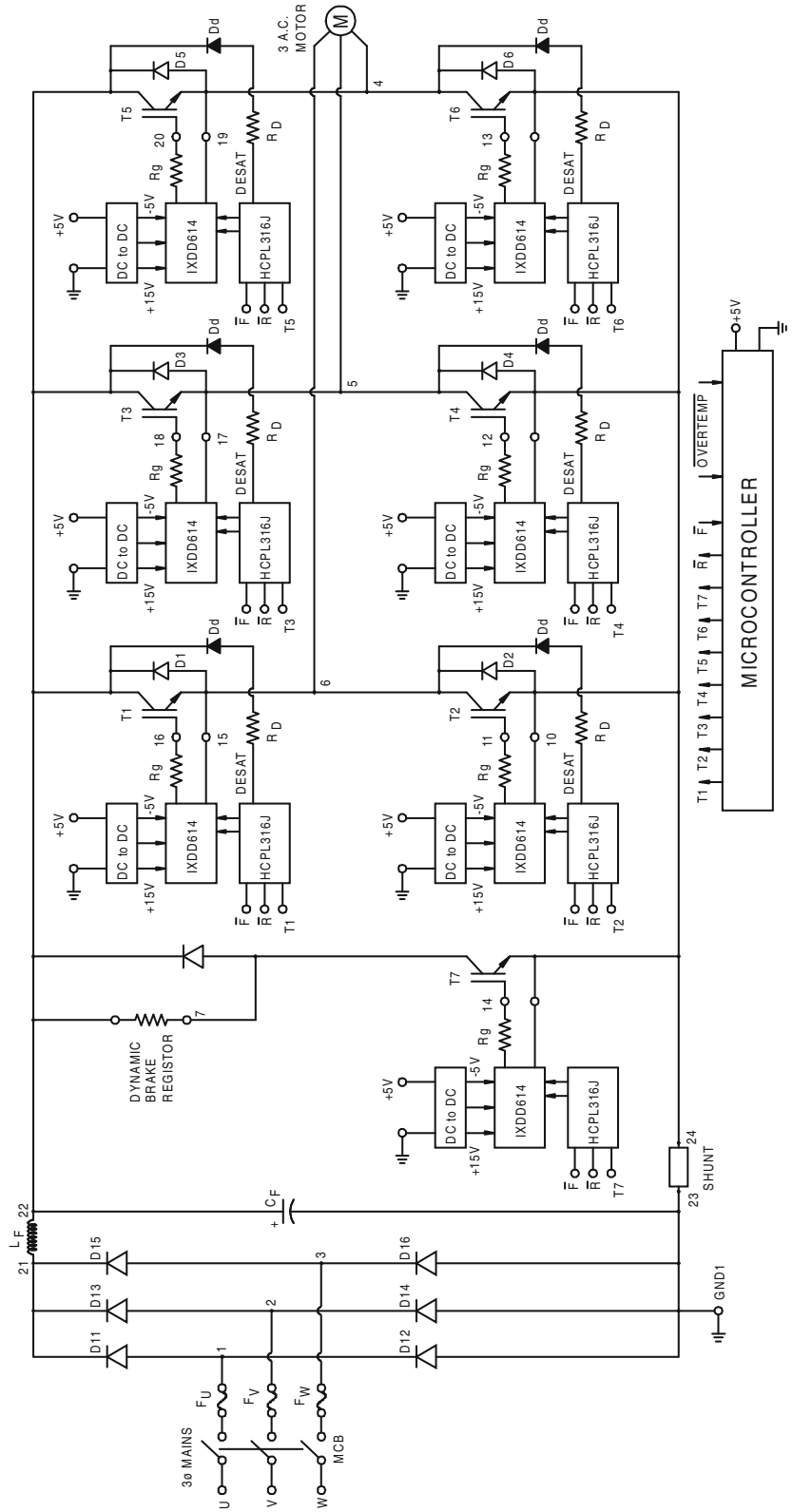


Figure 20 IXYS Converter, Brake Inverter (CBI) Module Being Driven By IXDD614 With Optocoupler and Desat, Overtemp, and Short Circuit/Overload Protections



NOTES: 1. ALL $\overline{F}$ = $\overline{FAULT}$ SIGNALS ARE TIED TOGETHER (BEING OPEN COLLECTOR) AND FED INTO MICROCOMPUTER.
2. ALL $\overline{R}$ = $\overline{RESET}$ SIGNALS ARE TIED TOGETHER AND FED TO HCPL-316J.
3. $\overline{OVERTEMP}$ AND OVERLOAD/SHORT CIRCUIT $\overline{FAULT}$ SIGNALS ARE GENERATED AS PER FIG(16)
$\overline{OVERTEMP}$ IS ALSO FED IN MICROCOMPUTER.

Bill of Materials for Figure 19 and Figure 20

Resistors:

R1: 10K, 1/4W, 1% MFR

R2: 560 Ohms, 1/4W, 1% MFR

R3: 10K, 1/4W, 1% MFR

R4: 2.2 MegOhms, 1/4W, 5%

R5: 10K, 1/4W, 1% MFR

R6: 100 Ohms, 1/4 W, 1% MFR

R7: 20K, 1/4W, 1% MFR

R8: 61.9K, 1/4W, 1% MFR

R9: 61.9K, 1/4W, 1% MFR

R10: 10K, 1/4W, 1% MFR

R11: 10K, 1/4W, 1% MFR

R12: 1.24K, 1/4W, 1% MFR

R13: 1.24K, 1/4W, 1% MFR

Rg: T.B.D. based on T_{on} , T_{off} , & size of IGBT

RD:100 Ohms,1/4 w, 5%

P1: 10K Trimpot, Bourns 3006P or Spectrol

SHUNT : 75 mV @ full load current

Capacitors:

C3, C4: 33 pF, silver dipped mica

CF: Electrolytic Filter Capacitor with very low ESR & ESL and screw type terminals to handle high ripple current. Voltage rating is based on DC Bus plus AC ripple Voltage

Diodes:

Dd: General Semiconductor make, RGP02-20E, 0.5A, 2000V, trr: 300ns

Zener Diodes:

Z1: Zener LM336, 2.5 Volt

Inductors:

LF: Gapped DC Choke for filtering rectified power

Semiconductors:

U3: LM339 Comparator

U4 : LM-101 Op Amp

U5: LM339 Comparator

CBI Module: IXYS Corporation Type Nos: MUBW 50-12A8 or any MUBW module from CBI 1, CBI 2 or CBI 3 series

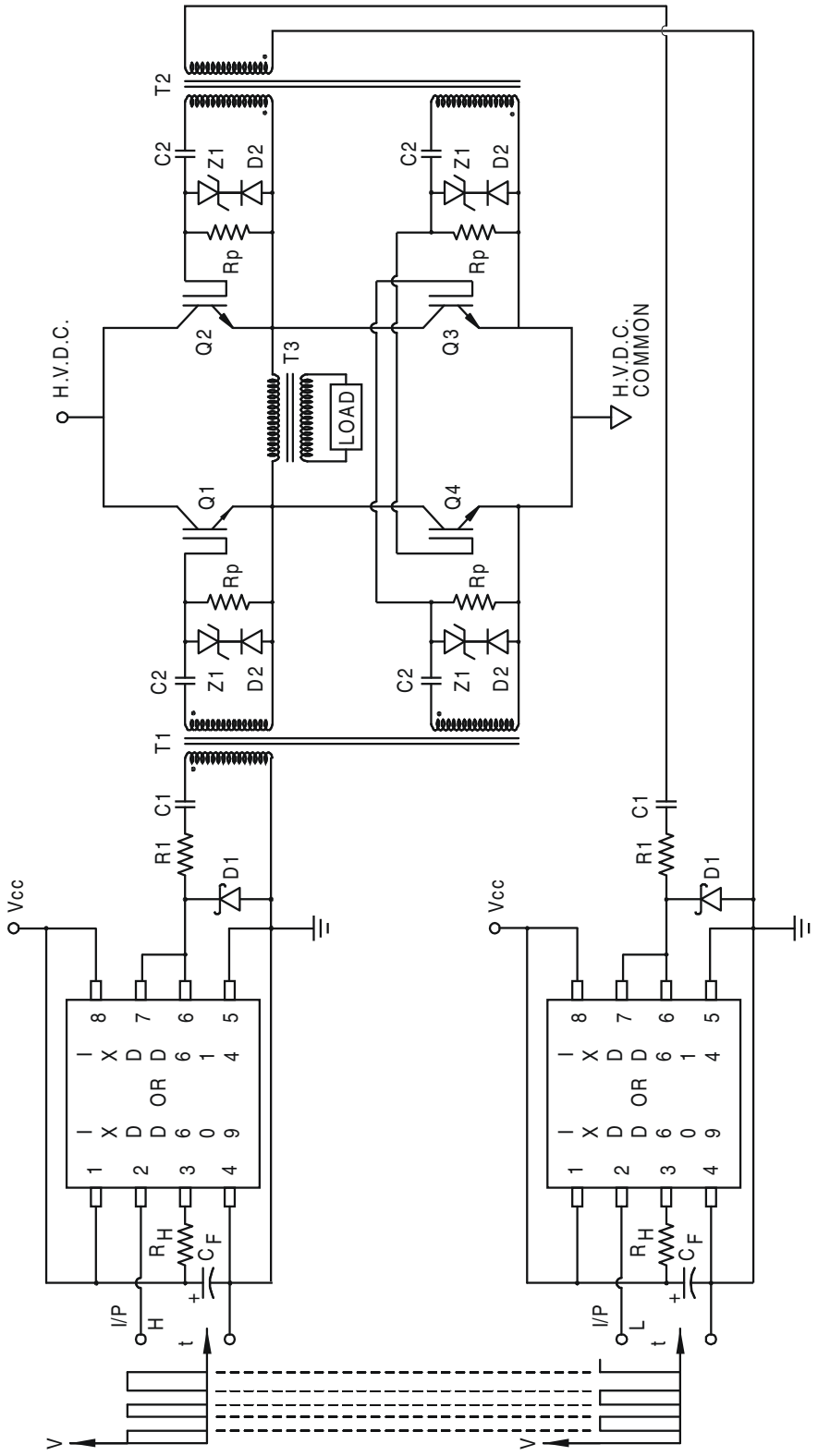
Microcontroller: T.I. TMS320F240 with embedded software for AC Drive, using brake feature.

IXDD614 Driver chip: 7 required to implement A.C.Drive, using Brake feature

HCPL316J(Optocoupler) : 7 required to implement A.C.Drive With Brake feature.

Isolated DC to DC Converter: 7 required with specified isolation.

Figure 21 IXYS Converter, Brake Inverter (CBI) Module Being Driven By IXDD614 With Optocoupler and Desat, Overtemp, and Short Circuit/Overload Protections



For additional information please visit our website at: www.ixysic.com

Specification: AN-401-R02

12/13/2012