Objectives

This document outlines the specific product features of the ISOPLUS™ power semiconductor family. **Figure 1** displays some of the family's packages.

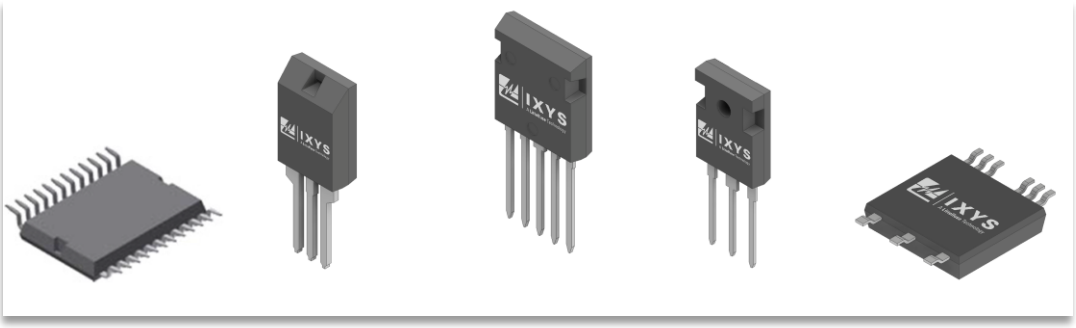

Figure 1. ISOPLUS™ Packages SMPD-DIL, TO-220, TO-247, I4-Pac and SMPD-B

Applications

- Industrial drives
- EV-charging
- White Goods
- Power Supplies
- Renewable energies

Target Audience

This document is intended for all power electronic developers confronted with hardware design and the challenge to build reliable systems with a focus on reasonable effort in component choice, layout, and thermal management.

Contact Information

For more information on this topic, contact the Littelfuse Power Semiconductor team of product and applications experts:

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- Central & South America – CSA_PowerSemi_Tech@Littelfuse.com
- Europe. Middle East, & Africa – EMEA_PowerSemi_Tech@Littelfuse.com
- Asia, Australia, & Pacific Islands – APAC_PowerSemi_Tech@Littelfuse.com

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1. Introduction

When using power semiconductors, there is usually a need to electrically isolate the devices from the heatsink, which could also be the equipment's chassis or housing. The main reasons for this are safety, the necessity to reduce electromagnetic interference by reducing stray capacitance between the chip and ground, and the desire to mount several devices onto the same heatsink.

Major penalties involve increased thermal resistances, complex assembly, and difficulty in testing of the insulation quality to meet different global safety standards. The most common method is to use an insulating material, sandwiched between the semiconductor device and the heatsink. Inherently, this increases the thermal resistance case-to-heatsink R_{thcs}.

Implementing discrete power semiconductors by adapting technologies from power modules led to the development of the ISOPLUS™ family. Here, a combination of insulating carriers with copper lead-frames and bond-wire interconnection enables an internal construction that achieves high insulation strength without sacrificing thermal performance.

This application note describes the major properties for the ISOPLUS™ Family.

2. Power Device

The ISOPLUS™ family today consists of a variety of different packages that all feature the same approach regarding internal construction and insulation. Being a power semiconductor platform, ISOPLUS™ family members are available in a wide range of technologies, topologies, and voltage classes.

3. Mechanical Construction

The key engineering achievement is the extension of the common copper lead frame by a copper-ceramic-copper laminate called Direct Copper Bonding or DCB. The ceramic itself can withstand an insulation voltage higher than 6 kV but for the ISOPLUS™-family, it is rated to 2.5 kV with respect to the external creepage and clearance distances of the package. The semiconductors are soldered to the structured DCB-frontside while the opposite side of the substrate is used for direct mounting to a heatsink. Interconnections of the chips is done using bond-wires. As an example, the cross section of the ISOPLUS™ SMPD package is displayed in **Figure 2**.

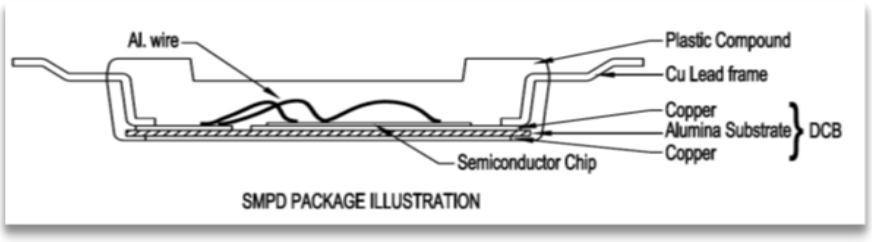

Figure 2. Cross-section of an ISOPLUS™ Device

The total number of layers from the heat source to the heatsink has been minimized to only one solder layer, the DCB ceramic and an external thermal grease. This results in a very low thermal resistance between chip and heatsink. Soldering the chip onto the DCB substrate that includes an insulator is a well-proven method for chip attachment and widely used in power semiconductor modules.

A common feature of all ISOPLUS™ devices is the hole-free package. In addition to the improvements in thermal performance, the area consumed by the mounting hole can now be utilized too.

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4. Comparing the Thermal Situation

In contrast to traditional lead-frame-based packages with electrically active backsides, all members of the ISOPLUS™-family can be mounted to a heat sink by simply adding a high-performance Thermal Interface Material (TIM). Though these materials are available qualified as electrically non-conductive, this may not be misinterpreted as offering a qualified insulation strength. Applied to achieve a thin bond line between the power electronic component and the heat sink, a direct metal-to-metal contact cannot be excluded. From a thermal transfer point of view, maximizing this contact is beneficial as direct metal contacts provide the lowest possible thermal resistance. With non-insulated devices, this connection could lead to unwanted, potentially hazardous effects and needs to be prevented. As an isolator is needed between an active part and the heat sink, the chain of thermal resistances involved is unnecessarily prolonged.

Inherently, the thermal transfer capability of the connection is reduced.

Figure 3 sketches the setup as well as the chain of thermal resistances using an ISOPLUS™ device in combination with grease as thermal interface material.

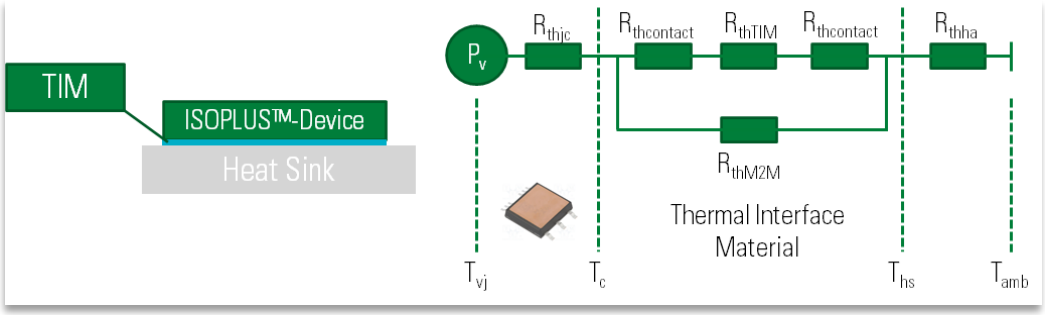

Figure 3. Thermal Model of an Isolated Package using Thermal Grease

The thermal resistance from junction to case R_{thjc} is defined by the solid construction of the power semiconductor. The path from the device's case to the heat sink's surface R_{thch} depends on the thermal interface in use. It's bulk resistance R_{thTIM} is typically given in the datasheet. Equally important is the material's capability to contact the surfaces to reduce the contact resistances $R_{thcontact}$ and allow a direct metal-to-metal path R_{thM2M}.

In comparison, a material with a guaranteed insulation strength changes the setup as inherently the metal-to-metal contact is eliminated. **Figure 4** depicts the difference, assuming a soft insulation layer like a silicone pad.

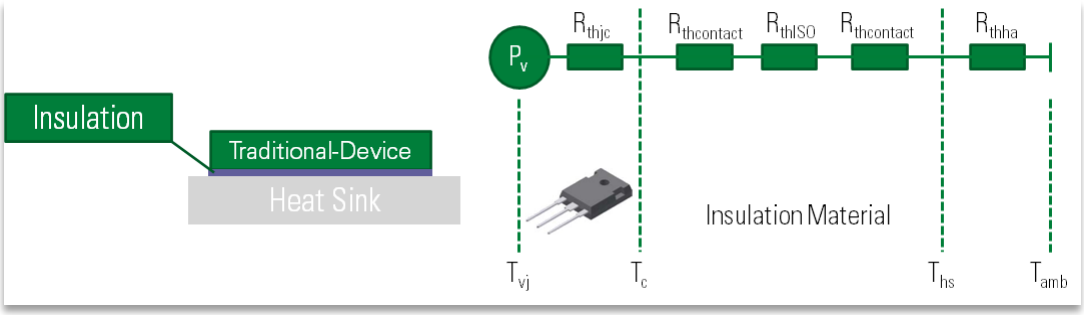

Figure 4. Thermal Model of a Non-insulated Package using a Silicone Pad

Without the metal-to-metal contact, a highly efficient part of the thermal chain is missing. Additionally, the contact resistance as well as the material's bulk resistance are higher than those of high-performance thermal greases, leading to lower thermal performance of the structure.

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Replacing the soft material with a higher performance version like ceramic sheets further worsens the situation. These hard materials do not offer low contact resistances. A thermal grease needs to be used on both sides of such platelets, unnecessarily increasing the thermal resistance further, as seen in **Figure 5**.

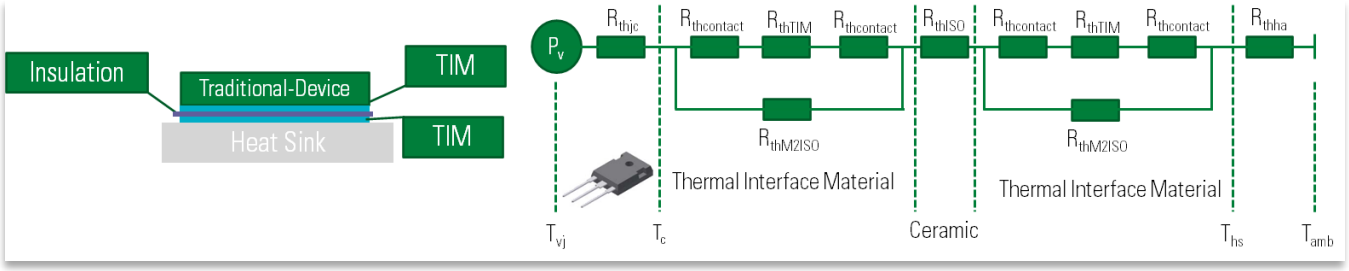

Figure 5. Thermal Model of a Non-insulated Package using a Ceramic Platelet and Thermal Grease

The improved thermal performance turns into higher electrical performance, as summarized in the diagram given in **Figure 6.**

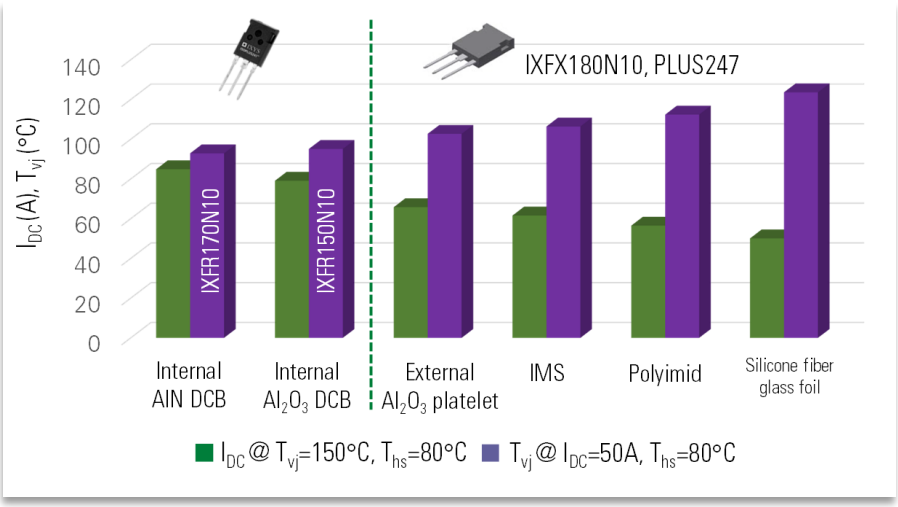

Figure 6. Comparing Electrical Performance of ISOPLUS™ 274 and PLUS247™ Devices

The PLUS247™ package is derived from the standard TO-247 and shares the same mechanical construction. To allow larger dies inside the package, no mounting hole is present in this package. Though the device used for this comparison holds the larger die inside, the DC-current achieved at maximum junction temperature is lower, compared to a smaller die in the ISOPLUS-setup. Vice versa, at the same chip current, the chip temperature is lower within the ISOPLUS-device, leading to a gain in device lifetime.

5. Assembly Benefits

Traditional devices with an active backside require insulation as described in case all devices involved are mounted on the same heat sink. Instead, another approach consists of designs that group components with the same collector-potential to a common heat sink. This allows for improvement of the thermal situation but leads to other drawbacks. In a classical sixpack, this requires having four dedicated heat sinks that in turn need to remain insulated from each other. In more complex structures, this leads to an unnecessary number of heat sinks and inconvenient assembly processes.

Because of the insulated construction, multiple ISOPLUS™-devices can be mounted on a common heat sink. Correlating mounting suggestions can be found in the application note *Mounting and Cooling Solutions for SMPD Packages*.

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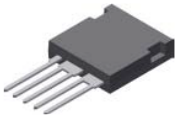
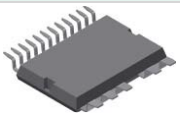
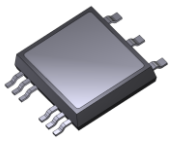
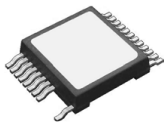
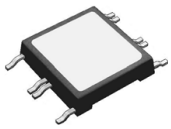
6. Available Packages

Since the introduction of the ISOPLUS™ family back in 1998, additional packages have been added, as pictured in **Table 1**.

Table 1. The ISOPLUS Family Members

Overview on the ISOPLUS-Family		
		
ISOPLUS220™	ISOPLUS247™	ISOPLUS264™
		
ISOPLUS I4-PAC™	ISOPLUS I4-PAC™	ISOPLUS I4-PAC™
		
ISOPLUS264™	ISOPLUS-DIL™	ISOPLUS-DIL™
		
ISOPLUS-SMPD™-B	ISOPLUS-SMPD™-X	ISOPLUS-SMPD™-Y

In each package, a variety of technologies, topologies, and voltage classes is available. The most recent information can be found in the Power Semiconductor Product Catalog. The file can be downloaded from the Technical Resources page on the Littelfuse website.

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Revision	Date	Major work done
1.0	2001	IXYS AN0025 on the ISOPLUS™
21.09a	2021	Reworked and updated

For additional information please visit www.Littelfuse.com/powersemi

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IXYS

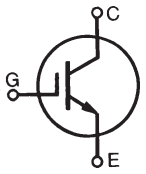
Preliminary Technical Information

High Voltage IGBTs

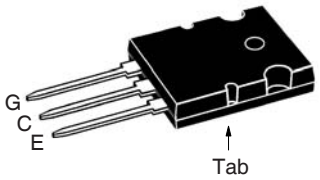
IXGK75N250
IXGX75N250

V_{CES} = 2500V
I_{C110} = 75A
$V_{CE(sat)} \leq$ 2.7V

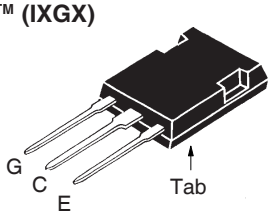
For Capacitor Discharge Applications



TO-264 (IXGK)



PLUS247™ (IXGX)



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capability)	170	A
I_{C110}	T_C = 110°C	75	A
I_{LRMS}	T_C = 25°C (Lead RMS Limit)	160	A
I_{CM}	T_C = 25°C, V_{GE} = 20V, 1ms	530	A
SSOA (RBSOA)	V_{GE}= 15V, T_{VJ} = 125°C, R_G = 1Ω Clamped Inductive Load	I_{CM} = 200 @ 0.8 • V_{CES}	A
P_C	T_C = 25°C	780	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
M_d	Mounting Torque (IXGK)	1.13/10	Nm/lb.in.
F_C	Mounting Force (IXGX)	20..120/4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

G = Gate E = Emitter
C = Collector Tab = Collector

Features

- Very High Peak Current Capability
- Low Saturation Voltage
- MOS Gate Turn-On
- Rugged NPT Structure
- Molding Epoxies meet UL 94V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Capacitor Discharge
- Pulser Circuits

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{CE} = 0V	2500			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	μA
	T_J = 125°C			5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	I_C = 75A, V_{GE} = 15V, Note 1			2.7	V
	I_C = 150A			3.6	V

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Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	35	58	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		9000	pF
C_{oes}			345	pF
C_{res}			110	pF
Q_g	I_C = 75A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		410	nC
Q_{ge}			63	nC
Q_{gc}			175	nC
$t_{d(on)}$	**Resistive Switching Times**		55	ns
t_r	I_C = 150A, V_{GE} = 15V		225	ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 1Ω		270	ns
t_f			455	ns
R_{thJC}				0.16 °C/W
R_{thCK}			0.15	°C/W

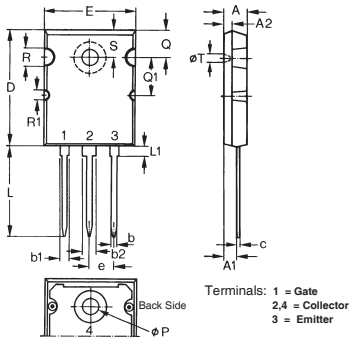
Note 1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.

*Additional provision for lead-to-lead voltage isolation are required at V_{CE} >1200V.

PRELIMINARY TECHNICAL INFORMATION

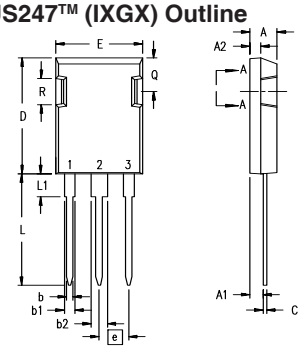
The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

TO-264 AA (IXGK) Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

PLUS247™ (IXGX) Outline



Terminals: 1 - Gate
2 - Collector
3 - Emitter

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25ºC

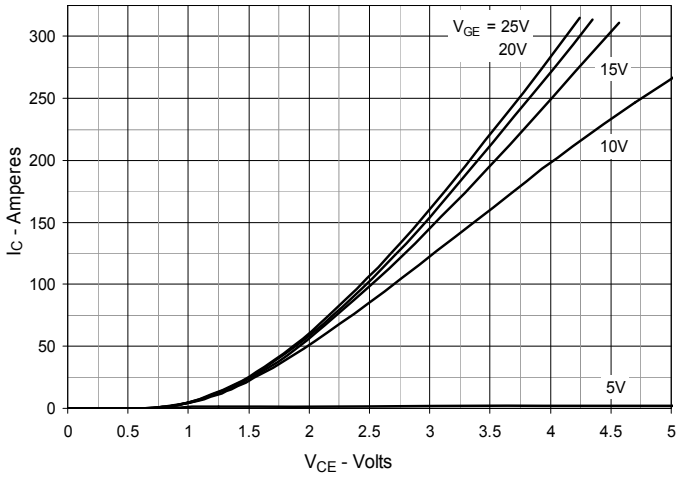


Fig. 2. Output Characteristics @ T_J = 125ºC

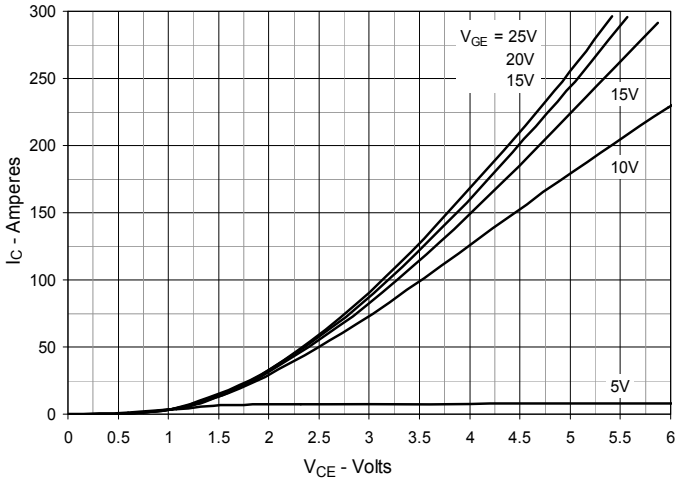


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

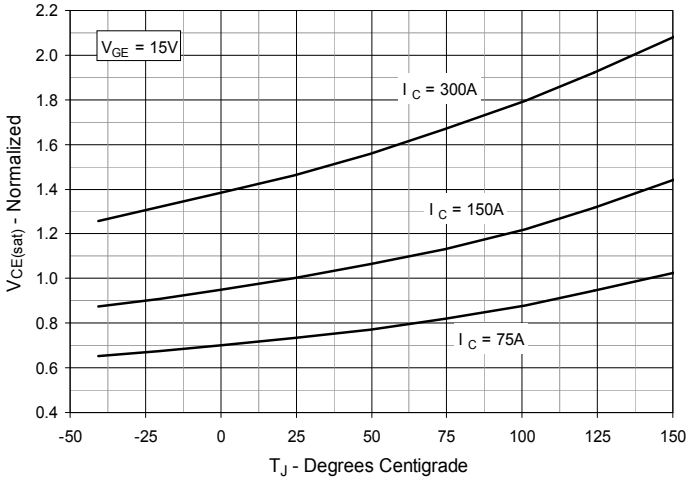


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

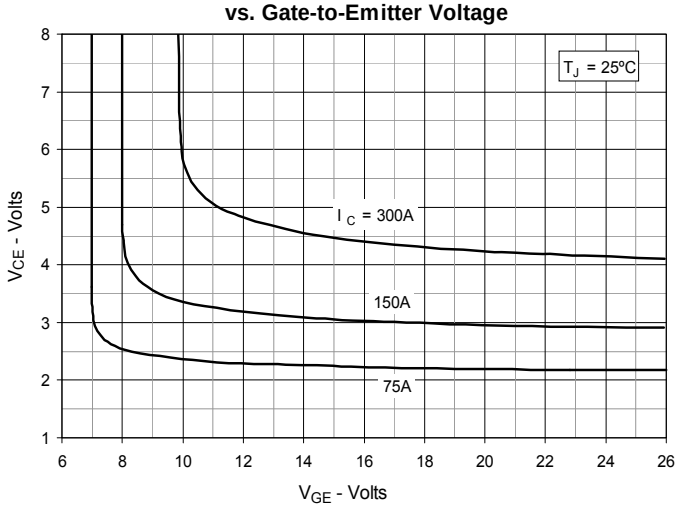


Fig. 5. Input Admittance

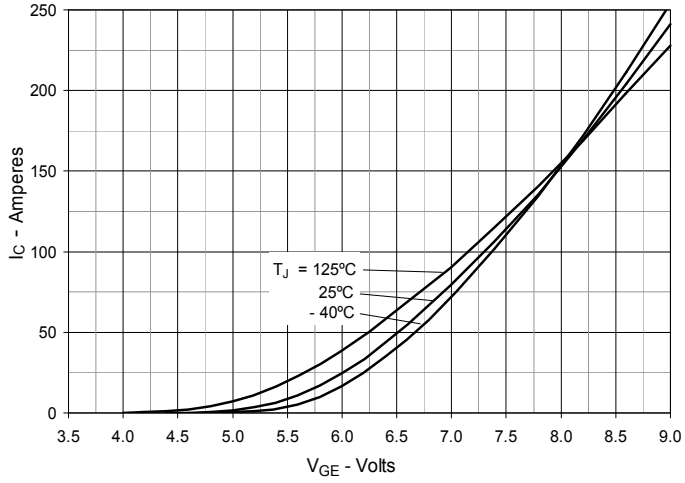


Fig. 6. Transconductance

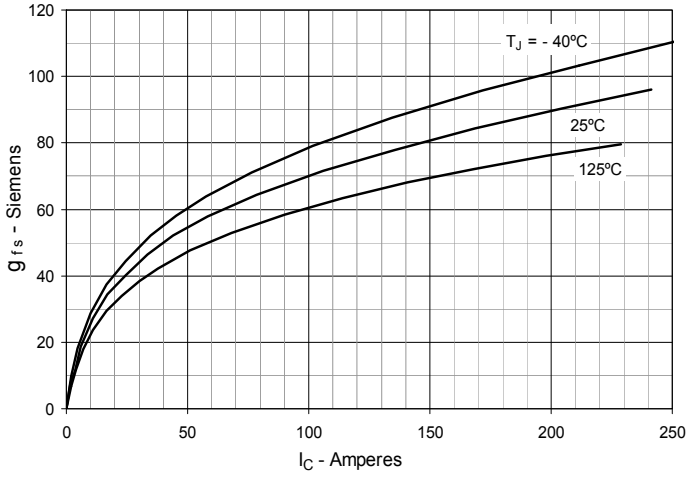


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Fig. 7. Gate Charge

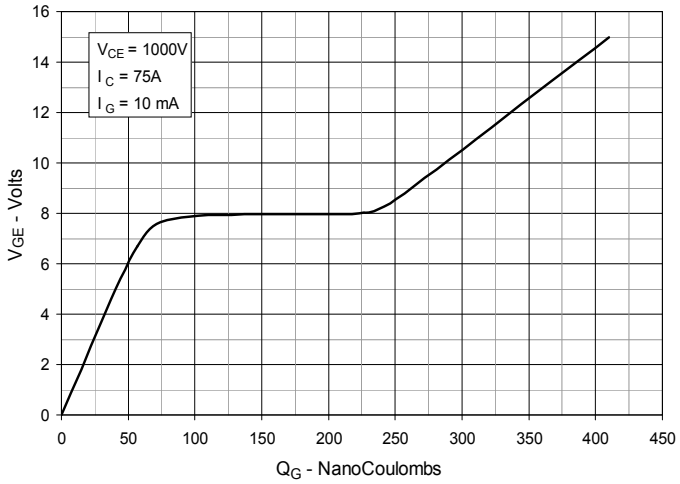


Fig. 8. Capacitance

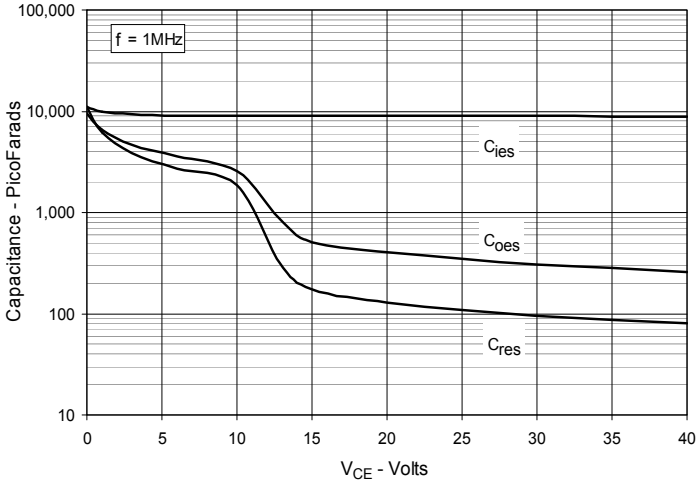


Fig. 9. Reverse-Bias Safe Operating Area

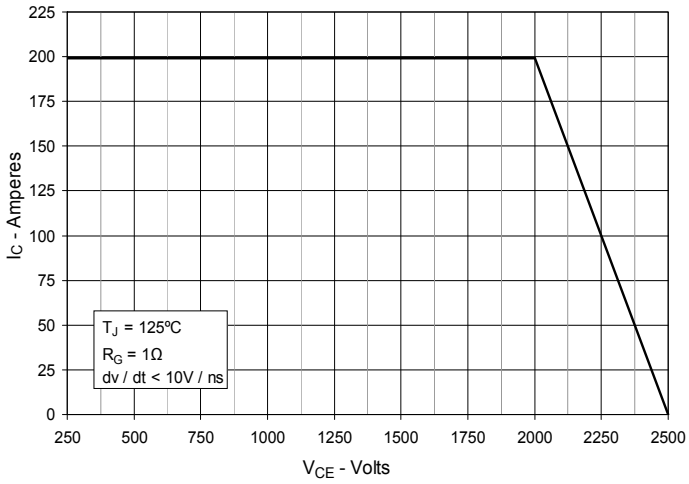


Fig. 10. Maximum Transient Thermal Impedance

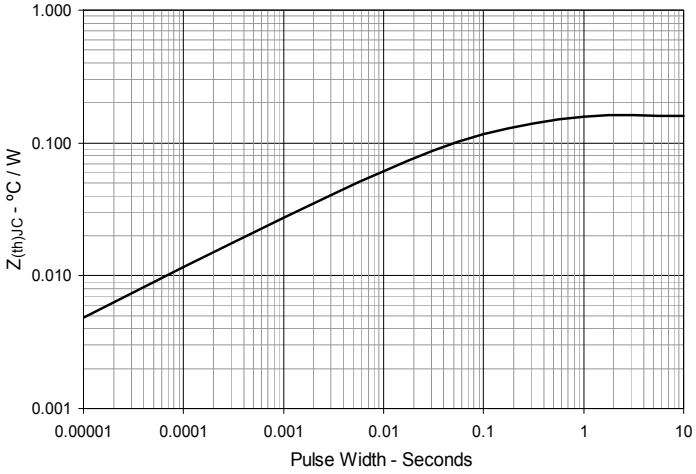


Fig. 11. Resistive Turn-on Rise Time vs. Junction Temperature

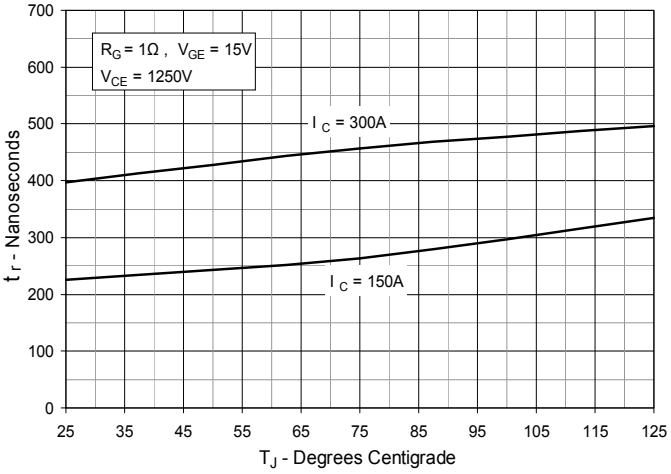


Fig. 12. Resistive Turn-on Rise Time vs. Collector Current

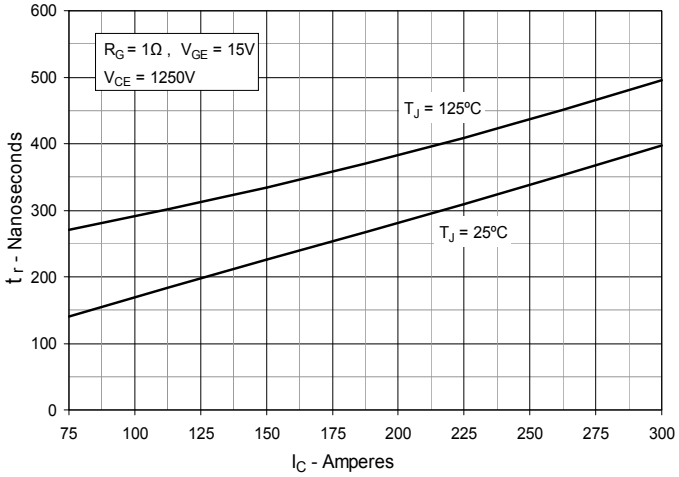


Fig. 13. Resistive Turn-on Switching Times vs. Gate Resistance

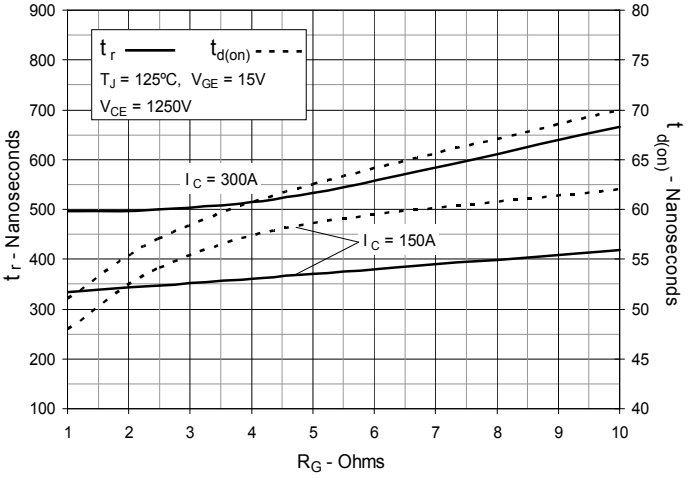


Fig. 14. Resistive Turn-off Switching Times vs. Junction Temperature

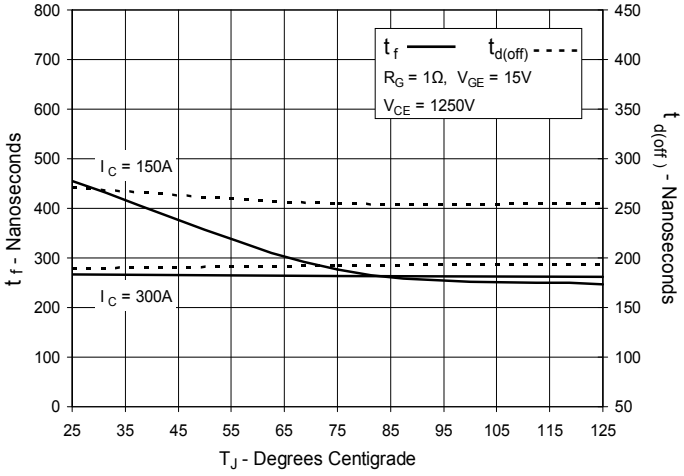


Fig. 15. Resistive Turn-off Switching Times vs. Collector Current

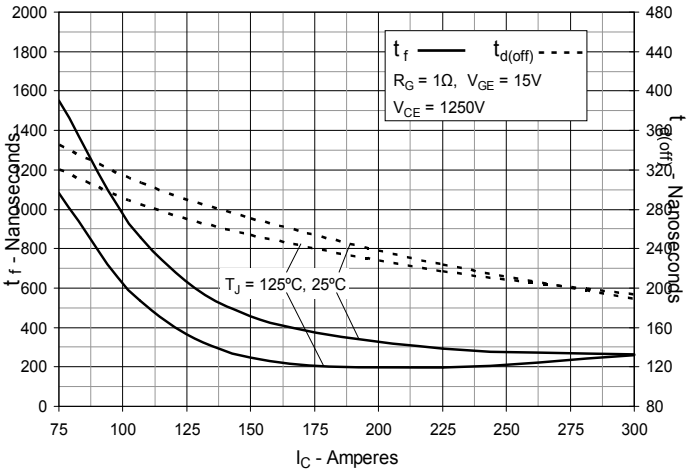
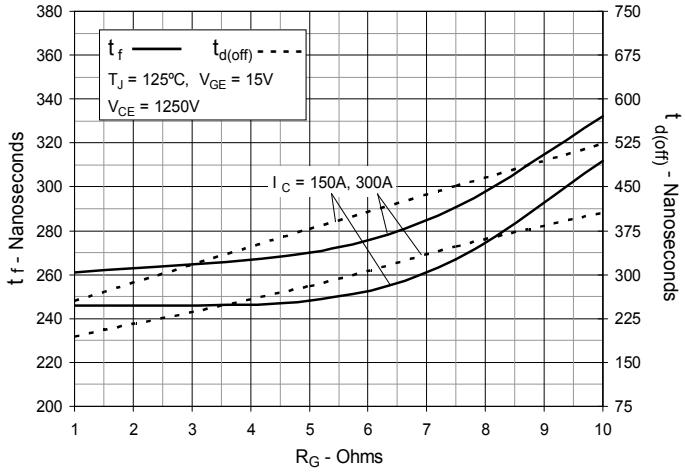


Fig. 16. Resistive Turn-off Switching Times vs. Gate Resistance



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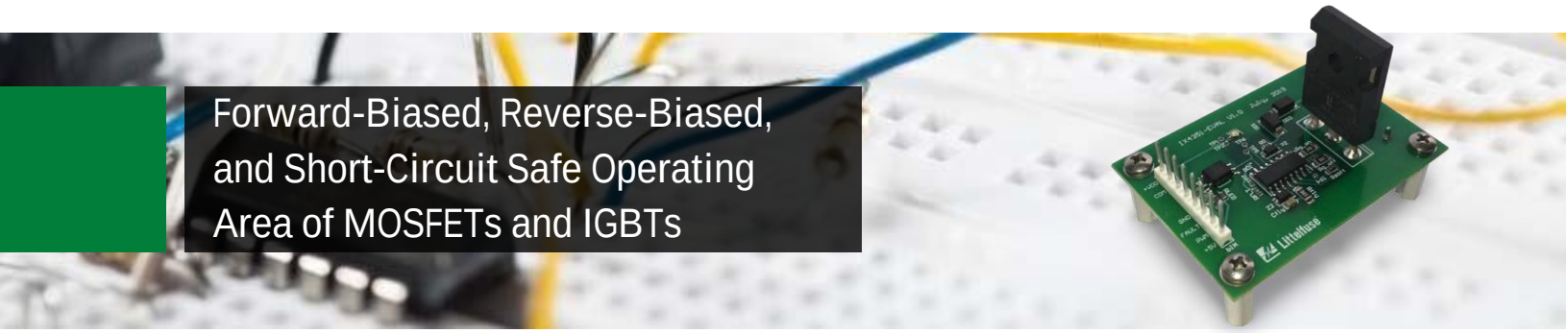

Forward-Biased, Reverse-Biased, and Short-Circuit Safe Operating Area of MOSFETs and IGBTs

Objectives

This document explains the operating conditions that a power semiconductor is supposed to work in without being damaged. Focus is set on the *Forward-Biased Safe Operating Area* (FBSOA), the *Reverse Biased, Safe Operating Area* (RBSOA) and the *Short-Circuit Safe Operating Area* (SCSOA).

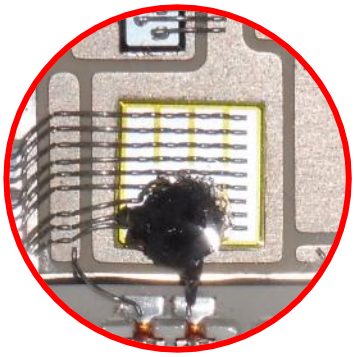

Figure 1. To be prevented – an IGBT destroyed by RBSOA-exceedance

Applications

The information compiled in this document is relevant for the power semiconductor itself and thus for all its applications.

Target Audience

This document is intended for all developers, design- and test-engineers involved in building power semiconductor applications.

Contact Information

For more information on the topic of safely operating power devices, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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Introduction

Power semiconductors like IGBTs, GTOs, thyristors, diodes, or bipolar junction transistors (BJT) have been developed into robust and reliable devices which can by now handle power levels into the MW-range and even beyond.

Despite these developments, they all have physical limitations which need to be known and respected to prevent damage to these components and the system they are mounted in. Depending on the instantaneous mode of operation, different conditions are described by a varying set of parameters, often referred to as operating area.

1. Safe Operating Area (SOA), also called Forward-Bias Safe Operating Area (FBSOA)

When a power semiconductor like an IGBT is used to conduct current in the predestined direction, the physical limits of the device to be considered include:

- the maximum collector current I_C,
- the saturation voltage V_{CEsat} across the device,
- the power generated by the product $I_C \cdot V_{CEsat}$, and
- the maximum junction temperature T_{VJ} allowed.

In cases where the power semiconductor is a MOSFET, dedicated to be operated in linear mode, the current can be influenced by tuning the gate-source-voltage accordingly. As a consequence, the drain-source-voltage V_{DS} of the devices changes which in turn impacts the losses. The device must dissipate these losses and the thermal impedance of the device poses the limits here.

For these operating conditions, the FBSOA-diagram features the forward voltage, the current and limits imposed by thermal development. Looking at Figure 2, it becomes obvious that growing losses can only be tolerated for shorter periods of time.

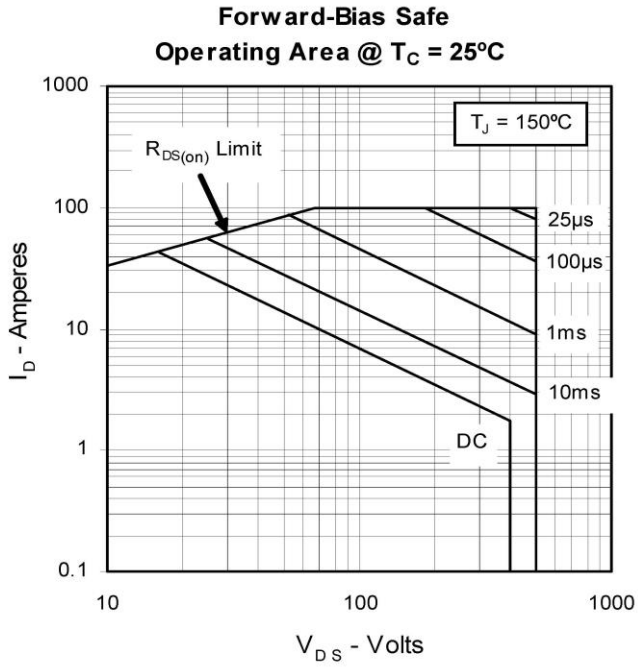

Figure 2. SOA Diagram for the IXTX46N50L

Any combination of forward voltage and current that is found below the correlating lines within the diagram is a legal point of operation as long as the junction temperature remains below the maximum limit and the duration of the loading is properly chosen. De-rating must be considered if the case temperature is different from the 25°C the diagram in Figure 2 refers to.

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2. Reverse Biased Safe Operating Area (RBSOA)

Power semiconductors like IGBTs or MOSFETs can turn off a current rather quickly but not at infinite speed. As the switching procedure does take some time, transient phenomena happen that need to be considered.

During this short period, when the device turns from conducting into blocking mode, the Reverse Biased Safe Operating Area needs to be respected at any time.

The limits are given by the current which is turned off and the voltage that appears across the device. The plot in Figure 3 schematically displays a turn-off event in detail.

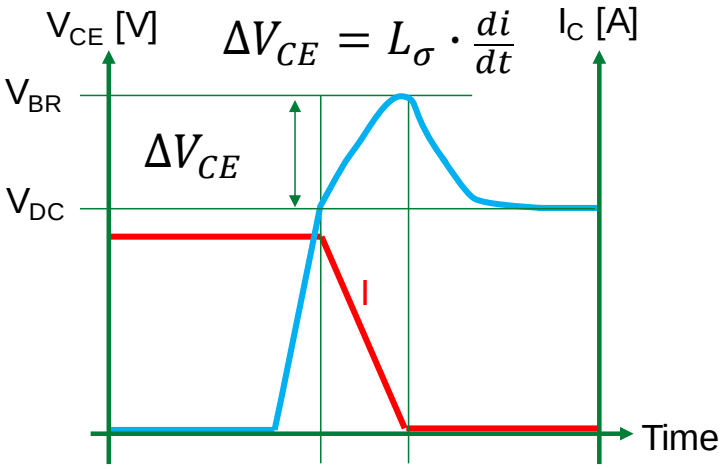

Figure 3. Voltage and current waveforms during a turn-off event

In the graph, it can clearly be seen that the voltage across the device first reaches the DC-link's voltage level before the current starts declining. Because of the current change rate di/dt and the inherently contained stray inductances L_σ, the voltage spike ΔV_{CE} is added on top of the DC-link voltage. If this spike exceeds the device's breakdown voltage V_{BR} – even for a very short period of time – the device will be destroyed.

The square-shaped Reverse Biased Safe Operating Area therefore is given by maximum current $I_{C,max}$ and the breakdown voltage V_{BR}, as depicted in Figure 4. Here too, the junction temperature poses a further limit.

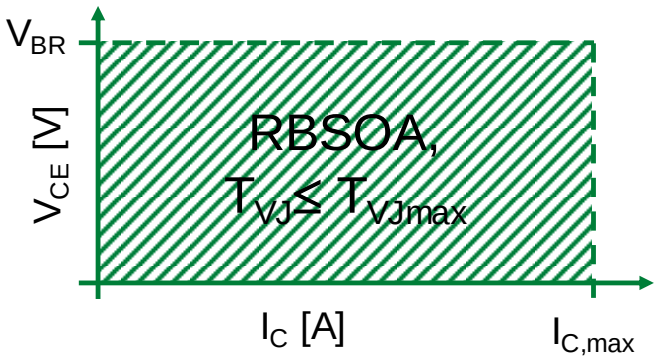

Figure 4. RBSOA-shape, limited by maximum current and breakdown voltage

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3. Short-Circuit Safe Operating Area (SCSOA)

Devices that feature desaturation, like most IGBTs, can withstand short-circuit events for a distinct duration. Corresponding datasheets highlight this information as Short Circuit Safe Operating Area or SCSOA. Such a datasheet's excerpt is given in Figure 5.

SCSOA	*short circuit safe operating area*	V_{CEK} = 1200 V					
t_{sc}	*short circuit duration*	V_{CE} = 720 V; V_{GE} = ±15	T_{VJ} = 125°C			10	µs
I_{sc}	*short circuit current*	R_G = 6.8 Ω; non-repetitive			450		A

Figure 5. SCSOA information taken from the MDMA280UB1600PTED datasheet

The short circuit condition demands that the IGBT goes into desaturation. In this mode, no further charge carriers remain available which also limits the current. Typically, IGBTs limit the short-circuit current to about three to four times their rated current. In the example in Figure 5, the 160 A-device is expected to limit the short circuit current to 450 A. This situation is tolerable for 10 µs only and limited by thermal development.

4. Resulting challenges for the designer

Combining the two areas for Reverse Biased Safe Operation and Short Circuit Safe Operation into a single diagram reveals a gap between them, as pictured in Figure 6.

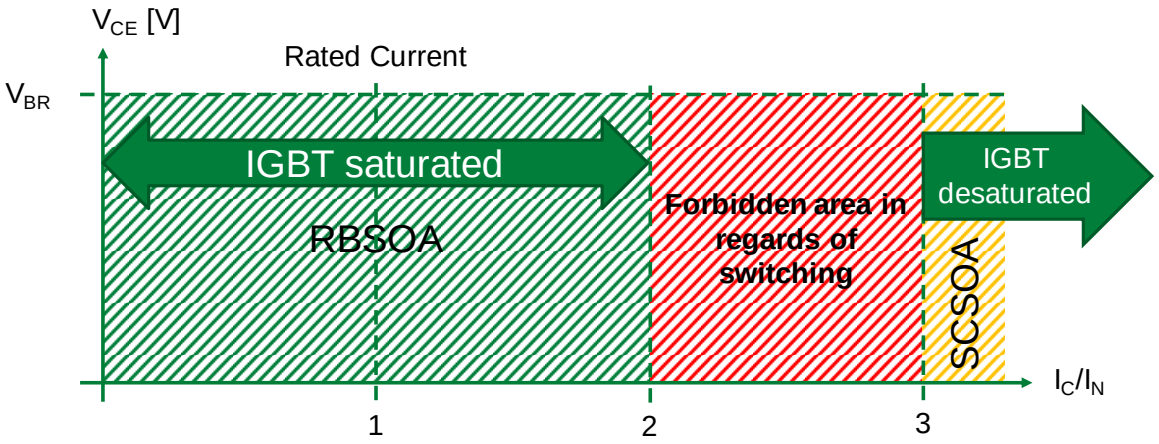

Figure 6. RBSOA, SCSOA, and the undefined region in between

Within the gap marked as forbidden area, located between twice and three times rated current, turning off the device is not allowed as it may lead to its destruction. The root cause of the destruction is found in very high local current densities, transiently forming during switching. The thermal limits in that case are reached already and additional burden due to switching losses leads to exceeding the limits. In turn, single cells on the chip fail and create a connection between collector and emitter. The current can no longer be turned off and the damage grows.

To overcome this situation, techniques to ensure that the IGBT reaches desaturation mode and enters the SCSOA can be used. The simplest way is to wait, instead of reacting on an overcurrent too quickly. Implementing a certain dead-time and fully exploit the 10 µs that the IGBT can withstand the conditions is a valid approach.

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Further methods include the so-called 2-Level turn-off. The device is not turned off by immediately cancelling or even reversing the gate-emitter voltage. Instead, the gate-emitter voltage is first reduced to minimize the number of charge carriers available for current transport. This speeds up reaching the desaturation stage. A few microseconds later, when desaturation is reached, the gate-emitter voltage is set to zero or reversed. The device is then safely turned off within the SCSOA-specification.

This fact becomes particularly important when handling overcurrent situations.

From a given setup, measurements from a destructive turn-off event seen in Figure 7 were analyzed:

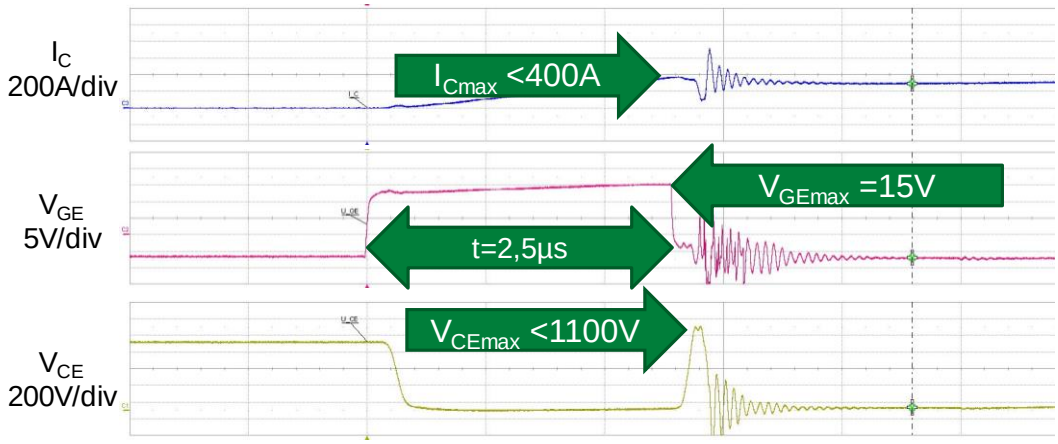

Figure 7. Measurement results from a destructive turn-off event

As the measurement reveals, the current turned off was well below the 450 A short-circuit limit. The gate-emitter-voltage was well-controlled, the time it took to turn off was below the 10 µs-limit and the overvoltage spike did not exceed the 1200 V the device is rated for. Still, the IGBT was destroyed, and the question raised, why so?

Entering the point of the turn-off into the diagram in Figure 6, the violation that happens becomes obvious in Figure 8:

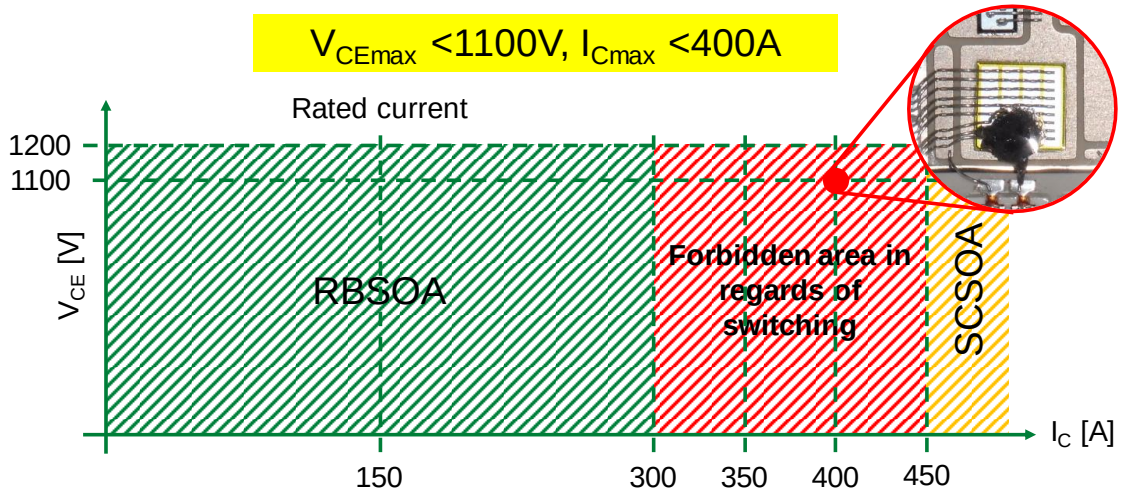

Figure 8. Locating the point of turn-off

Clearly, the switching event was done within the no-go-area with the destructive effect previously predicted.

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To clear the situation, the control strategy for short circuit was changed. Instead of reacting on the overcurrent signal instantly and turn off after just 2.5 µs, a blanking time of about 6 µs was added.

Figure 9 represents the measurement done in the same setup.

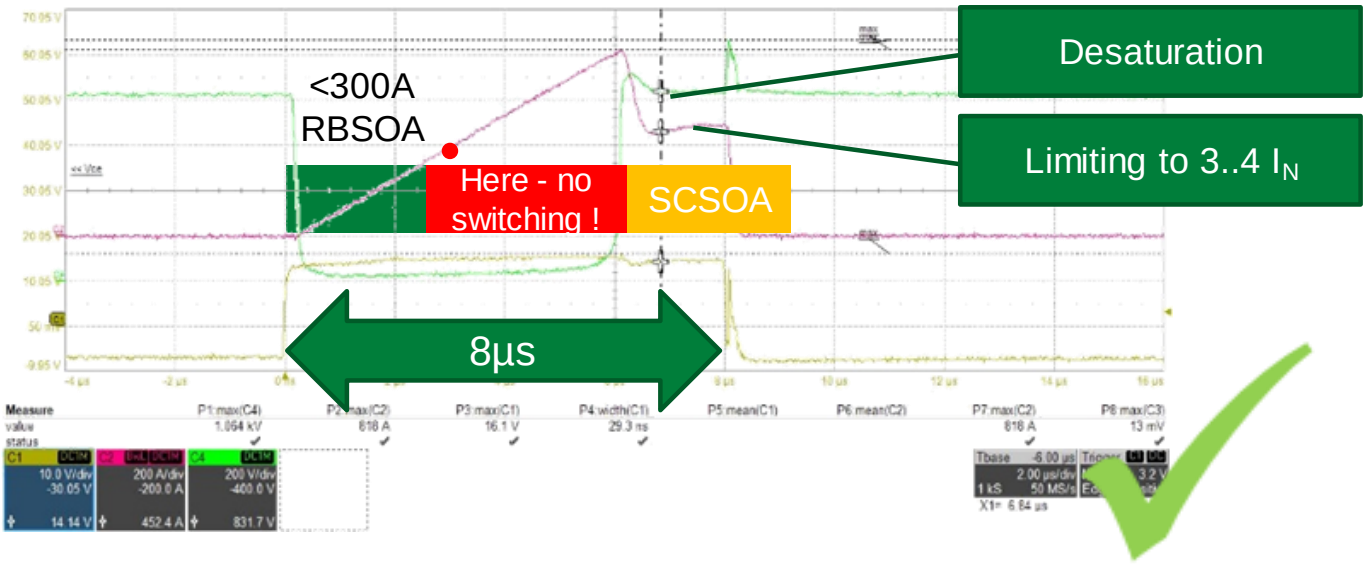

Figure 9. Properly turned off overcurrent or short-circuit event

While the red dot marks the former turn-off point, the current is now allowed to grow further. At first sight, this seems to worsen the situation as the losses and, as such, the chip temperature grows. However, after about 6 µs the IGBT reaches desaturation, enters the SCSOA and the turn-off after 8 µs is safely done without damaging the component.

MOSFETs, other than IGBTs, don't feature a dedicated SCSOA. At high currents, the MOSFET goes into linear operation as depicted in the FBSOA-diagram, so short-circuit and overcurrent events are covered by diagrams as given in Figure 2.

5. Conclusion

Handling overcurrent events, especially short circuit events, is challenging but manageable. Doing so while remaining within the given specifications can successfully be achieved.

Simply turning off a detected overcurrent as fast as possible may not be the best strategy as it may lead to damage caused by so-called RBSOA-exceedance. Ensuring that the IGBT reaches desaturation is a key factor in handling short circuit events with this technology.

For additional information please visit www.Littelfuse.com/powersemi

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