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IXYS SEMICONDUCTOR GMBH E72873
Edisonstrasse 15
68623 Lampertheim, GERMANY

Electrically Isolated Semiconductor Device, Model(s) GBO25-12NO1, GBO25-16NO1

Power Switching Semi-Conductors, "ISOPLUS-247 package", Model(s) C, D, I or M followed by additional numbers and letters, followed by HI, HJ, HQ or HR.

Power Switching Semi-Conductors, "ISOPLUS-247 package", Model(s) CS or DS followed by up to 10 numbers and letters, followed by R.

Power Switching Semi-Conductors, "ISOPLUS-i4", Model(s) C, D, I or M followed by two letters, followed by additional numbers and letters, followed by FB, FC, FD or FE.

Power switching semi-conductors, "ISOPLUS-i4", Model(s) CS#

Power Switching Semi-Conductors, "ISOPLUS-i4", Model(s) CS, DH, DS followed by up to 15 numbers and letters, followed by F or F1.

Power switching semi-conductors, "ISOPLUS-i4", Model(s) DS#, DSE#, FBE#, FBO#, FBS#, FCC#, FCD#, FDC#, FDD#, FDI#, FDM#, FEE#, FID#, FII#, FIO#, FMD#, FMK#, FMM#, FRR#, FSS#, FUE#, FUO#, FUS#, IXBF#, IXDF#, IXEF#, IXFF#, IXGF#, IXKF#, IXLF#, IXSF#, IXUF#

Power Switching Semi-Conductors, "ISOPLUS220 package", Model(s) C, D, I or M followed by additional numbers and letters, followed by PI or PJ.

Power Switching Semi-Conductors, "ISOPLUS220 package", Model(s) CS, DS or DG followed by numbers and letters, followed by C.

Power switching semi-conductors, Model(s) 40370-32*

Power Switching Semi-Conductors, Model(s) C, D, I or M followed by two letters, followed by additional numbers and letters, followed by NA.

Power Switching Semi-Conductors, Model(s) C, D, I, and M followed by numbers and/or letters, followed by GU, GV, GW, GX, GY or GZ.

Power Switching Semi-Conductors, Model(s) C, D, I, and M followed by numbers and/or letters, followed by LA, LB, LC, or LD.

Power Switching Semi-Conductors, Model(s) CS followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) D followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) D, C, M or I followed by additional letters and/or numbers, followed by PN or PM.

Power Switching Semi-Conductors, Model(s) DS followed by additional letters and/or numbers, followed by M.

Power switching semi-conductors, Model(s) DSEI....P, DSEK....P

Power Switching Semi-Conductors, Model(s) GUO followed by numbers, followed by "-", followed by numbers, followed by NO1.

Power Switching Semi-Conductors, Model(s) ISOPLUS-264 Models C, D, I or M, followed by two letters, followed by additional numbers and letters, followed by KI, KJ, KK, KL, KM, KN ,KO, KP, KQ, KR, KS, KT, KU, KV. Models IXBL, IXFL, IXTL or LKK, followed by additional numbers and letters

Power Switching Semi-Conductors, Model(s) IX (single phase) followed by two numbers, followed by MB, followed by three numbers.

Power Switching Semi-Conductors, Model(s) IX (three phase) followed by two numbers, followed by MT, followed by three numbers.

Power Switching Semi-Conductors, Model(s) IX followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) M followed by two letters, followed by additional numbers and letters, followed by JA, JB, JC, JD or JE.

Power Switching Semi-Conductors, Model(s) MC and M followed by two letters, followed by additional numbers or letters, followed by VB or VC.

Power Switching Semi-Conductors, Model(s) MC, MD, MI or MM followed by two letters, followed by additional numbers and letters, followed by ED, EH, SF, or SH.

Power Switching Semi-Conductors, Model(s) MC, MD, MI or MM followed by two letters, followed by additional numbers and letters, followed by ML or MH.

Power Switching Semi-Conductors, Model(s) MC, MD, MI or MM followed by two letters, followed by additional numbers and letters, followed by TA, TB, TC, TD, TE, TF, or TG.

Power Switching Semi-Conductors, Model(s) MC, MD, MI or MM followed by two letters, followed by additional numbers and letters, followed by VA.

Power Switching Semi-Conductors, Model(s) MC, MD, MI or MM followed by two letters, followed by additional numbers and letters, followed by YA, YB, YC, YD, YE,YF, YI, YJ, YK or YL.

Power Switching Semi-Conductors, Model(s) MC, MD, MI, and MM followed by 8 to 10 alphanumeric characters, followed by MI.

Power Switching Semi-Conductors, Model(s) MC, MD, MI, and MM followed by 8 to 10 alphanumeric characters, followed by SA.

Power Switching Semi-Conductors, Model(s) MC, MD, MI, and MM followed by 8 to 11 alphanumeric characters, followed by CA, CB, CC, CD, CE, CF, CG, CH.

Power Switching Semi-Conductors, Model(s) MC, MD, MI, or MM followed by two letters, followed by additional numbers and letters, followed by KA, KB, KC, KD or KE.

Power Switching Semi-Conductors, Model(s) MC, MD, MI, or MM followed by two letters, followed by additional numbers or letters, ending with VH.

Power Switching Semi-Conductors, Model(s) MCC, MCD, MCK, MDC, or MDD followed by 120 through 200.*

Power Switching Semi-Conductors, Model(s) MCC, MCD, MDA, MDC, or MDD followed by numbers between 19 and 100.*

Power Switching Semi-Conductors, Model(s) MCC, MCD, MDC, or MDD followed by 170 through 350.*

Power switching semi-conductors, Model(s) MCC165*, MCC220*, MCC250*, MCC310*, MCD165*, MCD220*, MCD250*, MCD310*

Power switching semi-conductors, Model(s) MCO or MDO, followed by 400 through 650.*

Power switching semi-conductors, Model(s) MDC165*, MDC220*, MDC250*, MDC310*, MDD165*, MDD220*, MDD250*, MDD310*

Power Switching Semi-Conductors, Model(s) MDI followed by 90 through 1550*

Power switching semi-conductors, Model(s) MDI, MID or MII, followed by 20 through 150.*

Power Switching Semi-Conductors, Model(s) MEA, MEE, MEK, MPK or MEO followed by numbers between 50 and 240.*

Power Switching Semi-Conductors, Model(s) MEA, MEE, MEK, or MEO followed by 150 through 600.*

Power Switching Semi-Conductors, Model(s) MID followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) MIE followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) MII followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) MIO followed by 90 through 1550*

Power switching semi-conductors, Model(s) MIO, VIO or VMO, followed by 200 through 1200.*

Power switching semi-conductors, Model(s) MLO 100*, MLO 36*, MLO 50*, MLO 75*, MLO....7, MMO 36*, MMO 50*, MMO 75*

Power Switching Semi-Conductors, Model(s) MMO, MCO, MCD followed by additional numbers, followed by io1 or io6.

Power switching semi-conductors, Model(s) MMO....7

Power Switching Semi-Conductors, Model(s) MUBW, MWI or MKI followed by additional numbers and/or letters, followed by 7or 8, may be followed by T.

Power Switching Semi-Conductors, Model(s) MUBW, MWI, or MKI followed by additional numbers and /or letters, followed by 6K.

Power Switching Semi-Conductors, Model(s) MWI followed by additional numbers and/or letters, followed by 9.

Power Switching Semi-Conductors, Model(s) MWI followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power Switching Semi-Conductors, Model(s) VBBW followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VBE*, VBE.. .NO7

Power Switching Semi-Conductors, Model(s) VBEF followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power Switching Semi-Conductors, Model(s) VBH followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VBO or VUO, followed by 10 through 125.*

Power switching semi-conductors, Model(s) VBO or VUO, followed by 50 through 100.*

Power switching semi-conductors, Model(s) VBO...7, VBO...NO7, VBO13*, VBO14*, VBO15*, VBO16*, VBO17*, VBO18*, VBO19*, VBO20*, VBO21*, VBO22*, VBO23*, VBO24*, VBO25*, VBO26*, VBO27*, VBO28*, VBO29*, VBO30*, VBO31*, VBO32*, VBO33*, VBO34*, VBO35*, VBO36*, VCA....7, VCC....7, VCD....7, VCK....7, VCO....7

Power Switching Semi-Conductors, Model(s) VDD may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VDI followed by 90 through 1550*

Power switching semi-conductors, Model(s) VDI....P1, VDI100*, VDI25*, VDI50*, VDI75*, VEE*, VGO....7, VH013*, VH014*, VH015*, VH016*, VH017*, VH018*, VH019*, VH020*, VH021*, VH022*, VH023*, VH024*, VH025*, VH026*, VH027*, VH028*, VH029*, VH030*, VH031*, VH032*, VH033*, VH034*, VH035*, VH036*, VHF*, VHF....7, VHF13*, VHF14*, VHF15*, VHF16*, VHF17*, VHF18*, VHF19*, VHF20*, VHF21*, VHF22*, VHF23*, VHF24*, VHF25*, VHF26*, VHF27*, VHF28*, VHF29*, VHF30*, VHF31*, VHF32*, VHF33*, VHF34*, VHF35*, VHF36*, VHFD*, VHM...7, VHO....7

Power Switching Semi-Conductors, Model(s) VID followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) VID may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power switching semi-conductors, Model(s) VID....P1, VID100*, VID25*, VID50*, VID75*

Power Switching Semi-Conductors, Model(s) VIE followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) VII followed by 90 through 1550*

Power switching semi-conductors, Model(s) VII....7, VII....P1, VII100*, VII25*, VII50*, VII75*, VIO....P1, VK013*, VK014*, VK015*, VK016*, VK017*, VK018*, VK019*, VK020*, VK021*, VK022*, VK023*, VK024*, VK025*, VK026*, VK027*, VK028*, VK029*, VK030*, VK031*, VK032*, VK033*, VK034*, VK035*, VK036*, VKI....7, VKI....P1, VKM...7, VKO....7

Power Switching Semi-Conductors, Model(s) VMD may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VMH may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VMK, VMM, or VMO followed by numbers between 25 and 250.*

Power Switching Semi-Conductors, Model(s) VMM followed by 90 through 1550*

Power Switching Semi-Conductors, Model(s) VMM may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power switching semi-conductors, Model(s) VMO....P1, VTO....7

Power Switching Semi-Conductors, Model(s) VUB followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VUB*

Power Switching Semi-Conductors, Model(s) VUB, VUO, or VVZB followed by additional numbers and/or letters, followed by NO1, NOX or ioX, may be followed by T.

Power switching semi-conductors, Model(s) VUB...P1, VUB...PO1, VUBM....P1

Power Switching Semi-Conductors, Model(s) VUBW followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VUC*

Power Switching Semi-Conductors, Model(s) VUC15 may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VUC25 may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VUC36 may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power switching semi-conductors, Model(s) VUCB*, VUE*, VUE.. .NO7, VUI*, VUI....N7

Power Switching Semi-Conductors, Model(s) VUM followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VUM*, VUM.....N7

Power Switching Semi-Conductors, Model(s) VUM24 may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VUM33 may be followed by 15, 24, 25, 33, or 36, followed by 05, 12, 14, 16, 500, 1200, 1400, or 1600, may be followed by G02, E, N01, N, PH *

Power Switching Semi-Conductors, Model(s) VUO followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VUO*, VUO...7, VUO...NO7, VUO30*, VUO50*, VUO60*

Power Switching Semi-Conductors, Model(s) VVBW followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VVY*, VVY12*, VVY24*, VVY40*

Power Switching Semi-Conductors, Model(s) VVZ followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VVZ*, VVZ....7, VVZ12*, VVZ24*, VVZ40*

Power Switching Semi-Conductors, Model(s) VVZB followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VW2X*, VW3....7, VWI....P1

Power Switching Semi-Conductors, Model(s) VWM followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VWM....7

Power Switching Semi-Conductors, Model(s) VWO followed by additional numbers and/or letters, followed by A5, DL1, iol, io2, ioX, NO1, NO2, or NOX, may be followed by T

Power switching semi-conductors, Model(s) VWO....7, VZI....P1

Power switching semi-conductors, package SOT-227B, miniBloc, Model(s) DH1X*, DH2X*, DSEI*, DSEP*, DSI*, DSS*, IXDN*, IXEN*, IXFN*, IXGN*, IXKN*, IXLN*, IXSN*, IXTN*, IXUN*, VBE*, VBO*, VBS*

Semi-conductor diodes, thyristors, IGBTs or MOSFETS, "ISOPLUS-247 package", Model(s) IXDR%, IXER%, IXFR%, IXKR%

Semi-conductor diodes, thyristors, IGBTs or MOSFETS, "ISOPLUS220 package", Model(s) IXKC*

- Followed by up to 15 numbers and letters.

% - Followed by up to 10 numbers and letters.

* - May be followed by additional numbers or letters.

Marking: Company name or trademark IXYS, and model designation.

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IXYS CORP E153432
1590 BUCKEYE DR
MILPITAS, CA 95035-7418 USA

Power Switching Semi-Conductors, Model(s) CS followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) D followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) D, C, M or I followed by additional letters and/or numbers, followed by PN or PM.

Power Switching Semi-Conductors, Model(s) DS followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) IX followed by additional letters and/or numbers, followed by M.

Power Switching Semi-Conductors, Model(s) IX followed by an upper case letter, followed by N, followed by any number 01 through 99999, followed by additional numbers and letters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISO247 package, Model(s) IX J Series IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by J, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS I4-PAC package, Model(s) IX F Series IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by F, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS SMPD package, Model(s) IXM2001 IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by L, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS SMPD package, Model(s) MDIX4X30N65B3 IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by L, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS SMPD package, Model(s) MMIX IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by L, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS SMPD package, Model(s) MMIX1992 IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by L, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS220 package, Model(s) IX followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by C, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, ISOPLUS264 package, Model(s) IX L Series IX, followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by L, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

Semi-conductor diodes, thyristors, IGBT or MOSFETS, SSMPD package, Model(s) MMJX MMJX, followed by 1, 2, 3, followed by B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by number 1-999, followed by N or P, followed by number 1-800, may be followed by up to 6 alpha-numeric characters.

Semi-conductor diodes, thyristors, or MOSFETS, 247 hole-less package, Model(s) DSE (a), IXBR (a), IXGR (a), IXLR (a), IXSR (a), IXTR (a)

Semi-conductor diodes, thyristors, or MOSFETS, ISOPLUS247 package, Model(s) IX followed by one letter B, C, D, E, F, G, H, K, L, S, T, U, X, or Y, followed by R, may be followed by 01-09, 1R1-1R9, 1-9, 10-99, or 100-999 may be followed by N or P, may be followed by 01-10, 1-99 or 100-800, may be followed by up to six alpha-numeric characters.

(a) - Followed by up to 10 numbers and letters.

Marking: Company name and model designation.

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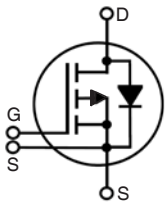
IXYS

PolarP™ Power MOSFET

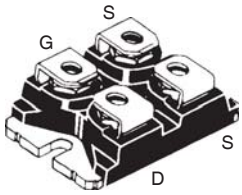
IXTN90P20P

V_{DSS} = - 200V
I_{D25} = - 90A
$R_{DS(on)}$ ≤ 44mΩ

P-Channel Enhancement Mode
Avalanche Rated



miniBLOC
E153432



G = Gate D = Drain
S = Source

Either Source Terminal S can be used as the Source Terminal or the Kelvin Source (Gate Return) Terminal.

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		- 200	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ		- 200	V
V_{GSS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C		- 90	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}		- 270	A
I_A	T_C = 25°C		- 90	A
E_{AS}	T_C = 25°C		3.5	J
dv/dt	I_S ≤ I_{DM}, V_{DD} ≤ V_{DSS}, T_J ≤ 150°C		10	V/ns
P_D	T_C = 25°C		890	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS	t = 1 minute	2500	V~
	I_{ISOL} ≤ 1mA	t = 1 second	3000	V~
M_d	Mounting Torque		1.5/13	Nm/lb.in
	Terminal Connection Torque		1.3/11.5	Nm/lb.in
Weight			30	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = - 250μA	- 200			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1mA	- 2.0		- 4.5	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
I_{DSS}	V_{DS} = V_{DSS}, V_{GS} = 0V			- 50	μA
	T_J = 125°C			- 250	μA
$R_{DS(on)}$	V_{GS} = -10V, I_D = 0.5 • I_{D25}, Note 1			44	mΩ

Features

- International Standard Package
- miniBLOC, with Aluminium Nitride Isolation
- Rugged PolarP™ Process
- Avalanche Rated
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switches
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment
- Current Regulators

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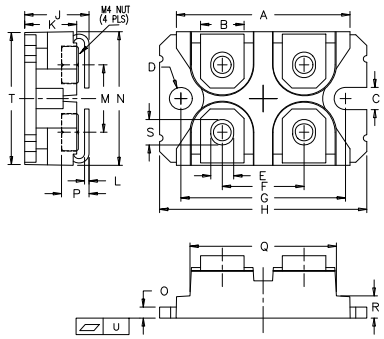
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = -10V, I_D = 0.5 • I_{D25}, Note 1	30	51		S
C_{iss}	V_{GS} = 0V, V_{DS} = - 25V, f = 1MHz		12		nF
C_{oss}			2210		pF
C_{rss}			250		pF
$t_{d(on)}$	**Resistive Switching Times**		32		ns
t_r	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0 .5 • I_{D25}		60		ns
$t_{d(off)}$	R_G = 1Ω (External)		89		ns
t_f			28		ns
$Q_{g(on)}$	V_{GS} = -10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		205		nC
Q_{gs}			45		nC
Q_{gd}			80		nC
R_{thJC}				0.14	°C/W
R_{thCS}			0.05		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			- 90	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 360	A
V_{SD}	I_F = - 45A, V_{GS} = 0V, Note 1			- 3.2	V
t_{rr}	I_F = - 45A, -di/dt = -150A/µs		315		ns
Q_{RM}	V_R = -100V, V_{GS} = 0V		6.6		µC
I_{RM}			- 42		A

Note 1: Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.

SOT-227B (IXTN) Outline



(M4 screws (4x) supplied)

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.240	1.255	31.50	31.88
B	.307	.323	7.80	8.20
C	.161	.169	4.09	4.29
D	.161	.169	4.09	4.29
E	.161	.169	4.09	4.29
F	.587	.595	14.91	15.11
G	1.186	1.193	30.12	30.30
H	1.496	1.505	38.00	38.23
J	.460	.481	11.68	12.22
K	.351	.378	8.92	9.60
L	.030	.033	0.76	0.84
M	.496	.506	12.60	12.85
N	.990	1.001	25.15	25.42
O	.078	.084	1.98	2.13
P	.195	.235	4.95	5.97
Q	1.045	1.059	26.54	26.90
R	.155	.174	3.94	4.42
S	.186	.191	4.72	4.85
T	.968	.987	24.59	25.07
U	-.002	.004	-0.05	0.1

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ T_J = 25ºC

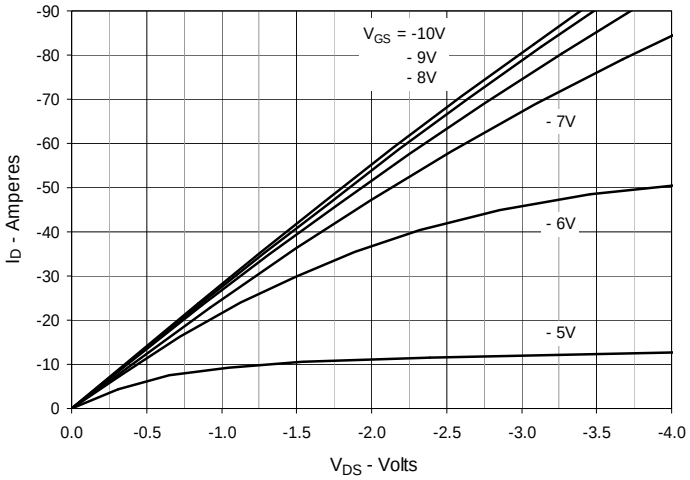

Fig. 2. Extended Output Characteristics @ T_J = 25ºC

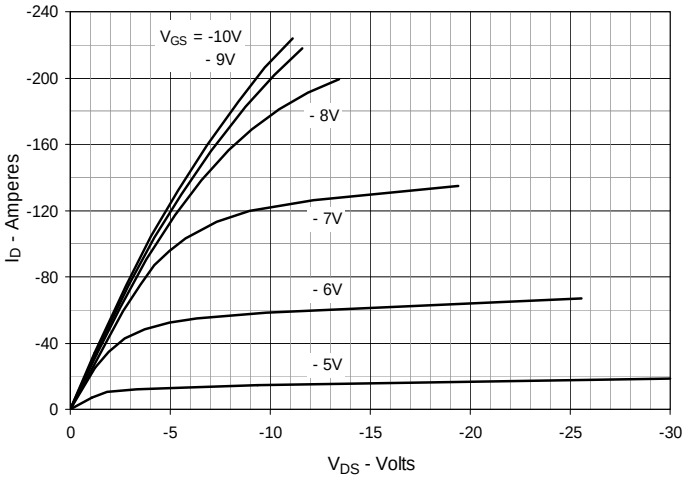

Fig. 3. Output Characteristics @ T_J = 125ºC

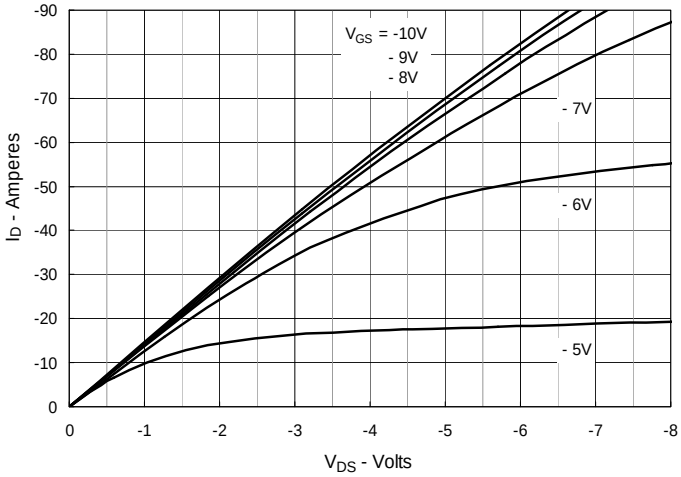

Fig. 4. $R_{DS(on)}$ Normalized to I_D = - 45A Value vs. Junction Temperature

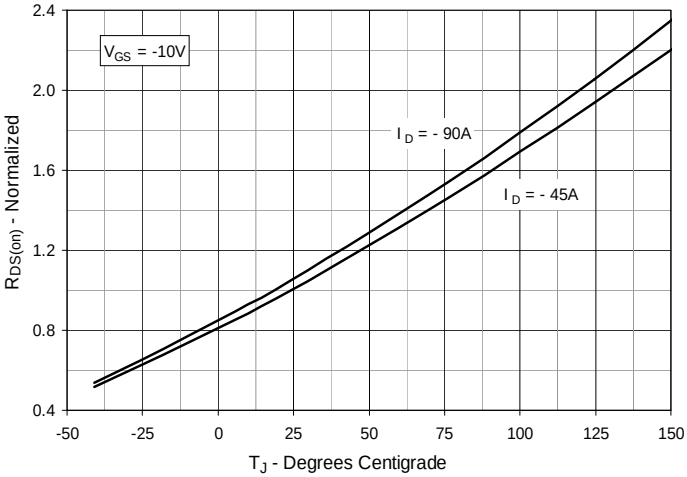

Fig. 5. $R_{DS(on)}$ Normalized to I_D = - 45A Value vs. Drain Current

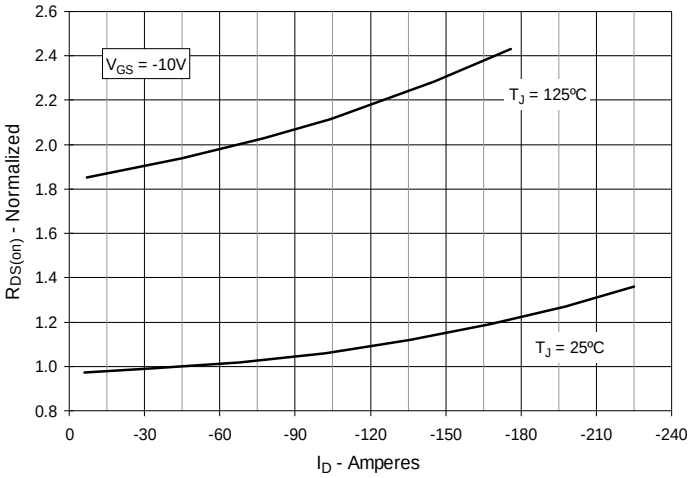

Fig. 6. Maximum Drain Current vs. Case Temperature

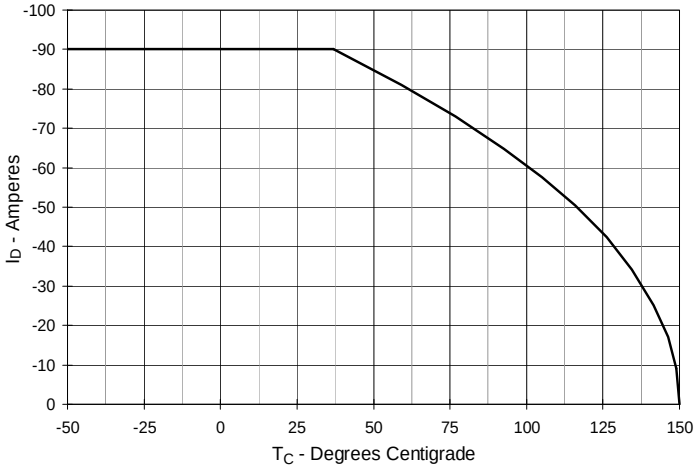

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Fig. 7. Input Admittance

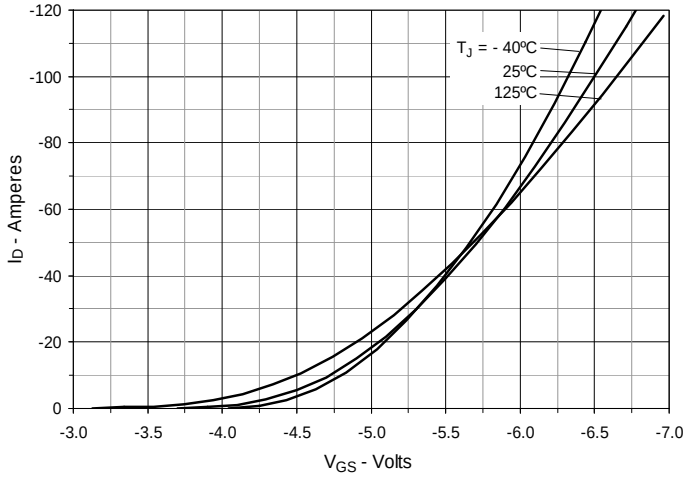

Fig. 8. Transconductance

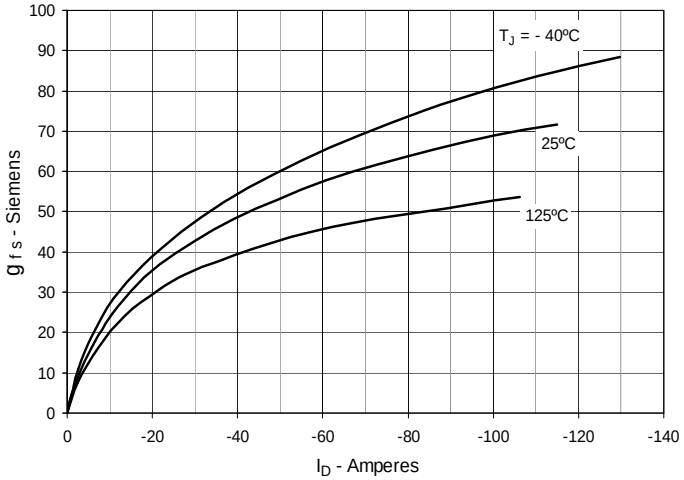

Fig. 9. Forward Voltage Drop of Intrinsic Diode

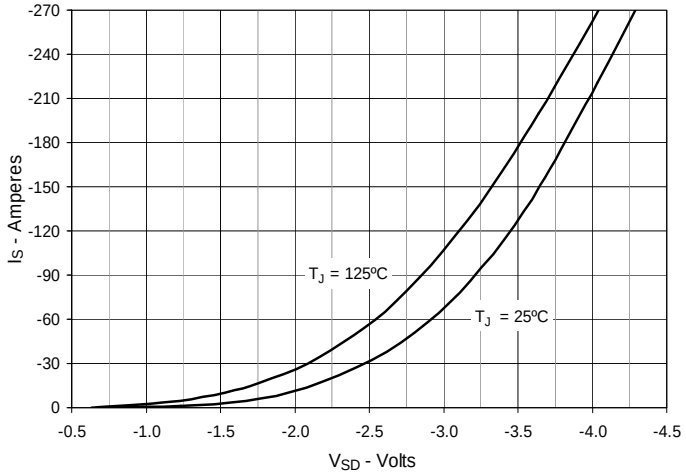

Fig. 10. Gate Charge

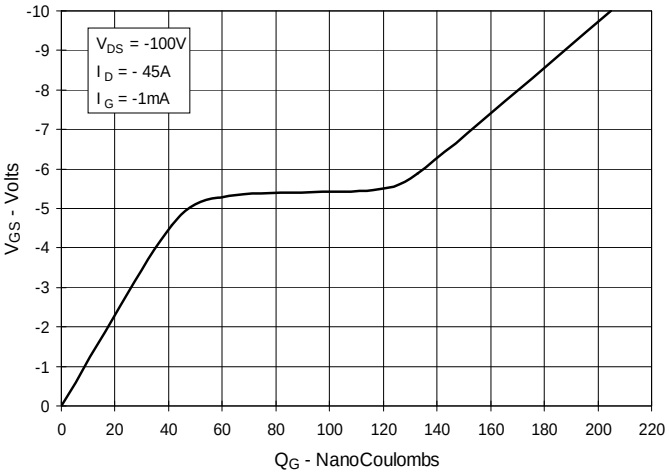

Fig. 11. Capacitance

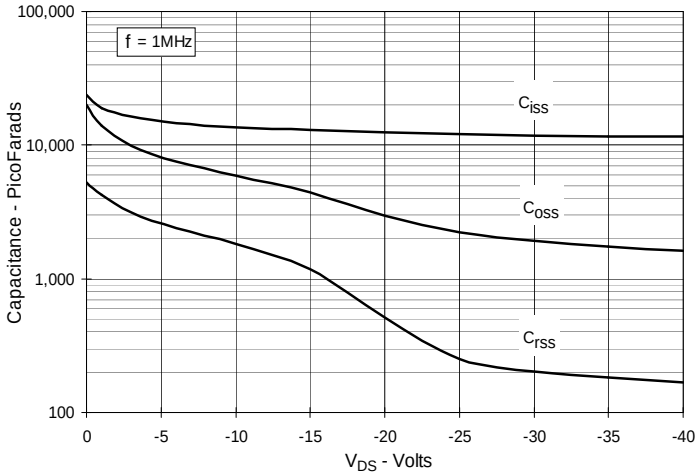

Fig. 12. Forward-Bias Safe Operating Area

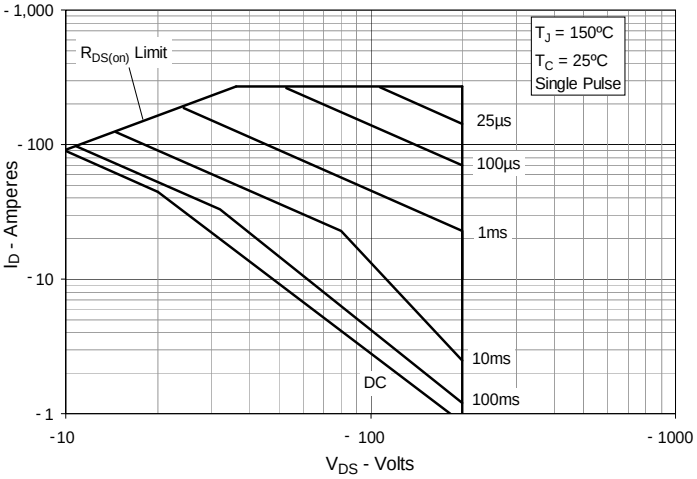

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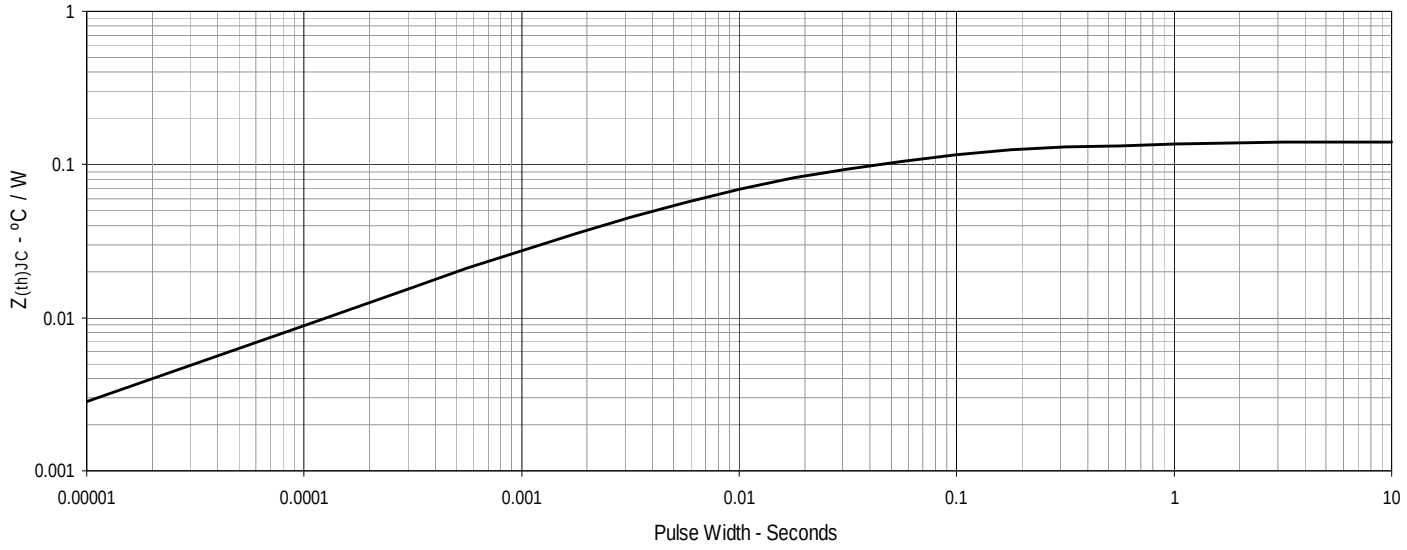
Fig. 13. Maximum Transient Thermal Impedance



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Handling and Mounting Littelfuse miniBLOC - SOT227B

Objectives

This application note discusses mounting and handling for Littelfuse power semiconductors in SOT227B package, the miniBLOC, as depicted in Figure 1. Information is provided focusing on special precautions to be considered during mounting.

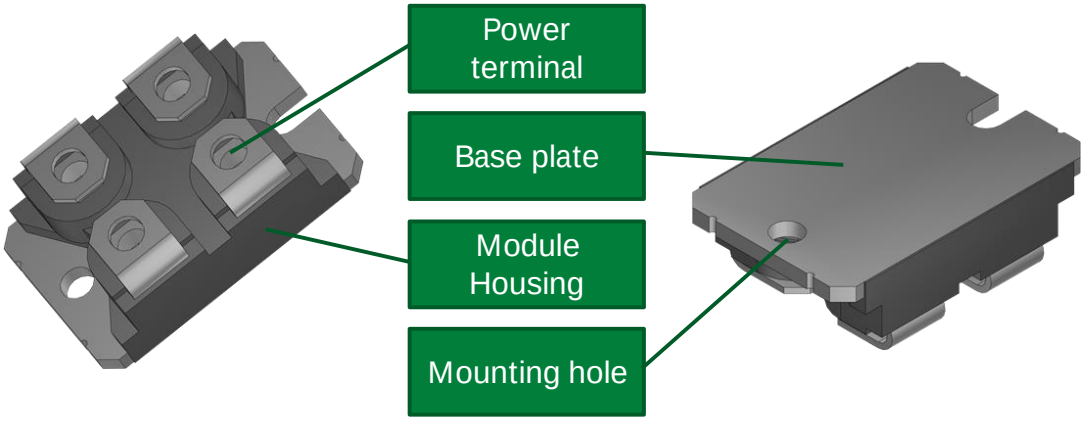

Figure 1: Littelfuse miniBLOC, in SOT227B

Applications

- Industrial motor drives
- PV inverters
- UPS systems
- DC-DC converters
- Commercial vehicles

Target Audience

This document is intended for potential adopters of power semiconductors who want to determine the appropriate mounting and cooling solution to ensure proper package mounting and thermal performance.

Contact Information

For more information on the topic of mounting this kind of device, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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1. Introduction

The miniBLOC is the intermediate link between discrete power devices like the TO-263 and power semiconductor modules like Littelfuse Y-series. Though it features a DCB-substrate to carry the dies, the molded housing structure characterizes it to be a discrete component rather than a power module. The internal DCB substrate inherently offers electrical insulation, allowing for mounting of several miniBLOCs to the same heat sink without additional means of isolation. The base plate in turn acts as large-area interface between the semiconductor and a heat sink.

The package provides features beneficial for power electronic applications. These include:

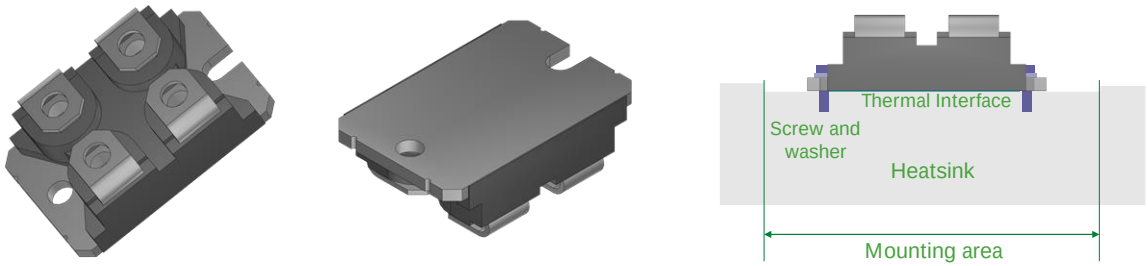
- High electric insulation strength
- High thermal performance
- Current ratings to support applications up to hundreds of kilowatts
- Internal construction is designed to reduce stray inductance and parasitic capacitances, leading to improved EMI-performance

With the four terminals, the miniBLOC is available in a variety of technologies including IGBT, thyristor , Si- and SiC- diode and MOSFET in voltage classes from 40 to 2500 V and current ratings up to 600A.

There are a few miniBLOCs, such as the DSEC 240-04A and the DSEC 240-06A, that feature a non-isolated construction and an electrically active base plate. These are diode devices, designed for special purposes. Despite the slightly different internal construction, the recommendations made in this application note are valid for these types as well.

2. Recommended Heat Sink Assembly

Semiconductor power devices are designed to be mounted onto a heat sink, most often using screws. A layer of Thermal Interface Material (TIM) is needed to ensure a high thermal conductivity from the dice to the heatsink. After the application of thermal interface material is completed, the component can be mounted to a heatsink by mounting screws. An example of a SOT227B assembly is sketched in Figure 2.



(a) Power device, top-view (b) Power device, bottom-view (c) Mounted to the Heat Sink

Figure 2. Mounting the miniBLOC to a Heat Sink

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2.1. Heat Sink Preparation

When the package is mounted, the base plate becomes the crucial surface for thermal management. A heatsink needs to be mounted for heat dissipation, as depicted in Figure 2. There are dedicated mounting holes in the package; the proper set of dimensions for the drill-hole-pattern is given in the correlating datasheet.

To ensure a low value of thermal resistance, the contact surface of the heat sink must be flat, even, and clean. For the mounting area, the surface quality must achieve or exceed the values given in Figure 3.

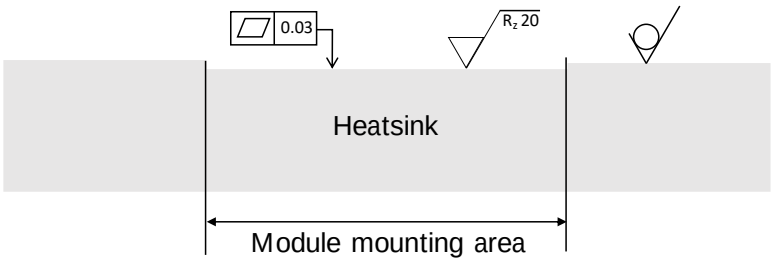


Figure 3. **Heat Sink's Surface Requirements to Mount** Power Modules

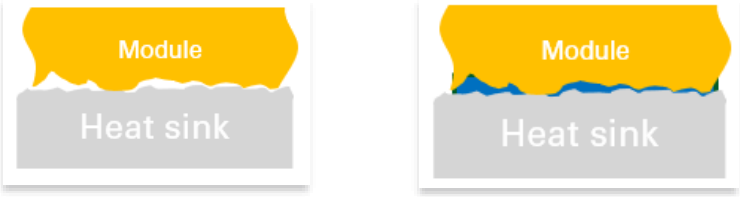
Prior to mounting, cleaning all surfaces with a suitable cleaning agent is advised.

2.2. Use of Thermal Interface Materials

The use of Thermal Interface Materials (TIM) is mandatory to achieve a suitable contact between the device's base and the heat sink surface. It reduces the thermal resistance case-to-heatsink, R_{thch}. Thermal interface materials are available as thermal pad and thermal grease or compound. Unlike the discrete packages where the copper cooling pad is usually electrically active, packages with solid metal base plates internally feature a DCB structure which uses a layer of ceramic as electrical isolation. With up to 4500 V isolation voltage, the packages provide the option to use electrically non-isolated thermal interface materials. It is not recommended to use an interface material with isolation such as silicone-pads sometimes used for discrete packaged devices. These materials inherently exhibit a higher thermal resistance compared to thermal greases or conductive thermal pads.

The thermal interface materials should be applied evenly to the device base plate or the heat sink surface. Ideally, screen printing is used to achieve accurate and reproduceable results. A screen thickness of 100µm with a fill-factor of 70-80% and a regular pattern of honeycomb-shaped openings has proven to be a reasonable approach.

As no electrical isolation is required from the TIM layer, it is recommended to have a very thin layer of TIM so that the material just fills the gaps and voids between the device's copper pad and the heatsink, as seen in Figure 4.



(a) Without TIM, air gaps remain

(b) With TIM, the gaps are filled, contact area increases, and thermal resistance is reduced

Figure 4. Improving Thermal Transfer by using Thermal Interface Material (TIM)

If a solid thermal pad is considered, softer materials with high thermal conductivity are preferred to better fill the gaps. The thermal pad should be as thin as possible to provide the lowest thermal resistance. The mounting mechanism using screws provides proper pressure on the thermal interface material to ensure a low value of thermal resistance. A procedure to create a proper stencil and set up a basic stencil-printing equipment is described in detail in the application note *Basics of Stencil Generation to Apply Thermal Grease to Power Semiconductors*, which can be downloaded from the Littelfuse website.

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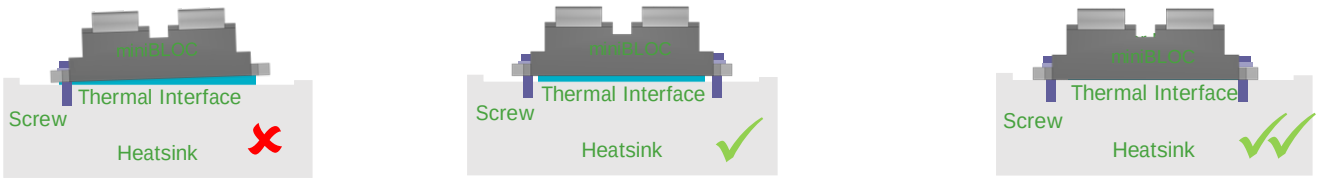
2.3. Detailed Mounting Procedure

Mounting the module by screws inherently achieves mounting forces in a range of kilonewton. Though the base plate is highly resistant to pressure, the internal DCB-structure is very sensitive towards bending. Therefore, careful handling and step-by-step tightening of the screws is mandatory to achieve the desired pressure distribution and prevent bending the internal DCB.
Besides the mounting forces, an even distribution of thermal interface material is important. Uneven distribution, particularly with higher amount of material in the center of the module, may also lead to high local forces that could damage the DCB inside the power module.
Using solid sheets as thermal interface material is not a recommended solution as these typically remain too thick and limit the module's thermal performance. Additionally, they may lead to further issues during mounting.

Figure 5(a) illustrates that the module lifts on one side in case the first screw is bolted down too much and Figure 5(b) and Figure 5(c) show a two-step sequence to prevent this from happening.



(a) To be prevented: Bolting down one side may tilt the module which leads to bending

(b) Recommended: Loosely bolt down all screws to the point **where the screw's head touches the washer**

(c) In a further step, tighten the screws to their final torque using a precise torque wrench

Figure 5: Bolting down the screw – Incorrect and Correct Method

The tightening procedure is summarized in Table 1.

Table 1: Mounting Sequence to mount SOT227B

Package Type	Screw Diameter	Step 1	Step 2	Step 3	Step 4
SOT227B	4 mm	Bolt down both screws, so that the screws' heads get the washers to contact the base pate	Apply 0.5 Nm to both screws	Wait for the assembly to settle. Settling time depends on the TIM in use and varies from 5-10 minutes	Apply no more than 1.5 Nm to both screws

In case imperial screws are preferred for mounting, a screw 8-36 is the closest replacement for M4. The mounting torque needs to be limited to not exceed 11.5 lb-in

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3. Further Mechanical Aspects

Besides the data and procedures to mount power electronic components, influences that arise from mechanical parts and physics need detailed attention. Some details that appear to be of minor impact can lead to unexpected effects with highly detrimental consequences.

3.1. Metric Thread, Imperial Thread, Self-tapping Screws

The recommended material for mounting the module to the heat sink is a metric screw with spring-washer and captivated washer as described by ISO 10644. Zinc- or nickel-plated steel screws with a property class 6.8 or higher, as depicted in Figure 6, are recommended.

Figure 6: Phillips-style Screws and Captivated Washers acc. to ISO 10644

Using screws with imperial scale is an option too. However, due to the different diameters and thread's pitch, the ratio between turning angle, torque, and resulting mounting forces also changes. Purely translating newton meter (Nm) into pound inches (lb-in) might result in misleading values. Individual verification of the result is advised to verify proper pressure and pressure distribution is achieved.

In case self-tapping screws like those described in DIN7504-K and ISO15480 are preferred, dedicated tests are needed to correlate torque, turning angle, and mounting force. As the torque mainly depends on the drill-hole's diameter and the heat sink material, no general recommendation can be made. Using washers and spring-washers in combination with self-tapping screws is advised.

3.2. Mounting the Electronics and DC-link Components

Power modules are robust regarding pressure applied, but highly sensitive towards pulling forces. Pulling forces can be a consequence of dynamic influences like shock and vibration but as well result from the combination of materials used in the construction and their tolerances.
A mechanical assembly must ensure that the resulting forces to the terminals remain directed as pictured in Figure 7.

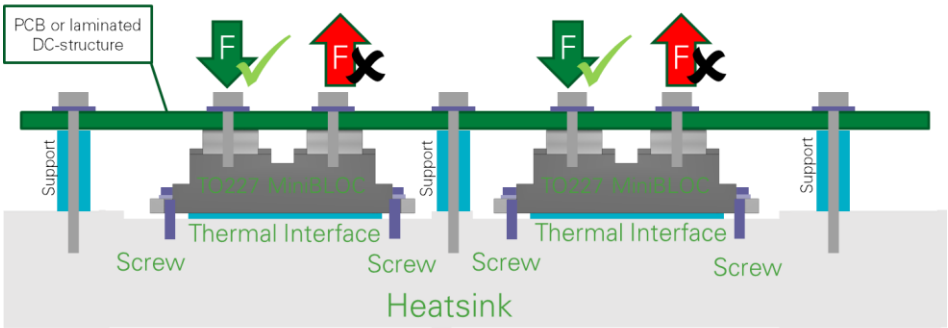

Figure 7: Module assembly with Power-Terminals attached

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A total force of up to 100N applying pressure to the module is tolerable while no pulling force may remain after mounting is complete. To achieve this, properly dimensioned supports must be installed. These prevent static forces as well as dynamic events from reaching the terminals. Including all tolerances, the supports' length needs to remain below the height of the module in use.
Larger components like DC-link capacitors, output terminals, or heavy current sensors require additional support. In case of vibration, undampened oscillating masses may inject destructive forces into the power component.

To mount the DC-link-structure to the modules, either as PCB or laminated copper plates, 4 suitable screws are delivered with each miniBLOC, a tube with 10 devices contains 40 screws. In case a different type of screw is desired, the screws mandatorily need to comply with the information given in the data sheet. The maximum length of the screws depends on the thickness of the structure mounted on top of the modules. Caution is advised as too long screws can damage the housing, enter electrically sensitive areas, and cause severe damage.

As the nuts embedded in the modules feature metric threads, the use of screws according to imperial scale is not an option for mounting the power terminals. The nuts are held in place by the housing. Applying too high torque can lead to damage of the housing and in turn to loss of function.

The terminal screws can support a maximum torque of 1.1 Nm or 9 lb-in. Especially in combination with oils used to prevent corrosion, the friction during mounting can change massively, leading to a distortion in the ratio of torque and turning angle. The same applies when using adhesive-based thread lockers.

When handling sub-assemblies, supporting the whole setup to move it is recommended. Using the bus bar or the PCB as a handle includes a high risk of applying pulling forces and therefore needs to be prevented.

If a module is being replaced, ensure there is no contamination in the threaded hole; for example, thermal paste that has been solvent washed into the threads, as this may limit the screws' engagement resulting in false fastener tension and module clamping force.
In situations where blind holes are not required for maintaining corrosion or pressure sealing performance, threaded through holes can be used as these can be brushed, washed clean, and inspected easily.

3.3. Insulation Management

Two major parameters require to be considered when PCB-layouts and DC-link-components are designed:

- Clearance – the shortest possible distance between two points, and
- Creepage distance – the shortest path from one point to another point along an uninterrupted line on solid material

Particularly when using laminated bus bar structures, isolating the layers from each other remains an important task.

In high-voltage environments, arcing between different voltage levels must be prevented. Arcing takes place over air-gaps – clearance distances – so the voltage level expected in the final system defines the distance between pads and traces as well as between active areas and heat sinks or other grounded parts. Even if the clearance between two points is chosen to be high enough, the insulation strength can be reduced by conductive particles over a longer period. This depends on the degree of pollution, which relates to the ambient conditions the device is used in.

IEC60664-1 gives an insight about the relevant conditions that need to be considered to determine the creepage and clearance distances in a targeted design.

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4. Conclusion

Littelfuse miniBLOC devices with their base plate and molded housing structure are mechanically robust components. Still, care needs to be taken to not bend the module during the mounting process and a mechanical arrangement must be designed to prevent pulling forces at the terminals. Applying thermal interface material by a well-controlled screen-printing process further helps to reduce unwanted mechanical stress to the device.

If these aspects are considered, mounting the devices can successfully be done by implementing established procedures and processes.

Revision History		
Version	Date	Changes
22.08a	August 2022	Initial version created for release

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Littelfuse Discrete Power MOSFET Datasheet Explanation

Objectives

The primary objective of this application note is to enhance the comprehension and analysis of power MOSFET datasheet parameters and graphs. By breaking down the technical specification into digestible insights, designers can gain deeper insights into the functionality and performance characteristics of MOSFETs. This application note provides a general recommendation about how to read and understand a datasheet with all its parameters and diagrams. The information presented plays a pivotal role in determining the operational limits and thresholds of the device.

Applications

This application note is applicable to all scenarios where power MOSFETs are utilized.

Target Audience

This document is intended for designers and developers who are utilizing Power MOSFETs within their respective applications.

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1. Introduction

In the realm of modern electronics and power systems, an extensive understanding of semiconductor components, particularly the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), is crucial for achieving optimal system-performance and -efficiency. MOSFETs play a pivotal role in switching applications, offering versatile solutions. This document serves as a guide, delving into the detailed parameters presented in MOSFET datasheets. It aims to empower engineers and designers to make informed decisions and effectively leverage MOSFET capabilities in diverse applications.

Littelfuse furnishes datasheets with parameters that are essential and useful for selecting the appropriate device as well as for predicting its performance in specific application. This facilitates designers in comparing products from various suppliers and gaining valuable insights into the operational constraints of the device.

The outlined values in the datasheet describe the device's behavior under varying virtual junction temperature and testing conditions. Additionally, the dynamic characterization tests undergo execution utilizing precise configurations aimed at precise measurement of switching losses. As a result, discrepancies in these metrics manifest between the intended user applications.

The graphs included in the datasheet represent typical performance characteristics and can be used to extrapolate from one set of operating conditions to another. This application note explains parameters based on the IXTH120N20X4 datasheet which is an N-channel enhancement mode, power MOSFET. All the parameters mentioned in a Littelfuse datasheet are measured according to *IEC 60747-8* standards.

2. Essential Datasheet Insight

This section serves as an overview of important information found on the first page of the datasheet, including the datasheet status.

2.1. Key Information

The first page of the datasheet includes details such as the part number, pinout diagram, features and benefits, applications, and key attributes of the product.

- **Part Number** indicates the manufacturer, MOSFET type, package type, current rating, channel type, voltage class, technology series and a suffix for some special packages that gives extra information such as high voltage package, over molded package, and w/ 4 leads. Designation of MOSFET part number is drafted in **Figure 1**. The detailed information about this can be found as part number nomenclature - discrete Si MOSFET on Littelfuse website.

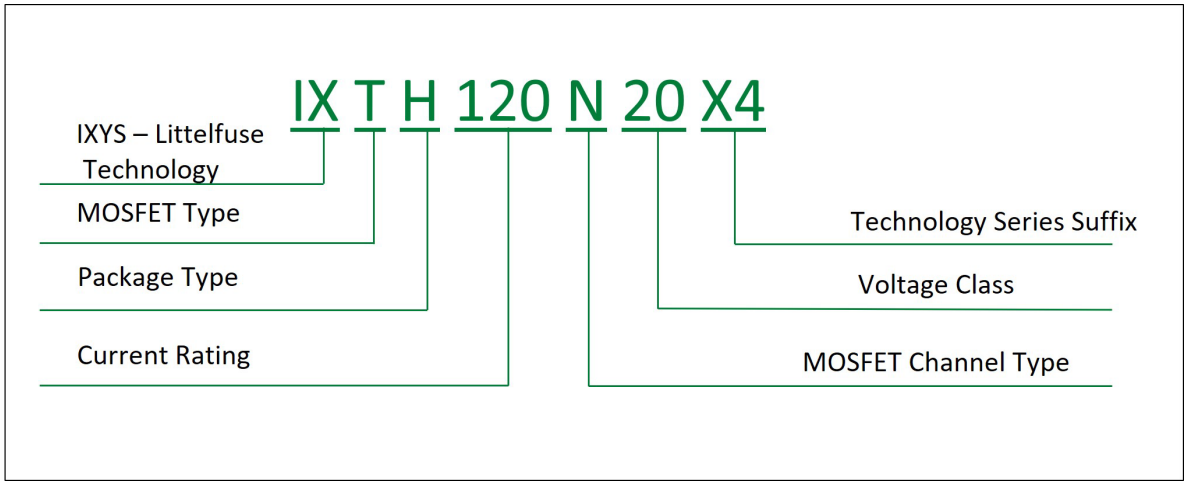

Figure 1. Part Number Designation

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- **Pinout Diagram** provides a visual representation of the device's physical layout including circuit symbol as highlighted in **Figure 2**.

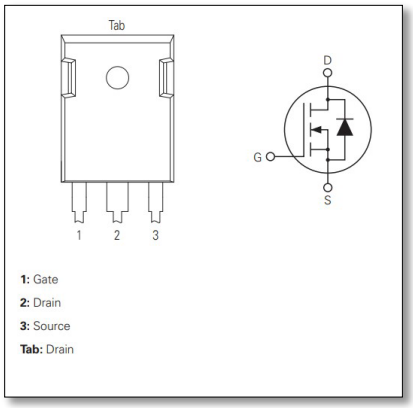

Figure 2. Pinout Diagram of TO-247 and Circuit Symbol of an N-channel Enhancement Mode MOSFET

- **Features and Benefits** encompasses a comprehensive list of features and their corresponding benefits offered by the MOSFET device, which helps user acquire a better understanding of how the MOSFET can meet their specific application requirements to deliver optimal performance and reliability.
- **Key Attributes / Product summary** highlights the key specifications and performance characteristics of the MOSFET, including parameters such as maximum drain-source voltage (V_{DSS}), maximum drain current (I_D) at 25°C, and on-state resistance ($R_{DS(on)}$) as pointed out in **Table 1**.

Table 1. Key Attributes/Product Summary

Characteristic	Value	Unit
V_{DS}	200	V
I_D @ 25 °C	120	A
$R_{DS(on)}$	≤ 9.5	mΩ

2.2. Datasheet Status

There are three distinct types of datasheets, each corresponding to a different stage of the product development or documentation process, depending on the degree of completeness, correctness, or approval.

- **Target datasheet:** During product development, the term *target datasheet* denotes a document laying out the desired product specifications, characteristics, and performance attributes. The development team uses this document to guide their efforts.
- **Preliminary datasheet:** Created before reaching its final, approved format. It is an early or preliminary representation of a product's specifications, features, and characteristics. The difference between a preliminary datasheet and a final datasheet is that certain data values are still missing. The missing values in the preliminary data sheet are noted as to be defined (TBD). These datasheets are made using the engineering samples that are in early phase of development.
- **Final datasheet:** Detailed and authoritative document that contains all the values that were missing in the preliminary datasheet. The parameters specified in the final datasheet are explained in this document. Any major change with respect to a MOSFET's characteristics in the final datasheet is associated with a Product Change Notification (PCN).

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3. MOSFET Datasheet Parameters

This section serves as a thorough exploration of the various parameters detailed within a MOSFET's datasheet. It describes the MOSFET's performance and characteristics, from maximum ratings to static and dynamic parameters, thermal properties, and package-related factors.

3.1. Maximum Ratings

The maximum ratings at which the MOSFET can be operated are listed on the second page of the datasheet in a table that summarizes the electrical and thermal limits of the device. The maximum ratings provided in the data sheets are absolute in nature. If any of the maximum ratings are surpassed, it is to be expected that the semiconductor experiences fatal failure, regardless of whether the remaining maximum ratings are utilized to their full extent. Unless otherwise noted, the values are applicable at a virtual junction temperature (T_{vj}) of 25°C. **Table 2** lists the maximum ratings designated for the IXTH120N20X4.

Table 2. IXTH120N20X4 MOSFET Maximum Ratings

Symbol	Characteristic	Conditions		Value	Unit
V_{DSS}	Drain-source voltage	$25\ °C \le T_{vj} \le T_{vj(max)}$		200	V
V_{GSS}	Gate-source voltage	–		± 20	V
V_{GSM}	Transient gate-source voltage	$t_{transient}$ = 1 ms		± 30	V
I_D	Drain current	–	T_c = 25 °C	120	A
			T_c = 100 °C	89	A
I_{DM}	Peak drain current	T_c = 25 °C, Pulse width limited by $T_{vj(max)}$		240	A
I_S	Diode forward current	V_{GS} = 0 V		120	A
I_{SM}	Diode peak forward current	Pulse width limited by $T_{vj(max)}$		480	A
I_{AS}	Non-repetitive single pulse avalanche current	–		60	A
E_{AS}	Non-repetitive single pulse avalanche energy	–		1	J
dv/dt	Diode dv/dt capability	V_{DS} = 0..... 200 V, $I_S \le$ 120 A		20	V/ns
P_{tot}	Total power dissipation	T_c = 25 °C		417	W
T_{vj}	Virtual junction temperature range	–		−55 to +175	°C
$T_{vj(max)}$	Maximum virtual junction temperature	–		175	°C
T_{stg}	Storage temperature range	–		−55 to +175	°C
T_{sld}	Soldering temperature	1.6 mm (0.062 in.) from case 10 s		300	°C
M_s	Mounting torque for screws to heat sink	–		1.3/10	Nm/lb.in

Drain-source voltage (V_{DSS}) is the crucial parameter in datasheets, representing the maximum voltage that can be applied across drain and source while the gate and source are being connected or V_{GS} = 0 V. It sets the limit to prevent breakdown and maintain operational functionality.

Gate-source voltage (V_{GSS}) and **Transient gate-source voltage (V_{GSM})** are visually delineated in **Figure 3**, offering a clear understanding of their roles in MOSFET operation. The gate-source voltage (V_{GSS}) denotes the maximum steady-state voltage that can be applied across gate and source without the gate oxide being damaged. Conversely, transient gate-source voltage (V_{GSM}) refers to the peak voltage that the gate terminal of the MOSFET can endure within a specified transient period ($t_{transient}$) or temporary change in voltage.

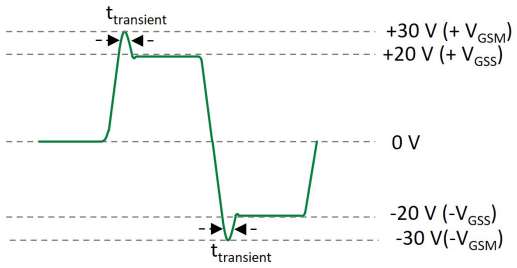

Figure 3. Gate-Source Voltage Definition

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Drain current (I_D) acts as a pivotal metric, outlining the maximum continuous current through the drain at a given case temperature T_c, of 25°C. Its calculation is based on several factors, including the maximum power dissipation P_{tot}, the temperature difference junction to case, the thermal resistance junction to case $R_{th(j-c)}$, and the maximum on-resistance $R_{DS(on)}$. Additionally, the temperature dependence of the on-state resistance is considered, as detailed in **Equation 1** and **Equation 2**. The drain current can be limited by the current handling capacity of leads or terminals.

$$P_{tot} = \frac{T_{vj(max)} - T_c}{R_{th(j-c)}} = I_D{}^2 \cdot R_{DS(on)}|_{T_{vj}=T_{vj(\max)}} \quad (1)$$

Solving for I_D as

$$I_D = \sqrt{\frac{T_{vj} - T_c}{R_{th(j-c)} \cdot R_{DS(on)}\ |_{T_{vj}=T_{vj(\max)}}}} \quad (2)$$

Peak drain current (I_{DM}) signifies the peak current that the device can handle above the I_D specification under the maximum virtual junction temperature. It varies with the current pulse width and heat dissipation conditions. **Figure 4** demonstrates the forward-bias safe operating area (FBSOA) of a MOSFET, which indicates the maximum pulse width at which the device can handle specific current without experiencing failure.

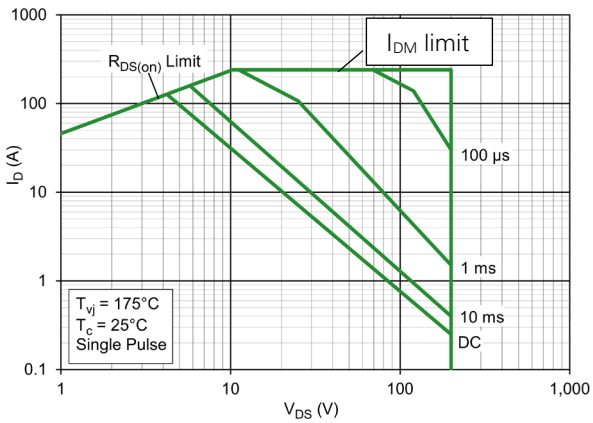

Figure 4. Forward-Bias Safe Operating Curve

Diode forward current (I_S) relates to the maximum DC forward current the body diode can handle in the forward direction at particular case temperature, which is typically equivalent to the MOSFET's continuous drain current I_D.

Diode peak current (I_{SM}) is an indicative of the peak current the diode can handle above diode forward current specification under maximum virtual junction temperature, which is typically equivalent or higher than the MOSFET's peak drain current I_{DM}.

Diode dv/dt capability corresponds to the maximum allowable rate of change of voltage across the body diode during the reverse recovery period without causing undesired effects. The power MOSFET structure contains a parasitic bipolar junction transistor (BJT), which could be activated by an excessive rise rate of the drain-source voltage (dv/dt), particularly after the recovery of the body diode.

Total power dissipation (P_{tot}), as expressed in Equation 1 , encompasses the maximum calculated power that the device can dissipate, serving as a function influenced by both maximum virtual junction temperature $T_{vj(max)}$, and the thermal resistance junction to case $R_{th(j-c)}$ at a case temperature of 25°C.

Virtual junction temperature (T_{vj}) range is –55 to 150°C or –55 to 175°C in most cases and it is the permissible temperature range in which the MOSFET may be operated continuously. The maximum virtual junction temperature $T_{vj(max)}$ is 150°C or 175°C depending on the technology. The negative temperature limit for Littelfuse discrete MOSFETs is typically –55 °C. The virtual junction temperature influences the electrical parameters of a MOSFET. For instance, at very high temperatures, the device's threshold voltage is reduced, and the leakage current increases, which leads to thermal runaway within the device.

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Storage temperature (T_{stg}) range points to the range of temperatures where the device can be safely stored or transported without adversely affecting its performance or reliability. The range is usually between –55°C to 150°C.

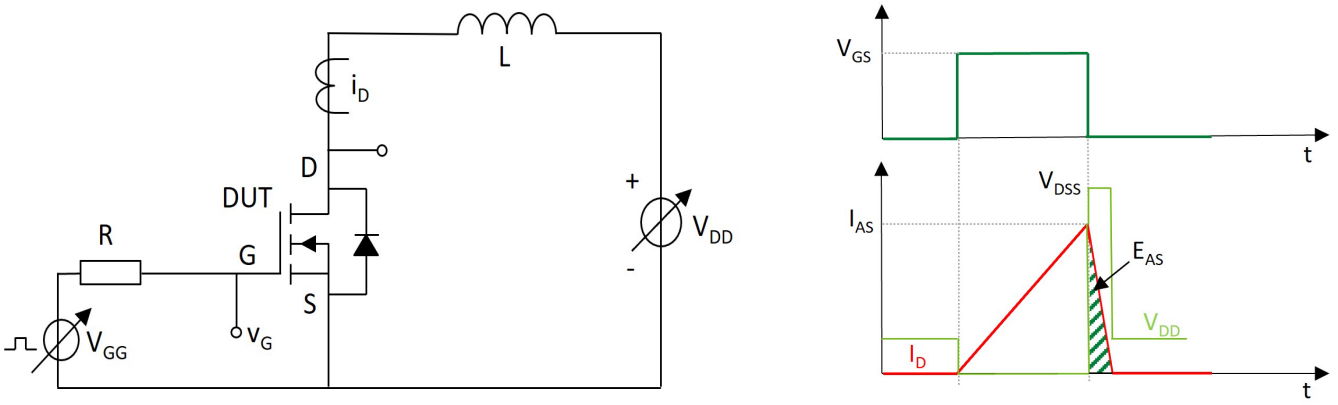
Soldering temperature (T_{sld}) enumerated in the datasheet implies the temperature at which the device can be safely soldered to the Printed Circuit Board (PCB) during the assembly process. The maximum soldering temperature is typically 300°C for devices with leads and 260°C for Surface Mount Devices (SMD).

Mounting torque (M_s) for screws to heatsink is the recommended maximum torque that can be applied during the process of mounting the MOSFET to a heatsink or a PCB. **Mounting torque (M_t)** for screws to terminals is the suggested torque that shall be applied to screwed terminals.

Mounting force (F) is the maximum force for pressure mounted devices, fixed by clips, that shall be applied to the isolated devices.

Non-repetitive single pulse avalanche current (I_{AS}) and Non-repetitive single pulse avalanche energy (E_{AS}) are specified only for avalanche-rated devices. I_{AS} denotes the maximum current that the MOSFET can endure during a single avalanche event without sustaining damage. Whereas E_{AS} quantifies the total energy absorbed by the device during such an event, indicating its ability to withstand high-energy transient events without permanent damage.

In **Figure 5 (a)**, the Unclamped Inductive Switching (UIS) test circuit, used to test the avalanche capability of a power MOSFET is depicted. In **Figure 5 (b)**, the waveforms during avalanche breakdown are presented. A gate pulse turns-on the MOSFET and allows the current (I_D) to ramp up according to the inductor's value (L) and the drain supply voltage (V_{DD}). At the end of gate pulse, the MOSFET turns-off causing the voltage across the MOSFET to rise sharply. The over voltage is clamped at the breakdown voltage (V_{DSS}) until the load current reaches zero and all the energy is dissipated. The green area shaded in **Figure 5 (b)** is the avalanche energy E_{AS}.



(a) Unclamped Inductive Switching

(b) Waveforms during Avalanche Breakdown

Figure 5. Typical Avalanche Test Circuit

Non-repetitive single pulse avalanche energy is calculated from the **Equation 3**:

$$E_{AS} = \frac{1}{2} \cdot L \cdot {I_{AS}}^2 \cdot \frac{V_{DSS}}{(V_{DSS} - V_{DD})} \qquad 3$$

where V_{DSS} is the drain-source avalanche voltage.

Note : When V_{DD} is set to a smaller value compared to V_{DSS}, then E_{AS} is calculated by using the approximation equation of $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2$

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3.2. Static Electrical Characteristics - MOSFET

Static electrical characteristics are the set of parameters and properties that describe the device behavior under steady-state condition. Most of the parameters included in the datasheet, along with their typical ranges of variance is listed in **Table 3**. In accordance with IEC 60747-8{ed3.1}, the characteristics of Power MOSFETs are provided at 25°C and, when necessary, at another higher operating temperature.

Table 3. MOSFET Static Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$V_{(BR)DSS}$	Breakdown voltage, drain-source	V_{GS} = 0 V, I_D = 250 µA		200	–	–	V
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA		2.5	–	4.5	V
I_{DSS}	Drain-source leakage current	V_{DS} = V_{DSS}, V_{GS} = 0 V	T_{vj} = 25 °C	–	–	25	µA
			T_{vj} ≤ 150 °C	–	–	500	
I_{GSS}	Gate leakage current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, I_D = 0.5 · I_D	T_{vj} = 25 °C	–	–	9.5	mΩ

Breakdown voltage, drain-source ($V_{(BR)DSS}$) corresponds to the minimal blocking voltage between drain and source, measured according to **Figure 6**, at a specified collector current while the gate and source are connected.

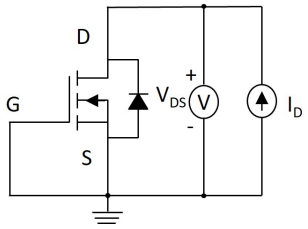

Figure 6. Circuit Diagram to Measure Breakdown Voltage

Gate-source threshold voltage ($V_{GS(th)}$) is the voltage measured across gate to source at which the drain current begins to flow, and the device is at on-state. It has a negative temperature coefficient. The circuit diagram illustrating the measurement of $V_{GS(th)}$ is depicted in **Figure 7**. Initially, the drain pin and the gate pin are short, after which drain current is applied while observing the gate-source voltage ($V_{GS(th)}$) reading.

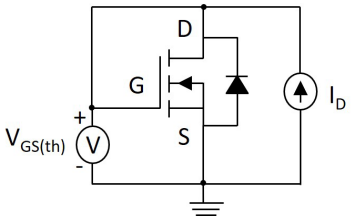

Figure 7. Circuit Diagram to Measure Gate-Source Threshold Voltage

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Drain-source leakage current (I_{DSS}) value indicates the drain current measured at a given drain-source voltage and with the gate to source connected, as illustrated in **Figure 8**. The datasheets specify the value at 25°C and higher virtual junction temperature.

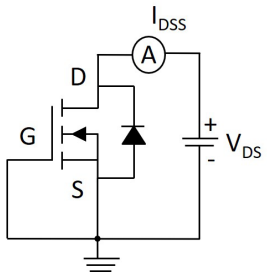

Figure 8. Circuit Diagram to Measure MOSFET's Leakage Current

Gate leakage current (I_{GSS}) refers to the small amount of current that flows between the gate and source when the MOSFET is in an off state. **Figure 9** demonstrates the circuit used to measure the gate leakage current. Initially, the drain-to-source terminal is connected, and then a maximum allowable voltage is applied across the gate and source terminals to monitor the leakage current.

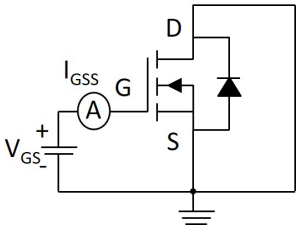

Figure 9. Circuit Diagram to Measure Gate Leakage Current

Drain-source on-state resistance ($R_{DS(on)}$) describes the resistance across the drain and source when the MOSFET is in the on-state. **Figure 10** presents the circuit diagram for measuring the drain-source on-state resistance ($R_{DS(on)}$). Initially, the gate-source voltage (V_{GS}) is set to a defined value, and then the voltage drop across the drain-source voltage $V_{DS(on)}$ is measured, using a given current source (I_D). $R_{DS(on)}$ is calculated using the **Equation 4**:

$$R_{DS(on)} = \frac{V_{DS(on)}}{I_D} \quad (4)$$

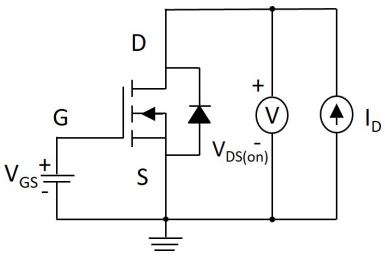

Figure 10. Circuit Diagram to Measure Gate Drain-Source On-State Resistance

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3.3. Dynamic Characteristics

This section of the datasheet provides information on the behavior of the device in dynamic conditions, as shown in **Table 4**. The intrinsic capacitances, gate charge and switching behavior of the MOSFET are pivotal factors influencing the dynamic performance of the device.

Table 4. Dynamic Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$R_{g(int)}$	Internal gate resistance	f = 1 MHz, open drain		–	6	–	Ω
C_{iss}	Input capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	6100	–	pF
C_{oss}	Output capacitance			–	865	–	
C_{rss}	Reverse transfer capacitance			–	1.8	–	
$C_{oss(er)\ eff.}$	Effective output capacitance, energy related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V		–	510	–	pF
$C_{oss(tr)\ eff.}$	Effective output capacitance, time related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V, I_D = constant		–	2000	–	pF
Q_G	Gate charge	V_{DD} = 0.5 · V_{DSS}, V_{GS} = 10 V, I_D = 0.5 · I_D		–	108	–	nC
Q_{GS}	Gate-source charge			–	27	–	
Q_{GD}	Gate-drain charge			–	27	–	
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 0.5 · I_D		72	120	–	S
$t_{d(on)}$	Turn-on delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	13	–	ns
t_r	Rise time		T_{vj} = 25 °C	–	24	–	
t_{on}	Turn-on time		T_{vj} = 25 °C	–	37	–	
$t_{d(off)}$	Turn-off delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	100	–	ns
t_f	Fall time		T_{vj} = 25 °C	–	12	–	
t_{off}	Turn-off time		T_{vj} = 25 °C	–	112	–	

Internal gate resistance ($R_{g(int)}$) signifies the resistance that exists within the device gate structure. The internal gate resistance mentioned in **Figure 11**, constitutes a component of the parasitic elements within the MOSFET. Together with the MOSFET's input capacitance, the gate resistance forms an RC network that determines the voltage change at the MOSFET gate and thus the switching time.

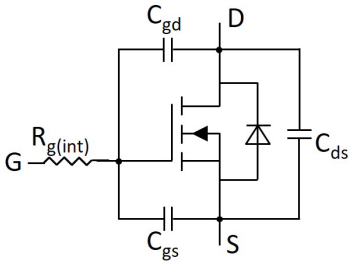

Figure 11. Power MOSFET Parasitic Components

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Capacitance Characteristics play a crucial role in switching characteristics of the MOSFET.

- **Input capacitance (C_{iss})** encompasses both gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs}, representing the total capacitance measured between the gate and source terminals with the drain connected to the source terminal.

$$C_{iss} = C_{gs} + C_{gd} \quad (5)$$

- **Output capacitances (C_{oss})** consists of the drain-to-source capacitance C_{ds} and gate to drain capacitance C_{gd}, indicating the output capacitance which is measured between the drain and source with the gate connected to the source terminal.

$$C_{oss} = C_{ds} + C_{gd} \quad (6)$$

- **Reverse transfer capacitance (C_{rss})** primarily arises from C_{gd}, delineating the capacitance between the gate and drain with the source terminal connected to ground.

$$C_{rss} = C_{gd} \quad (7)$$

Effective output capacitance of the MOSFET includes both energy related and time related parameters, denoted as $C_{oss(er)}$ and $C_{oss\ (tr)}$ respectively. $C_{oss(er)}$ represents a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to specified voltage. Conversely, $C_{oss(tr)}$ signifies a fixed capacitance that gives the same charging time as a C_{oss} while V_{DS} is rising from 0 V to specified voltage and at a constant drain current I_D.

Total gate charge (Q_G) is the total amount of charge that is required during the MOSFET's turn-on and turn-off transition. The switching speed depends on the speed at which a gate driver can charge or discharge the input gate charge. **Figure 12** presents a typical gate charge waveform for a power MOSFET in a resistive-load circuit. The fundamental equation for calculating the gate charge is formulated in **Equation 8**.

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t)dt \quad (8)$$

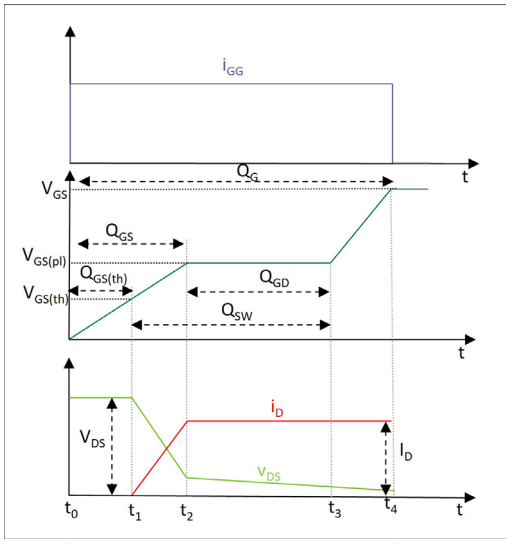

Figure 12. Gate Charge Waveform of Power MOSFET during Turn-on Transition with Resistive Load

As depicted in the gate charge waveform, the total gate charge encloses the **Gate-Source Charge (Q_{GS})**, the **Gate-Drain Charge (Q_{GD})**, and the **Gate Switch charge (Q_{SW})**. Q_{GS} represents the amount of charge that is required to charge the gate-source capacitance (C_{gs}) from its initial voltage to the miller plateau level. Q_{GD} quantifies the charge that is needed to fully charge the gate-drain capacitance (C_{gd}) during switching, ensuring full channel enhancement and sustaining the MOSFET in its conducting state. Lastly, Q_{SW} encapsulates charge stored in the gate capacitance from when the gate-source voltage has reached the gate-source threshold voltage, $V_{GS(th)}$ until the end of the miller plateau.

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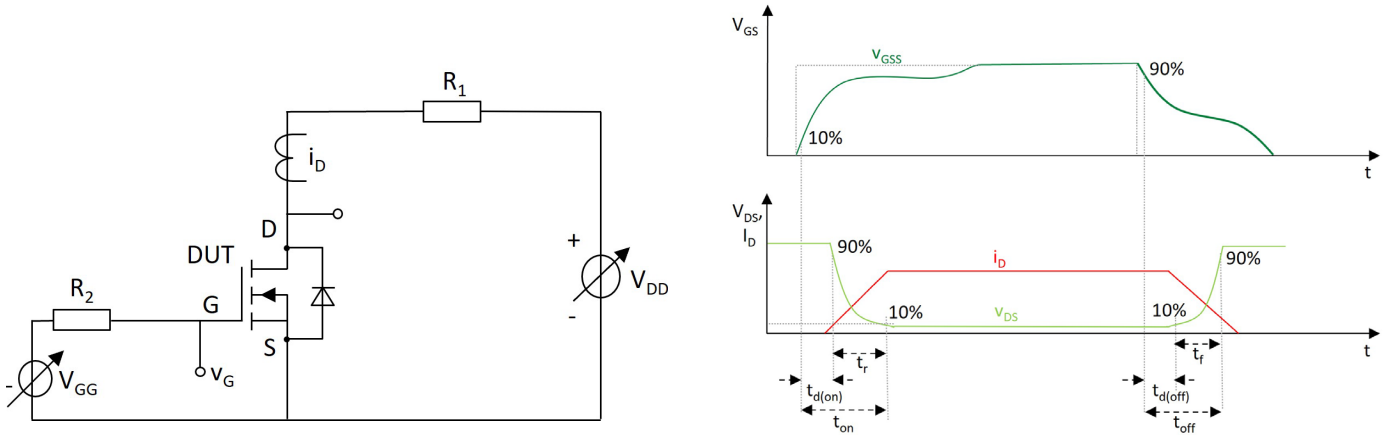
Transconductance (g_{fs}) is described as the change in drain current divided by the change in gate voltage for a constant drain voltage. A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. The transconductance is mathematically expressed as:

$$g_{fs} = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS\,=\,constant}} \qquad 9$$

MOSFETs, due their physical structure, can change their state from on to off much faster than IGBTs. The correlations of switching time measurement circuit and the switching time definitions are demonstrated **Figure 13**.



(a) Switching Time Measurement Circuit Diagram

(b) Switching Time Definition Waveform

Figure 13. Correlation of Switching Time Measurement Circuit and Switching Time Definition

- **Turn-on delay time ($t_{d(on)}$)** is the time interval when the gate-source voltage (V_{GS}) has reached 10% of its end value, to the time when the drain-source voltage (V_{DS}) has dropped to 90% of its initial value or rated value.
- **Rise time (t_r)** specifies the time interval between the drain-source voltage dropping from 90% to 10% of its initial value. The drain current starts to rise, and a major part of turn-on losses is generated during this period.
- **Turn-off delay time ($t_{d(off)}$)** denotes the time interval between the moment when the gate-source voltage (V_{GS}) has declined to 90% of its initial value and the drain-source voltage has risen to 10% of the supply voltage.
- **Fall time (t_f)** implies the time interval between the drain-source voltage rise from 10% to 90% of its end value. During this period, the drain current starts to fall, and a major part of turn-off losses is generated during this time.

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3.4. Electrical Characteristics – Body Diode

Power MOSFET generally contain a body diode, which provides freewheeling operation in the inductive load switching. Hence, the MOSFET datasheet from Littelfuse also contains the electrical parameters and graphs related to the body diode. **Table 5** shows the electrical characteristics listed in IXTH120N20X4 datasheet.

Table 5. Electrical Characteristics – Body Diode

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{SD}	Diode forward voltage	V_{GS} = 0 V, I_S = 100 A [1]	–	–	1.4	V
t_{rr}	Diode reverse recovery time	V_{DD} = 100 V, I_S = 60 A, $-di_S/dt$ = 200 A/µs	–	190	–	ns
Q_{rr}	Reverse recovery charge		–	3.2	–	µC
I_{rrm}	Peak reverse recovery current		–	33.7	–	A

Note 1: Pulse test, t ≤ 300 µs, duty cycle, d ≤ 2%

Diode forward voltage (V_{SD}), measured under specified conditions including a given forward current (I_S), zero gate-source voltage (V_{GS}), and a virtual junction temperature of 25°C, symbolizes the maximum forward voltage drop across the intrinsic diode, as illustrated in **Figure 14**.

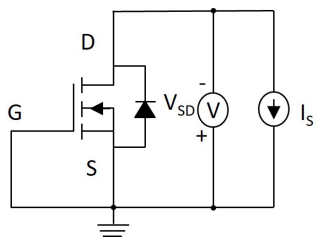
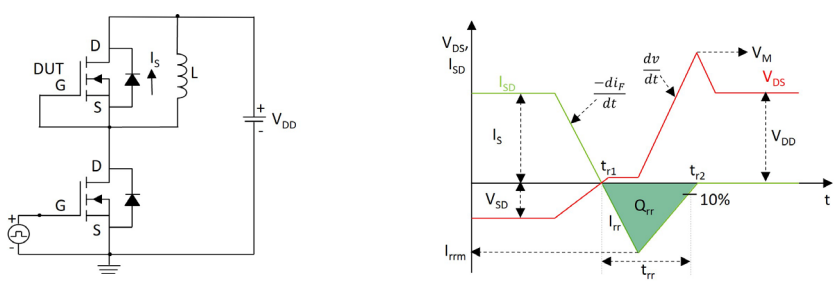


Figure 14. Circuit Diagram to Measure Diode Forward Voltage

Reverse recovery charge (Q_{rr}) characterizes the charge that is built up in the diode during the transition from the conducting or forward bias state to the non-conducting or reverse-biased state. The time that is necessary to remove the charge that persists within the diode during the reverse recovery phase is called **Diode Reverse Recovery Time (t_{rr})**. **Peak Reverse Recovery Current (I_{rrm})** denotes the maximum current flowing in the reverse direction during this period.

The circuit diagram and reverse recovery measurement waveforms are demonstrated in **Figure 15**. Mathematically, the reverse recovered charge, Q_{rr}, is defined as the integral of the reverse recovery current, I_{rr}, during the process of current commutation, with time as the variable. This relationship is expressed by **Equation 10**. The reverse recovery time, t_{rr}, is measured from the point of reverse bias initiation to the moment when the reverse current reaches 10% of its peak value.

$$Q_{rr} = \int_{t_{r1}}^{t_{r2}} I_{rr}(t)dt \qquad 10$$



(a) Measurement Circuit (b) Waveform

Figure 15. Diode Reverse Recovery

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3.5. Thermal Characteristics – Thermal Resistance (R_{th})

R_{th} signifies the thermal characteristics of the MOSFET at steady state, making it an essential parameter for thermal management of the MOSFET. **Table 6** outlines the R_{th} values presented in the datasheet. The heat generated within the silicon chip needs to be dissipated by means of heat sink into the ambient. The thermal dissipation pathway for a power MOSFET in a conventional and isolated discrete package with a heat sink is visually outlined in **Figure 16 (a) and (b)**.

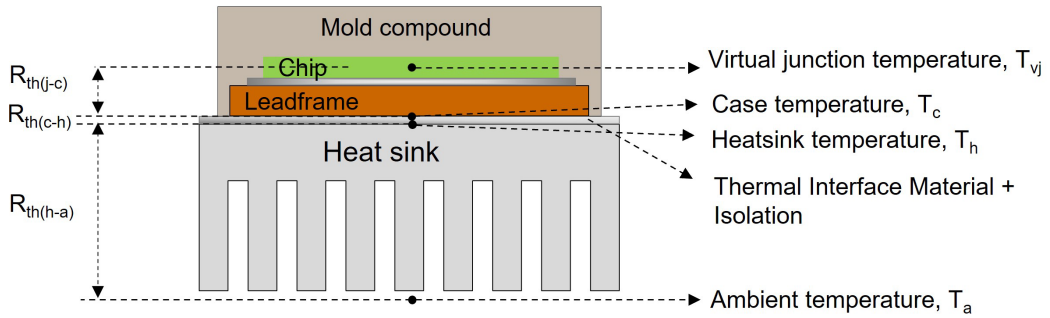
Table 6. Thermal Characteristics

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance junction to case – MOSFET	–	–	–	0.36	K/W
$R_{th(c-h)}$	Thermal resistance case to heat sink – MOSFET	–	–	0.21	–	K/W

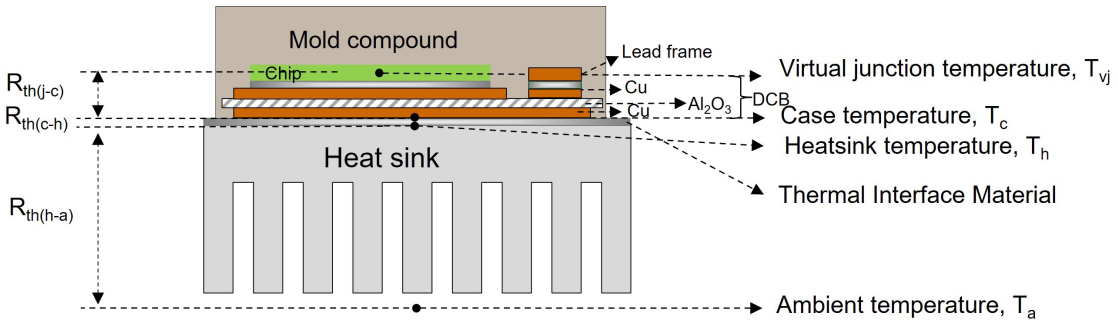
Thermal resistance junction to case ($R_{th(j-c)}$) is the thermal resistance from the junction of the die to the outside of the device's case. It describes the passage of heat between the semiconductor chip and the case. Littelfuse specifies a maximum static $R_{th(j-c)}$ at T_{vj} = 125°C.

Thermal resistance case to heatsink ($R_{th(c-h)}$) characterizes the static heat dissipation of a MOSFET and depends on module size, heatsink, case surfaces, thickness parameters of thermal layers between module and heatsink.

Thermal resistance junction to ambient ($R_{th(j-a)}$) is equal to sum of junction to case, $R_{th(j-c)}$, case to heatsink $R_{th(c-h)}$ and heatsink to ambient thermal resistance, $R_{th(h-a)}$. The $R_{th(j-c)}$ is specified in the datasheet whereas $R_{th(c-h)}$ and $R_{th(c-a)}$ is determined by the user's board design and depends on the application.



(a) Conventional Discrete Package



(b) Isolated Discrete Package

Figure 16. Lateral Thermal Resistance Chain within a Semiconductor Package

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3.6. Package – Mechanical Rating

This part of the datasheet covers physical characteristics of the device.

Package weight (G) refers to the mass of the package or housing, including the MOSFET die and the required electrical and thermal connections.

Isolation voltage (V_{isol}) is specified only for isolated devices and represents the isolation voltage between all terminals connected against the cooling surface or base plate. The verification test circuit used to determine the isolation voltage rating between terminals and baseplate is visualized in **Figure 17**.

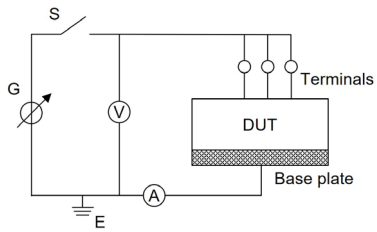

Figure 17. Circuit Diagram for Isolation Withstand Voltage Test

3.7. Characteristics Curves

The essential curve in the datasheet provides graphical portrayal of key performance characteristics of MOSFET devices. In this application note, the graphs, and parameters from the IXTH120N20X4 datasheet are used as reference.

Typical Output Characteristics of IXTH120N20X4, illustrating various modes of operation, are delineated in **Figure 18**. In the Cut-off region, the gate-source voltage (V_{GS}) is less than the gate-threshold voltage ($V_{GS(th)}$) and the device is an open circuit or off. In the *Ohmic region*, the device acts as a resistor with an almost constant on-resistance $R_{DS(on)}$ and which is equal to V_{DS} /I_D. In the linear-mode of operation, the device operates in the *Current-Saturated* region where the drain current (I_D) is a function of the gate-source voltage (V_{GS}) and defined by the **Equation 11**:

$$I_D = K \cdot \left(V_{GS} - V_{GS(th)}\right)^2 = g_{fs} \cdot \left(V_{GS} - V_{GS(th)}\right) \quad \textbf{11}$$

In this equation, K is a parameter depending on temperature and device geometry and g_{fs} is the current gain or transconductance. When the drain-source voltage (V_{DS}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. This reduction in surface potential continues as V_{DS} increases until it reaches a critical point, known as the *Channel Pinch-off Voltage*, where the drain voltage equals $\left(V_{GS} - V_{GS(th)}\right)$. At this point, the drain current becomes saturated.

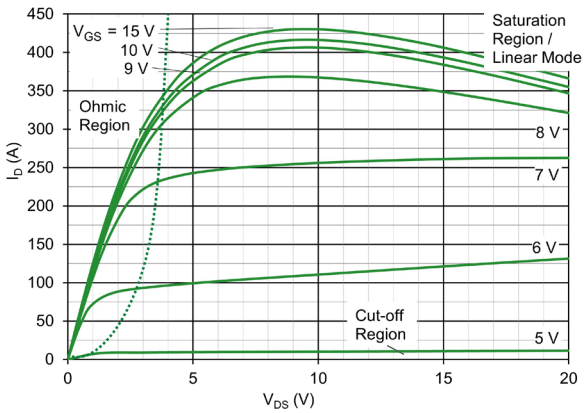

Figure 18. Typical Output Characteristics

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Typical Transfer Characteristics depicted in **Figure 19**, illustrates the relationship between drain current and gate voltage across varying temperatures of –40, 25, and 150°C. The intercepts of these lines at I_D = 0 A provides the threshold voltages for the respective temperature. It can be concluded that the transfer characteristic depends on both temperature and drain current and the threshold voltage decreases with increasing temperature.
In certain scenarios, a cross-over point or zero temperature coefficient point may be present. Below this point, the gate-source voltage exhibits a negative temperature coefficient, implying a decrease in gate-source voltage at higher temperatures for a given drain current. Conversely, above this point, the temperature coefficient for the gate-source voltage becomes positive.

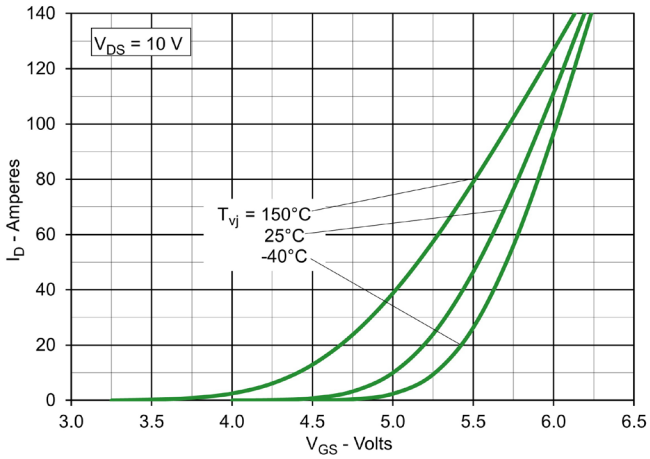

Figure 19. Typical Transfer Characteristics

Typical Drain-Source On-State Resistance (Normalized) vs. Virtual Junction Temperature - The value of $R_{DS(on)}$ is critical in power MOSFETS as it serves as an indicator of the device's capacity to handle current. An important characteristic is an increase in the on-resistance with increasing temperature, as evidenced in **Figure 20**, which portrays a positive temperature coefficient. The positive temperature coefficient of $R_{DS(on)}$ is a beneficial feature when paralleling power MOSFETs because it ensures thermal stability and balanced current sharing.

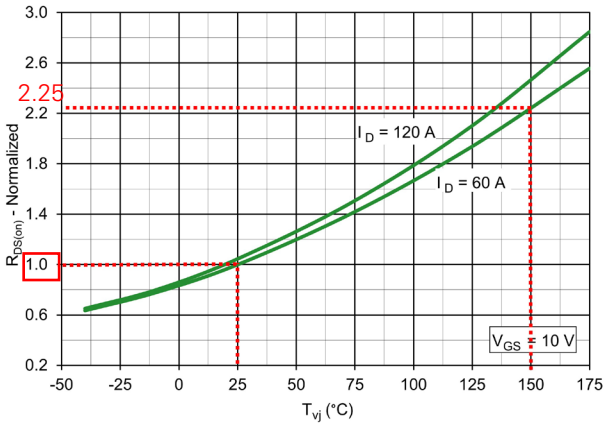

Figure 20. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Virtual junction temperature

From **Figure 20**, $R_{DS(on)}$ vs. T_{vj} (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at T_{vj} = 25°C, and it increases to 2.25 at T_{vj} = 150°C. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., 0.5·I_{D25}) is specified as 9.5 mΩ at T_{vj} = 25°C, then it is predicted that it will change to 21.375 mΩ when Tvj = 150°C is applied. The normalized value is obtained from $R_{DS(on)}|T_{vj}$ / $R_{DS(on)}|T_{vj}$ = 25°C.

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Typical Drain-Source On-State Resistance (Normalized) vs. Drain Current presented in **Figure 21** provides information about the relative change in on-state resistance at different drain currents. The calculation of the on-state resistance, $R_{DS(on)}$ as a function of drain current I_D and gate-source voltage V_{GS} can be derived from the typical output characteristic diagram depicted in **Figure 18,** employing Ohm's Law.

$$R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D} \quad (12)$$

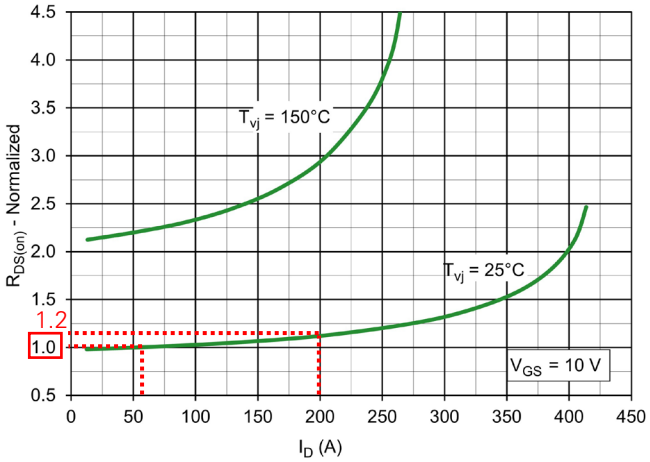

Figure 21. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Drain Current

From **Figure 21**, $R_{DS(on)}$ vs. I_D (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at I_D = 60 A, and it changes to 1.2 at I_D = 200 A. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., 0.5·I_{D25}) is specified as 9.5 mΩ, then it is predicted that the resistance $R_{DS(on)}$ will change to 11.4 mΩ when I_D = 200 A is applied. The normalized value is obtained from $R_{DS(on)}|I_D$ / $R_{DS(on)}|I_D$ = 60 A.

Typical Breakdown Voltage and Gate Threshold Voltage (Normalized) vs. Virtual Junction Temperature - The relationship between $V_{(BR)DSS}$ / $V_{GS(th)}$ and T_{vj} is expressed in **Figure 22**. The breakdown-voltage $V_{(BR)DSS}$ features a positive temperature coefficient, whereas gate-source threshold voltage $V_{GS(th)}$ has a negative temperature coefficient. At 25°C, the normalized breakdown-voltage $V_{(BR)DSS}$ is 1, growing to value of 1.14 at 150°C. This signs that breakdown-voltage $V_{(BR)DSS}$ at T_{vj} = 25°C is 200 V and is expected to be 228 V at T_{vj} = 150°C. The value of gate-source threshold voltage $V_{GS(th)}$ is 1 at 25°C and 0.643 at 150°C, respectively. Assuming the device's gate-source threshold voltage $V_{GS(th)}$ is 3.5 V, then the $V_{GS(th)}$ remains at 3.5 V at T_{vj} = 25°C, but is anticipated to decrease to 2.24 V at T_{vj} = 150°C.

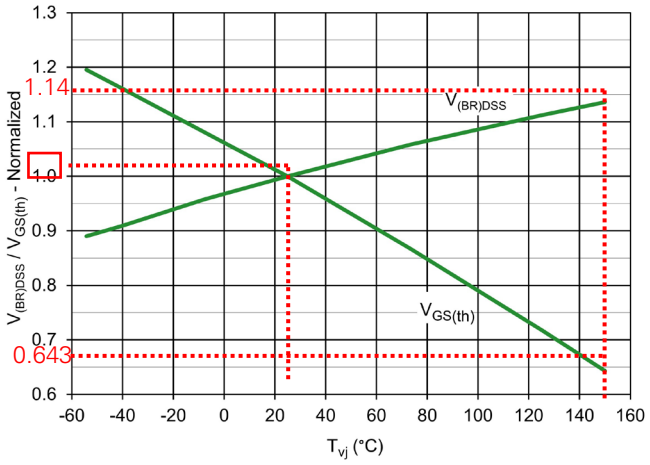

Figure 22. Typical $V_{(BR)DSS}$/$V_{GS(th)}$ (Normalized) vs. Virtual Junction Temperature

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Drain Current vs. Case temperature curve illustrated **Figure 23** depicts the solution of **Equation 2** across different case temperatures, demonstrating that at low case-temperature T_c, the maximum drain current I_D remains constant, while at high case-temperature T_c, it gradually decreases until reaching zero at $T_c = T_{vj(max)}$. However, the actual drain current is restricted by additional factors, including bond wire diameter, chip design, and assembly. It is noteworthy that, in certain instances, the continuous current is constrained by the package leads, although the switched current could potentially be higher.

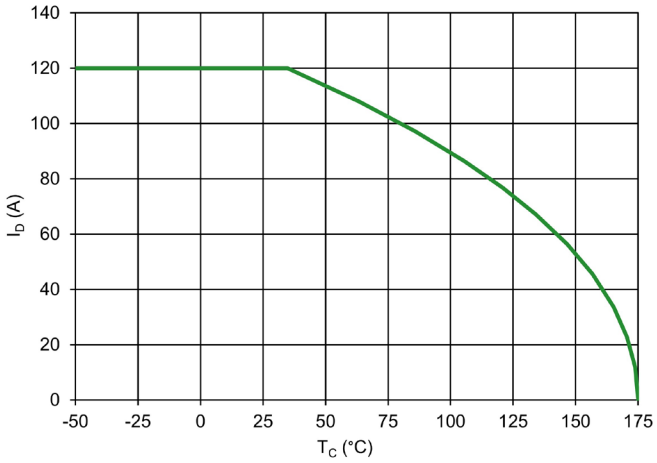

Figure 23. Drain Current vs. Case Temperature

Typical Transconductance - A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. **Figure 24** displays a typical variation of the transconductance with respect to drain current. The reduction in the mobility with increasing temperature adversely affects the transconductance.

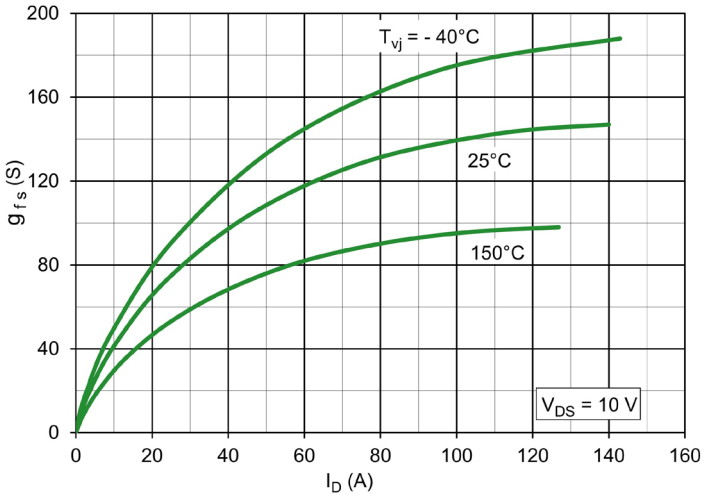

Figure 24. Typical Transconductance Curve

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Typical Gate Charge curve depicts the typical variation of the requisite gate charge to switch on the device at a specified V_{GS} and V_{DD}. A typical gate charge waveform for a power MOSFET can be observed in **Figure 25**. The gate charge reflects the charge stored on the inter-terminal capacitances and is used in designing the gate drive circuit.

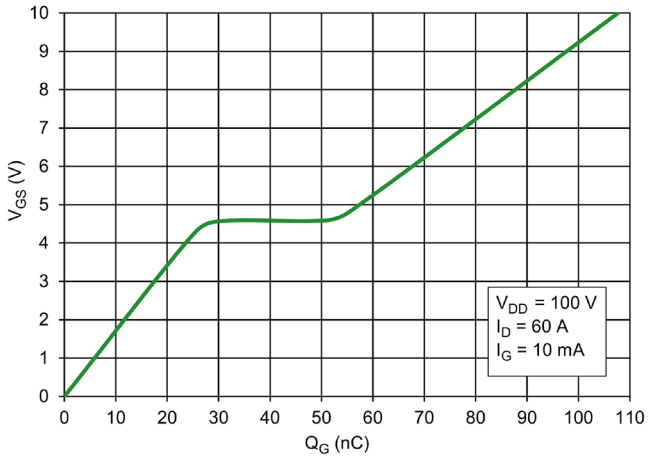

Figure 25. Typical Gate Charge Characteristics

In **Figure 26**, the parasitic **Junction Capacitances Characteristics** are represented as a function of drain-source voltage. Its components include input capacitance (C_{iss}), which consists of gate-source capacitance C_{GS} in parallel with drain-gate capacitance C_{DG}, output capacitance (C_{oss}), which consists of drain-gate capacitance C_{DG} in parallel with drain-source capacitance C_{DS} and reverse transfer capacitance (C_{rss}), which is the drain-gate capacitance C_{DG}.

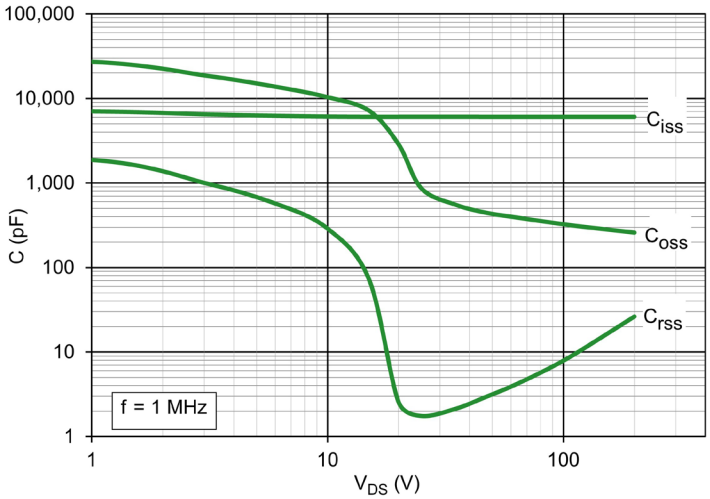

Figure 26. Typical Junction Capacitance

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Forward-Bias Safe Operating Area (FBSOA) is a datasheet figure of merit that defines the maximum allowed operating points. **Figure 27** shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bound by the maximum drain-to-source voltage V_{DSS}, maximum conduction current I_{DM}, maximum drain-source on-state resistance and constant power dissipation lines for various pulse durations.

In **Figure 27**, there is a series of curves that include a DC line along with four single pulse operating lines, 10 ms, 1 ms, and 100 µs. The top of each line is limited by the maximum drain current and is bounded by a positive sloped line defined by the on-state resistance $R_{DS(on)}$ of the device. The right-hand side of each line is terminated at the rated drain-source voltage limit V_{DSS}. Each line has a negative slope and is determined by the maximum power dissipation P_{tot} of the device:

$$P_{tot} = \frac{[T_{vj,max} - T_c]}{Z_{th(j-c)}} = V_{DS} \cdot I_D \qquad 13$$

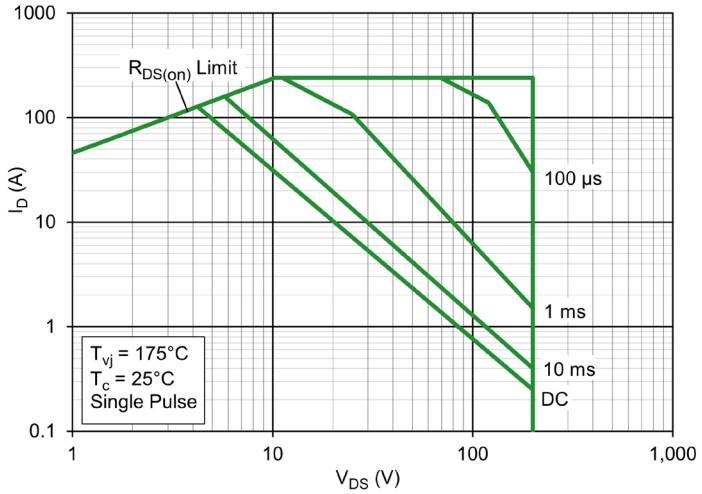

Figure 27. Forward Biased Safe Operating Area (FBSOA) Curve

These theoretical constant power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFET. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, as a result of lateral heat flow. Secondly, material imperfections like die attach voids and thermal grease cavities may cause local decrease of thermal conductivity. Additionally, fluctuations in dopant concentrations, gate oxide thickness and fixed charge will cause fluctuations of the local threshold voltage and the current gain (g_{fs}) of individual MOSFE's cells, which will also affect the local temperatures of the die.

Die temperature variations are mostly harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than the time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications are known to have limited capability to operate in the right-side bottom corner of the FBSOA graph.

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Typical Forward Characteristics of a Reverse Diode plotted against various temperatures are presented in **Figure 28**. This curve aids in comprehending the diode's conduction behavior and its forward voltage drop characteristics. It clearly demonstrates the negative temperature coefficient of diode forward voltage V_{SD} in the low-current region. As a result, it is anticipated that the diode forward voltage will decrease as the temperature increases. In the high-current region that is above the cross-over point (Q), the diode forward voltage will increase as the temperature increases.

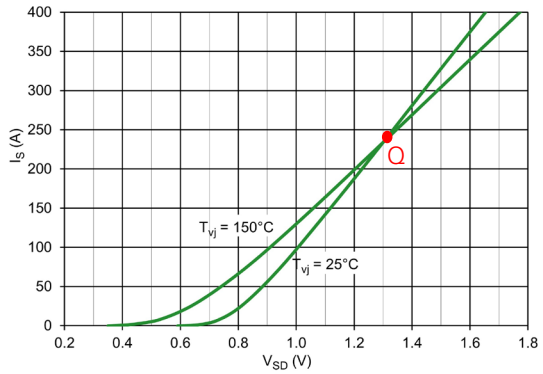

Figure 28. Typical Forward Characteristics of a Reverse Diode

Typical E_{oss} vs. Drain-Source Voltage - E_{oss} refers to the output switching energy. Specifically, it represents the energy that is required to charge or discharge output capacitance of a MOSFET during the switching operation.

$$Q_{oss} = \int_0^{V_{DS}} C(v)\ dv \qquad 14$$

$$E_{oss} = Q_{oss} \cdot V_{DS} \qquad 15$$

Where in this equation, Q_{oss} is the amount of charge required for charging the drain-source capacitance and C(v) is a function of the output capacitance C_{oss} that is dependent on drain to source voltage V_{DS} as shown in **Figure 29**.

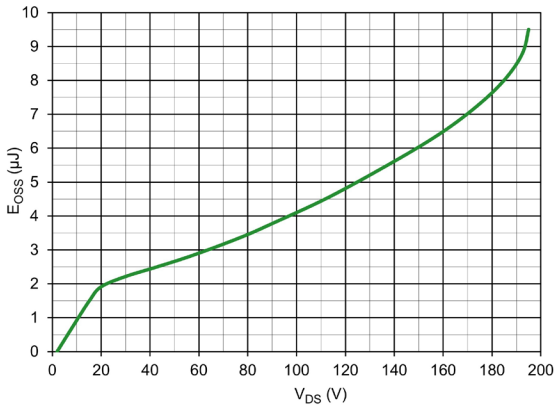

Figure 29. Typical E_{oss} vs. Drain-Source Voltage

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Typical Transient Thermal Impedance - A Power MOSFET has a virtual junction temperature, T_{vj} limitation. It should be operated below the maximum virtual junction temperature, $T_{vj(max)}$ specified in the datasheet to ensure reliability. The heat generated within the silicon chip needs to be dissipated by means of a heat sink into the ambient environment. The virtual junction temperature's rise above the ambient temperature T_a and is directly proportional to this heat flow and the junction-to-ambient thermal resistance, $R_{th(j-a)}$. The steady-state virtual junction temperature can be calculated by:

$$T_{vj} = P_{tot} \cdot R_{th(j-a)} + T_a|_{T_{vj} \leq T_{vj(max)}} \quad (16)$$

Here, P_{tot} is the maximum power dissipated in the junction. The total thermal resistance between junction and ambient is,

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad (17)$$

The steady-state thermal resistance is not sufficient when calculating the peak virtual junction temperatures for pulsed applications. When a power pulse is applied to the device, the peak virtual junction temperature varies depending on peak power and pulse width. The temperature swing due to short pulses of power can be calculated using the thermal impedance Z_{th}.

$$Z_{th(j-c)}(t) = r(t) \cdot R_{th(j-c)} \quad (18)$$

Here, r(t) is a time dependent factor that is defined by the thermal capacity of the device. For short pulses, the r(t)-value is small but for long pulse, it approaches 1, which means that the thermal impedance approaches the steady-state thermal resistance. A typical thermal impedance curve is shown in **Figure 30**, approaching the steady-state value for pulses exceeding a duration of about one second. The thermal impedance can be used to estimate the peak temperature rise for square wave power pulses, which is typical in power supply design circuits.

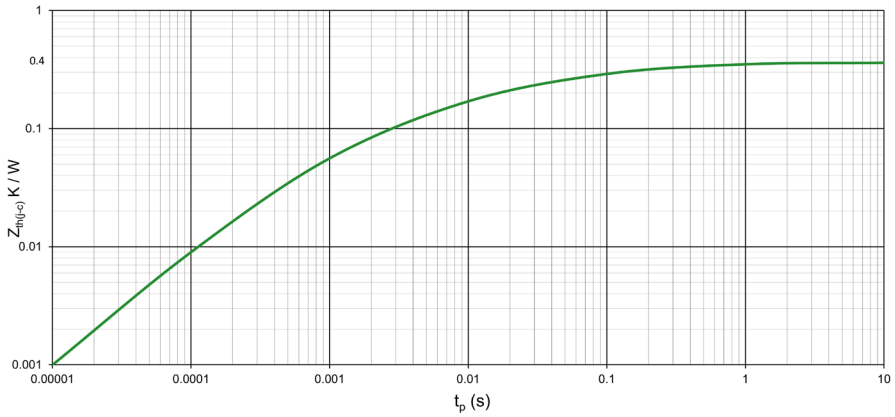

Figure 30. Typical Thermal Impedance

For additional information please visit www.Littelfuse.com/powersemi

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