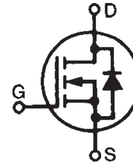
IXYS

PolarHT™ Power MOSFET

IXTQ 96N15P
IXTT 96N15P

V_{DSS} = 150 V
I_{D25} = 96 A
$R_{DS(on)}$ ≤ 24 mΩ

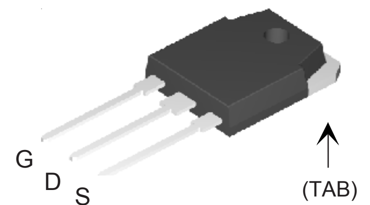
N-Channel Enhancement Mode
Avalanche Rated



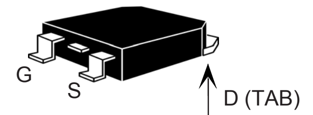
Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25° C to 150° C	150	V
V_{DGR}	T_J = 25° C to 150° C; R_{GS} = 1 MΩ	150	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25° C	96	A
$I_{D(RMS)}$	External lead current limit	75	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}	250	A
I_{AR}	T_C = 25° C	60	A
E_{AR}	T_C = 25° C	40	mJ
E_{AS}	T_C = 25° C	1.0	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤100 A/µs, $V_{DD} \leq V_{DSS}$ T_J ≤150° C, R_G = 4 Ω	10	V/ns
P_D	T_C = 25° C	480	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
T_{SOLD}	Plastic body for 10 s	260	°C
M_d	Mounting torque (TO-3P)	1.13/10	Nm/lb.in.
Weight	TO-3P	5.5	g
	TO-268	5.0	g

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	150			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	V_{DS} = V_{DSS}			25	µA
	V_{GS} = 0 V T_J = 125° C			250	µA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.5 I_{D25} Pulse test, t ≤300 µs, duty cycle d ≤ 2 %			24	mΩ

TO-3P (IXTQ)



TO-268 (IXTT)



G = Gate D = Drain
S = Source TAB = Drain

Features

- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect

Advantages

- Easy to mount
- Space savings
- High power density

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Symbol	Test Conditions	Characteristic Values (T_J = 25° C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V; I_D = 0.5 I_{D25}, pulse test	35	45		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3500		pF
C_{oss}			1000		pF
C_{rss}			280		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 60 A R_G = 4 Ω (External)		30		ns
t_r			33		ns
$t_{d(off)}$			66		ns
t_f			18		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		110		nC
Q_{gs}			26		nC
Q_{gd}			59		nC
R_{thJC}				0.31	° C/W
R_{thCS}	(TO-3P)		0.21		° C/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25° C, unless otherwise specified) Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			96	A
I_{SM}	Repetitive			250	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤300 μs, duty cycle d≤ 2 %			1.5	V
t_{rr}	I_F = 25 A, -di/dt = 100 A/μs		150		ns
Q_{RM}	V_R = 100 V, V_{GS} = 0 V		2.0		μC

TO-3P (IXTQ) Outline

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – DRAIN (COLLECTOR)

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP	.126	.134	3.20	3.40
øP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

TO-268 (IXTT) Outline

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

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IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405B2 6,759,692 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2

Fig. 1. Output Characteristics @ 25ºC

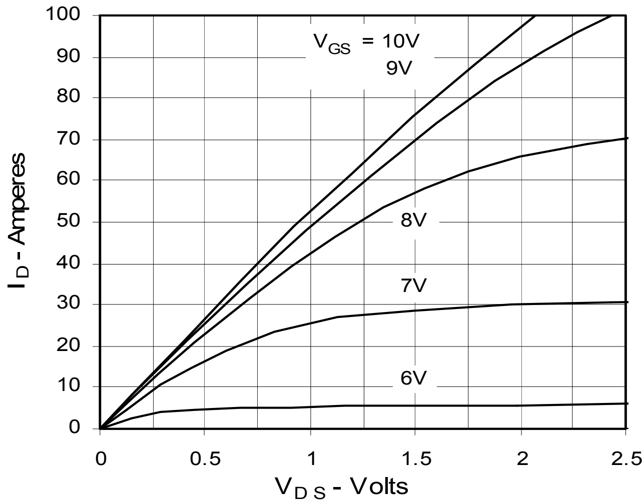


Fig. 2. Extended Output Characteristics @ 25ºC

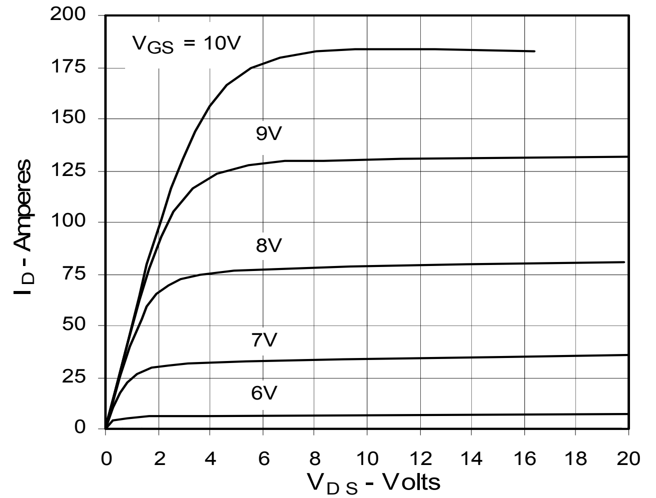


Fig. 3. Output Characteristics @ 150ºC

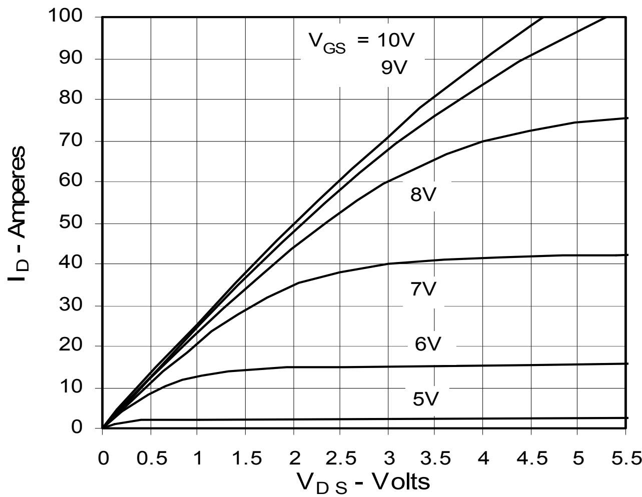


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

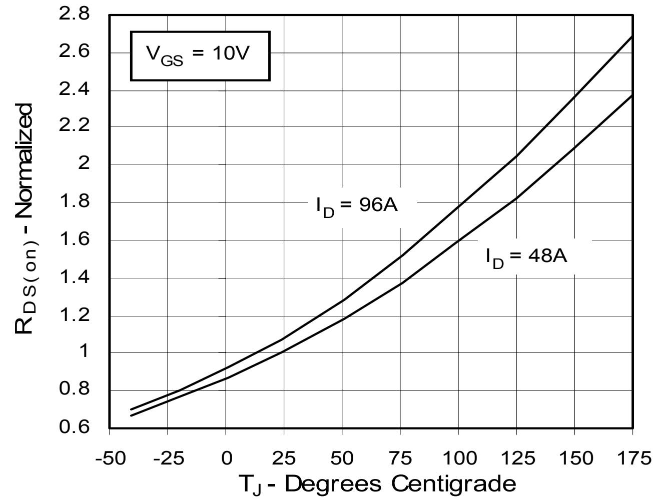


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

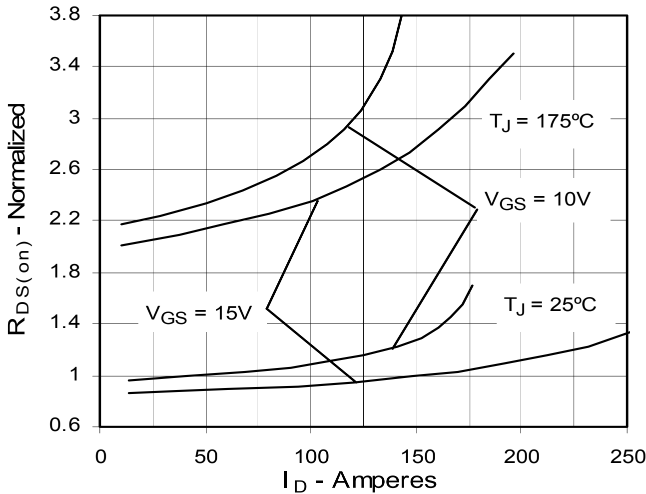
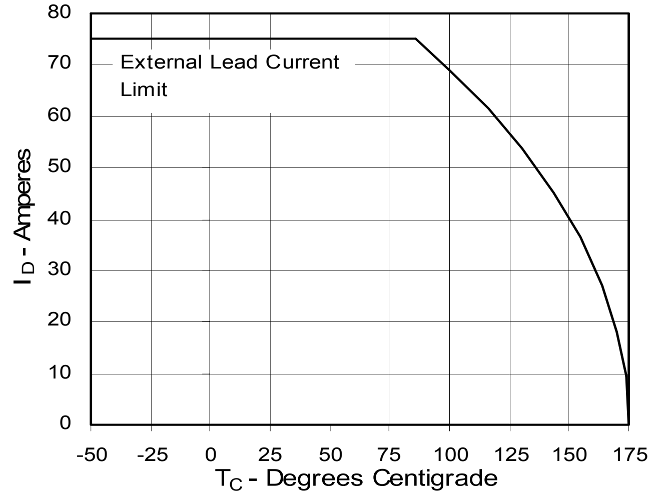


Fig. 6. Drain Current vs. Case Temperature



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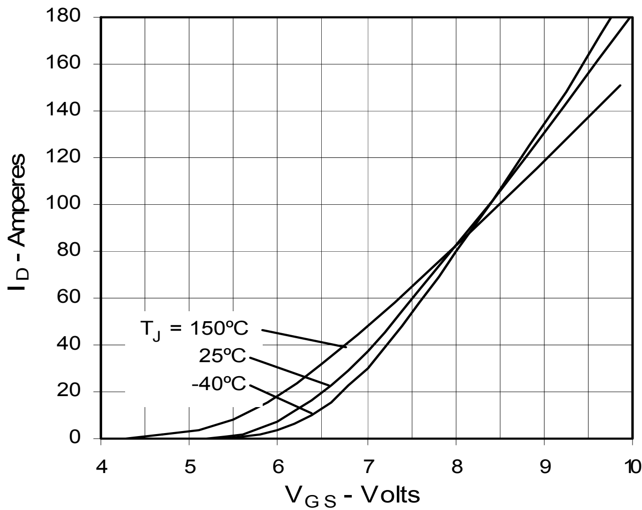

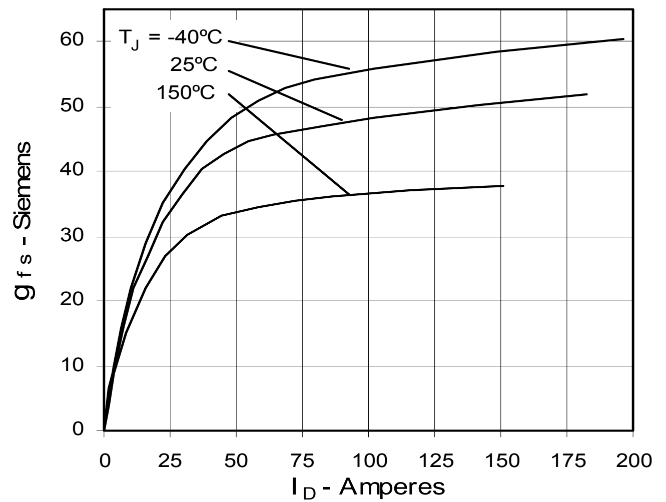

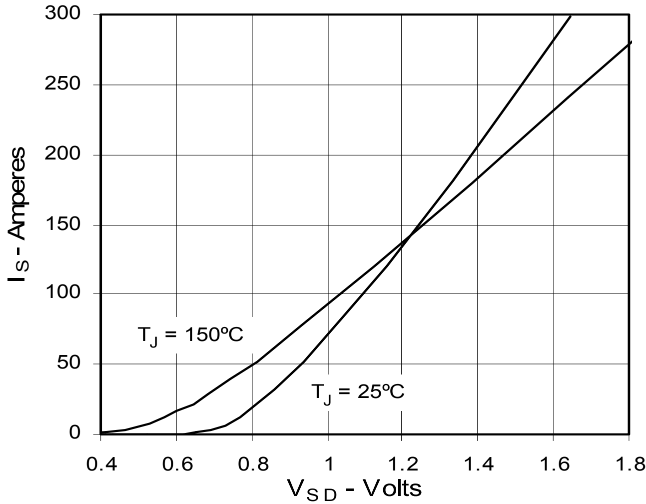

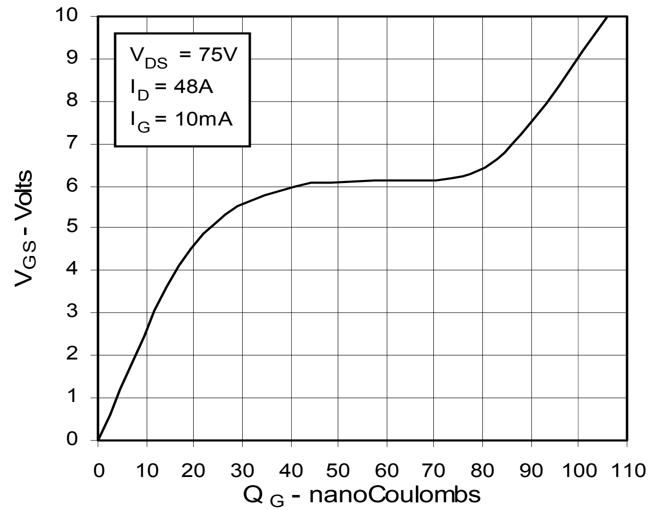

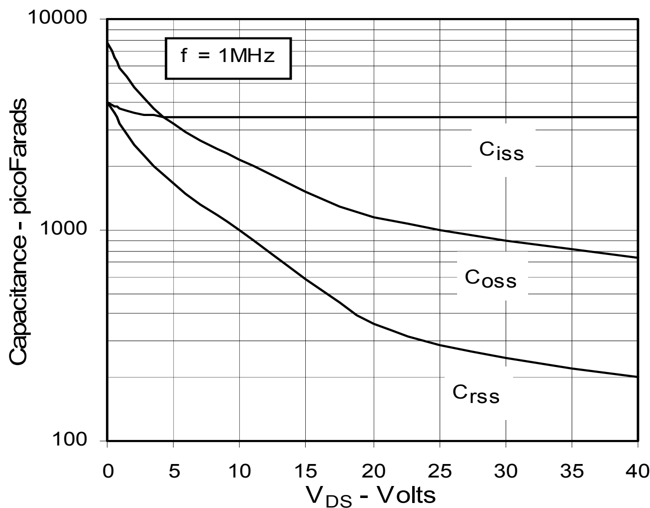

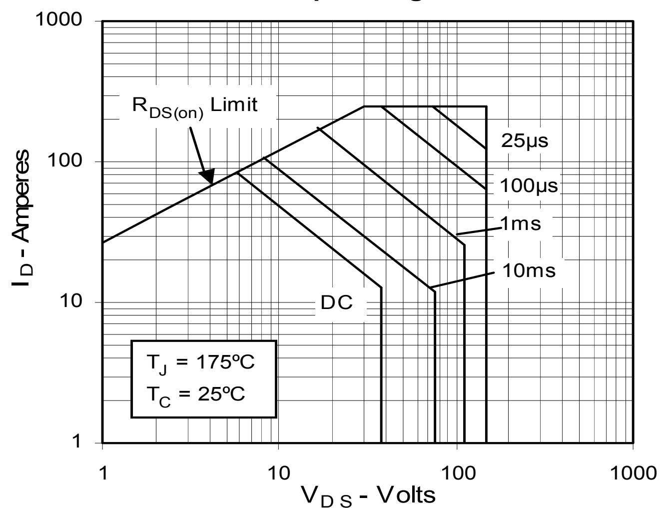

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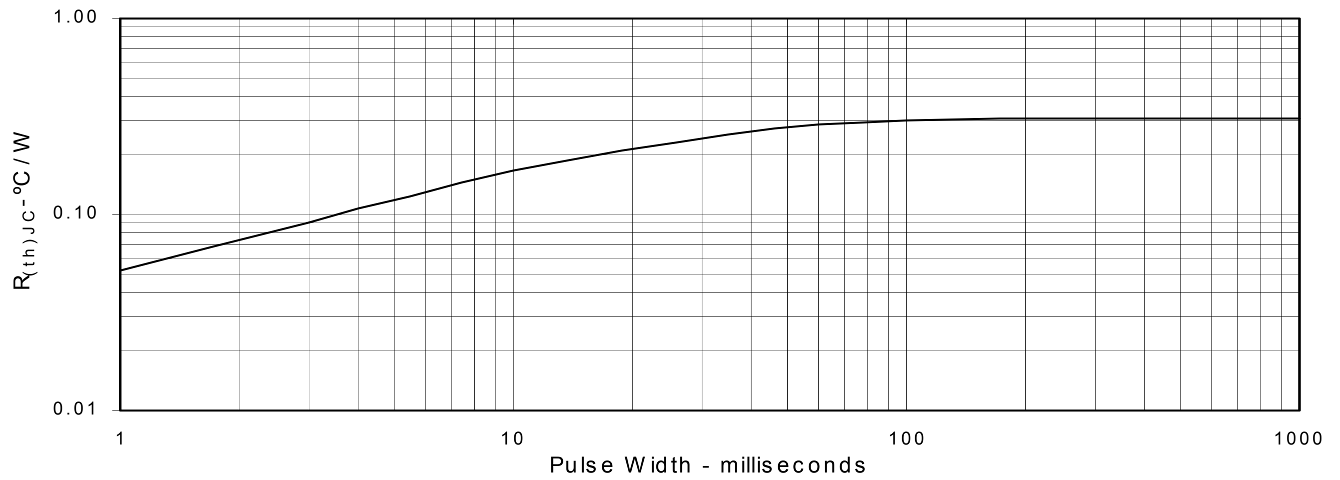

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Forward-Biased, Reverse-Biased, and Short-Circuit Safe Operating Area of MOSFETs and IGBTs

Objectives

This document explains the operating conditions that a power semiconductor is supposed to work in without being damaged. Focus is set on the *Forward-Biased Safe Operating Area* (FBSOA), the *Reverse Biased, Safe Operating Area* (RBSOA) and the *Short-Circuit Safe Operating Area* (SCSOA).

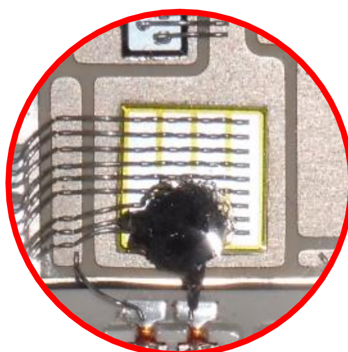

Figure 1. To be prevented – an IGBT destroyed by RBSOA-exceedance

Applications

The information compiled in this document is relevant for the power semiconductor itself and thus for all its applications.

Target Audience

This document is intended for all developers, design- and test-engineers involved in building power semiconductor applications.

Contact Information

For more information on the topic of safely operating power devices, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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Introduction

Power semiconductors like IGBTs, GTOs, thyristors, diodes, or bipolar junction transistors (BJT) have been developed into robust and reliable devices which can by now handle power levels into the MW-range and even beyond.

Despite these developments, they all have physical limitations which need to be known and respected to prevent damage to these components and the system they are mounted in. Depending on the instantaneous mode of operation, different conditions are described by a varying set of parameters, often referred to as operating area.

1. Safe Operating Area (SOA), also called Forward-Bias Safe Operating Area (FBSOA)

When a power semiconductor like an IGBT is used to conduct current in the predestined direction, the physical limits of the device to be considered include:

- the maximum collector current I_C,
- the saturation voltage V_{CEsat} across the device,
- the power generated by the product $I_C \cdot V_{CEsat}$, and
- the maximum junction temperature T_{VJ} allowed.

In cases where the power semiconductor is a MOSFET, dedicated to be operated in linear mode, the current can be influenced by tuning the gate-source-voltage accordingly. As a consequence, the drain-source-voltage V_{DS} of the devices changes which in turn impacts the losses. The device must dissipate these losses and the thermal impedance of the device poses the limits here.

For these operating conditions, the FBSOA-diagram features the forward voltage, the current and limits imposed by thermal development. Looking at Figure 2, it becomes obvious that growing losses can only be tolerated for shorter periods of time.

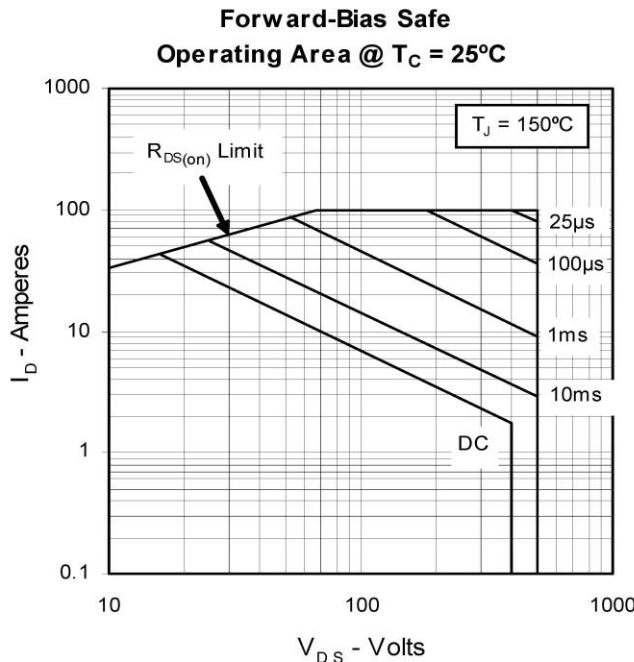

Figure 2. SOA Diagram for the IXTX46N50L

Any combination of forward voltage and current that is found below the correlating lines within the diagram is a legal point of operation as long as the junction temperature remains below the maximum limit and the duration of the loading is properly chosen. De-rating must be considered if the case temperature is different from the 25°C the diagram in Figure 2 refers to.

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2. Reverse Biased Safe Operating Area (RBSOA)

Power semiconductors like IGBTs or MOSFETs can turn off a current rather quickly but not at infinite speed. As the switching procedure does take some time, transient phenomena happen that need to be considered.

During this short period, when the device turns from conducting into blocking mode, the Reverse Biased Safe Operating Area needs to be respected at any time.

The limits are given by the current which is turned off and the voltage that appears across the device. The plot in Figure 3 schematically displays a turn-off event in detail.

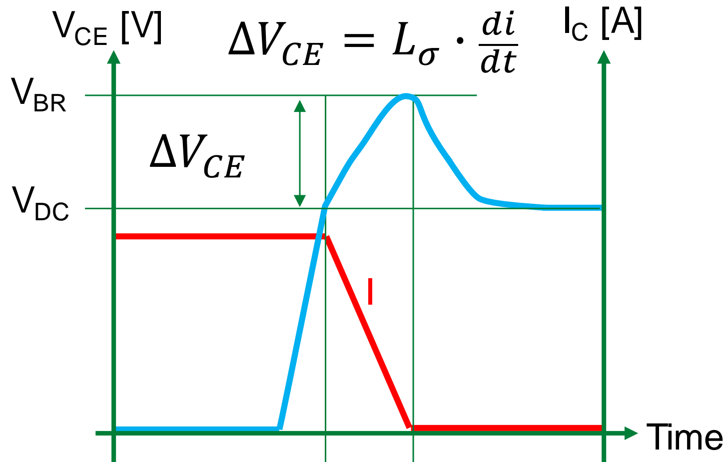

Figure 3. Voltage and current waveforms during a turn-off event

In the graph, it can clearly be seen that the voltage across the device first reaches the DC-link's voltage level before the current starts declining. Because of the current change rate di/dt and the inherently contained stray inductances L_σ, the voltage spike ΔV_{CE} is added on top of the DC-link voltage. If this spike exceeds the device's breakdown voltage V_{BR} – even for a very short period of time – the device will be destroyed.

The square-shaped Reverse Biased Safe Operating Area therefore is given by maximum current $I_{C,max}$ and the breakdown voltage V_{BR}, as depicted in Figure 4. Here too, the junction temperature poses a further limit.

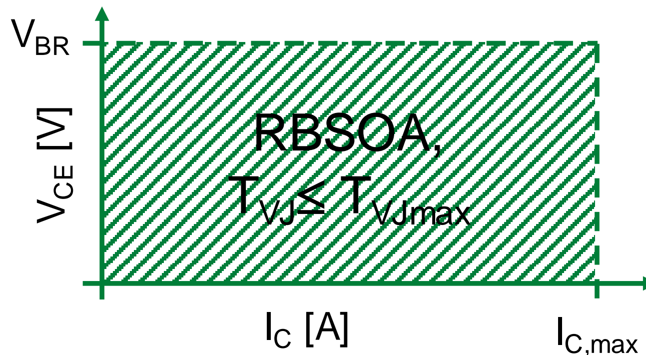

Figure 4. RBSOA-shape, limited by maximum current and breakdown voltage

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3. Short-Circuit Safe Operating Area (SCSOA)

Devices that feature desaturation, like most IGBTs, can withstand short-circuit events for a distinct duration. Corresponding datasheets highlight this information as Short Circuit Safe Operating Area or SCSOA. Such a datasheet's excerpt is given in Figure 5.

SCSOA	*short circuit safe operating area*	V_{CEK} = 1200 V					
t_{SC}	*short circuit duration*	V_{CE} = 720 V; V_{GE} = ±15	T_{VJ} = 125°C			10	µs
I_{SC}	*short circuit current*	R_G = 6.8 Ω; non-repetitive			450		A

Figure 5. SCSOA information taken from the MDMA280UB1600PTED datasheet

The short circuit condition demands that the IGBT goes into desaturation. In this mode, no further charge carriers remain available which also limits the current. Typically, IGBTs limit the short-circuit current to about three to four times their rated current. In the example in Figure 5, the 160 A-device is expected to limit the short circuit current to 450 A. This situation is tolerable for 10 µs only and limited by thermal development.

4. Resulting challenges for the designer

Combining the two areas for Reverse Biased Safe Operation and Short Circuit Safe Operation into a single diagram reveals a gap between them, as pictured in Figure 6.

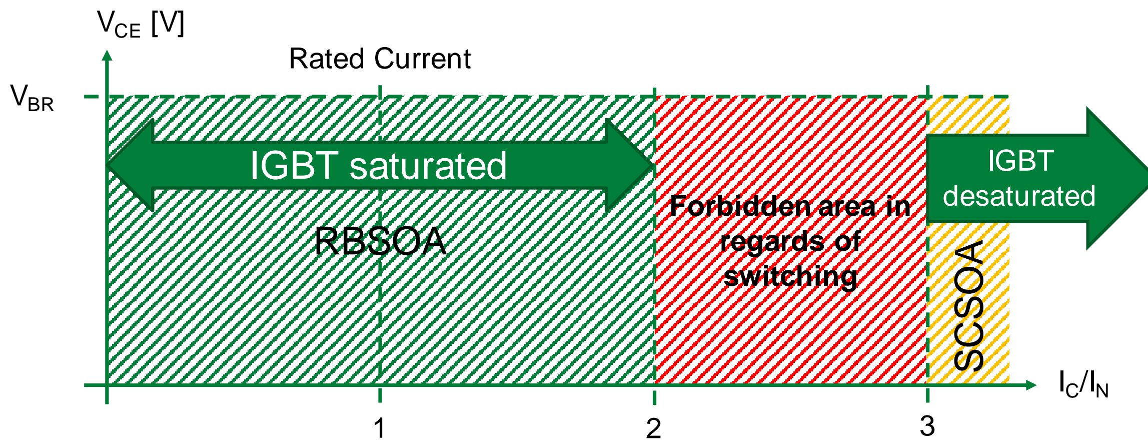

Figure 6. RBSOA, SCSOA, and the undefined region in between

Within the gap marked as forbidden area, located between twice and three times rated current, turning off the device is not allowed as it may lead to its destruction. The root cause of the destruction is found in very high local current densities, transiently forming during switching. The thermal limits in that case are reached already and additional burden due to switching losses leads to exceeding the limits. In turn, single cells on the chip fail and create a connection between collector and emitter. The current can no longer be turned off and the damage grows.

To overcome this situation, techniques to ensure that the IGBT reaches desaturation mode and enters the SCSOA can be used. The simplest way is to wait, instead of reacting on an overcurrent too quickly. Implementing a certain dead-time and fully exploit the 10 µs that the IGBT can withstand the conditions is a valid approach.

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Further methods include the so-called 2-Level turn-off. The device is not turned off by immediately cancelling or even reversing the gate-emitter voltage. Instead, the gate-emitter voltage is first reduced to minimize the number of charge carriers available for current transport. This speeds up reaching the desaturation stage. A few microseconds later, when desaturation is reached, the gate-emitter voltage is set to zero or reversed. The device is then safely turned off within the SCSOA-specification.

This fact becomes particularly important when handling overcurrent situations.

From a given setup, measurements from a destructive turn-off event seen in Figure 7 were analyzed:

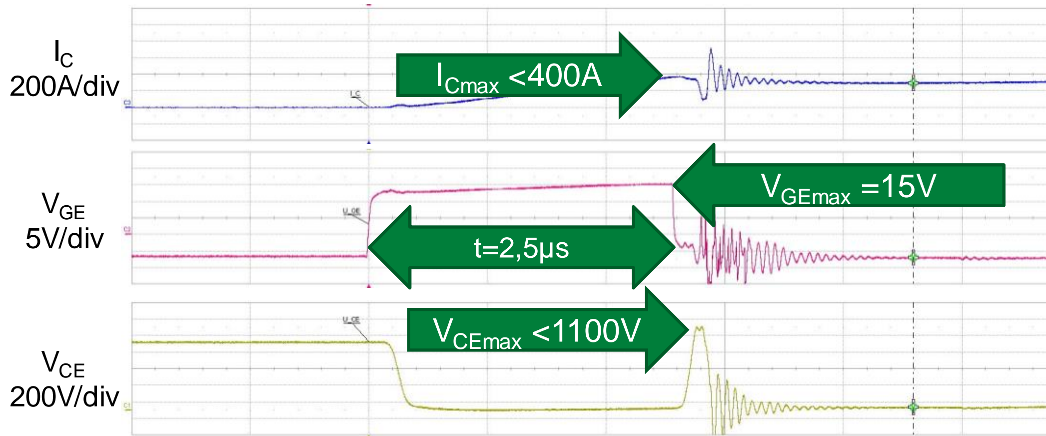

Figure 7. Measurement results from a destructive turn-off event

As the measurement reveals, the current turned off was well below the 450 A short-circuit limit. The gate-emitter-voltage was well-controlled, the time it took to turn off was below the 10 µs-limit and the overvoltage spike did not exceed the 1200 V the device is rated for. Still, the IGBT was destroyed, and the question raised, why so?

Entering the point of the turn-off into the diagram in Figure 6, the violation that happens becomes obvious in Figure 8:

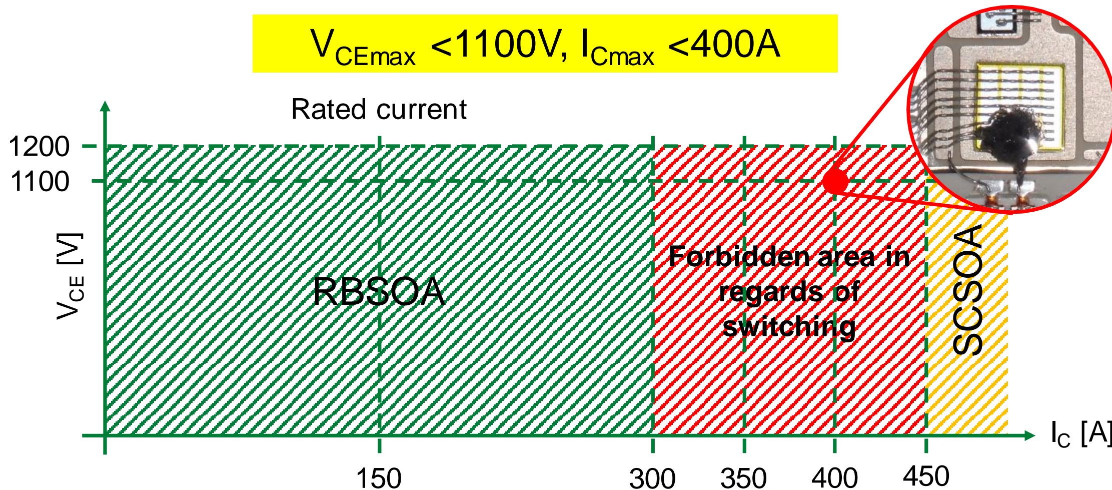

Figure 8. Locating the point of turn-off

Clearly, the switching event was done within the no-go-area with the destructive effect previously predicted.

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To clear the situation, the control strategy for short circuit was changed. Instead of reacting on the overcurrent signal instantly and turn off after just 2.5 µs, a blanking time of about 6 µs was added.

Figure 9 represents the measurement done in the same setup.

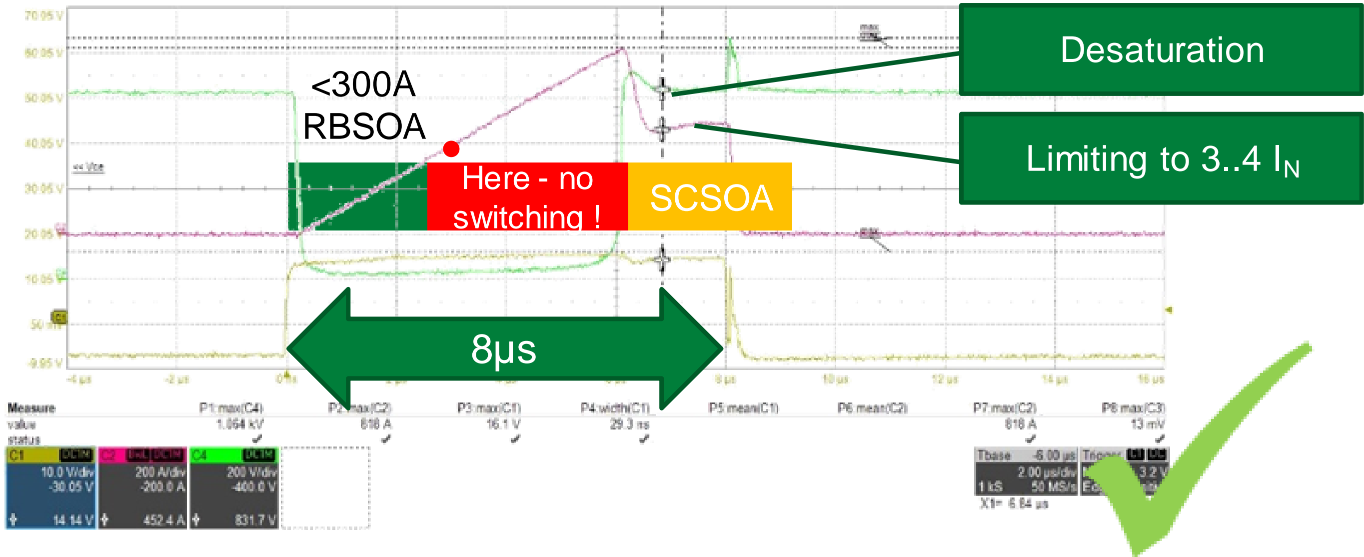

Figure 9. Properly turned off overcurrent or short-circuit event

While the red dot marks the former turn-off point, the current is now allowed to grow further. At first sight, this seems to worsen the situation as the losses and, as such, the chip temperature grows. However, after about 6 µs the IGBT reaches desaturation, enters the SCSOA and the turn-off after 8 µs is safely done without damaging the component.

MOSFETs, other than IGBTs, don't feature a dedicated SCSOA. At high currents, the MOSFET goes into linear operation as depicted in the FBSOA-diagram, so short-circuit and overcurrent events are covered by diagrams as given in Figure 2.

5. Conclusion

Handling overcurrent events, especially short circuit events, is challenging but manageable. Doing so while remaining within the given specifications can successfully be achieved.

Simply turning off a detected overcurrent as fast as possible may not be the best strategy as it may lead to damage caused by so-called RBSOA-exceedance. Ensuring that the IGBT reaches desaturation is a key factor in handling short circuit events with this technology.

For additional information please visit www.Littelfuse.com/powersemi

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Littelfuse Discrete Power MOSFET Datasheet Explanation

Objectives

The primary objective of this application note is to enhance the comprehension and analysis of power MOSFET datasheet parameters and graphs. By breaking down the technical specification into digestible insights, designers can gain deeper insights into the functionality and performance characteristics of MOSFETs. This application note provides a general recommendation about how to read and understand a datasheet with all its parameters and diagrams. The information presented plays a pivotal role in determining the operational limits and thresholds of the device.

Applications

This application note is applicable to all scenarios where power MOSFETs are utilized.

Target Audience

This document is intended for designers and developers who are utilizing Power MOSFETs within their respective applications.

Contact Information

For more information, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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1. Introduction

In the realm of modern electronics and power systems, an extensive understanding of semiconductor components, particularly the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), is crucial for achieving optimal system-performance and -efficiency. MOSFETs play a pivotal role in switching applications, offering versatile solutions. This document serves as a guide, delving into the detailed parameters presented in MOSFET datasheets. It aims to empower engineers and designers to make informed decisions and effectively leverage MOSFET capabilities in diverse applications.

Littelfuse furnishes datasheets with parameters that are essential and useful for selecting the appropriate device as well as for predicting its performance in specific application. This facilitates designers in comparing products from various suppliers and gaining valuable insights into the operational constraints of the device.

The outlined values in the datasheet describe the device's behavior under varying virtual junction temperature and testing conditions. Additionally, the dynamic characterization tests undergo execution utilizing precise configurations aimed at precise measurement of switching losses. As a result, discrepancies in these metrics manifest between the intended user applications.

The graphs included in the datasheet represent typical performance characteristics and can be used to extrapolate from one set of operating conditions to another. This application note explains parameters based on the IXTH120N20X4 datasheet which is an N-channel enhancement mode, power MOSFET. All the parameters mentioned in a Littelfuse datasheet are measured according to *IEC 60747-8* standards.

2. Essential Datasheet Insight

This section serves as an overview of important information found on the first page of the datasheet, including the datasheet status.

2.1. Key Information

The first page of the datasheet includes details such as the part number, pinout diagram, features and benefits, applications, and key attributes of the product.

- **Part Number** indicates the manufacturer, MOSFET type, package type, current rating, channel type, voltage class, technology series and a suffix for some special packages that gives extra information such as high voltage package, over molded package, and w/ 4 leads. Designation of MOSFET part number is drafted in **Figure 1**. The detailed information about this can be found as part number nomenclature - discrete Si MOSFET on Littelfuse website.

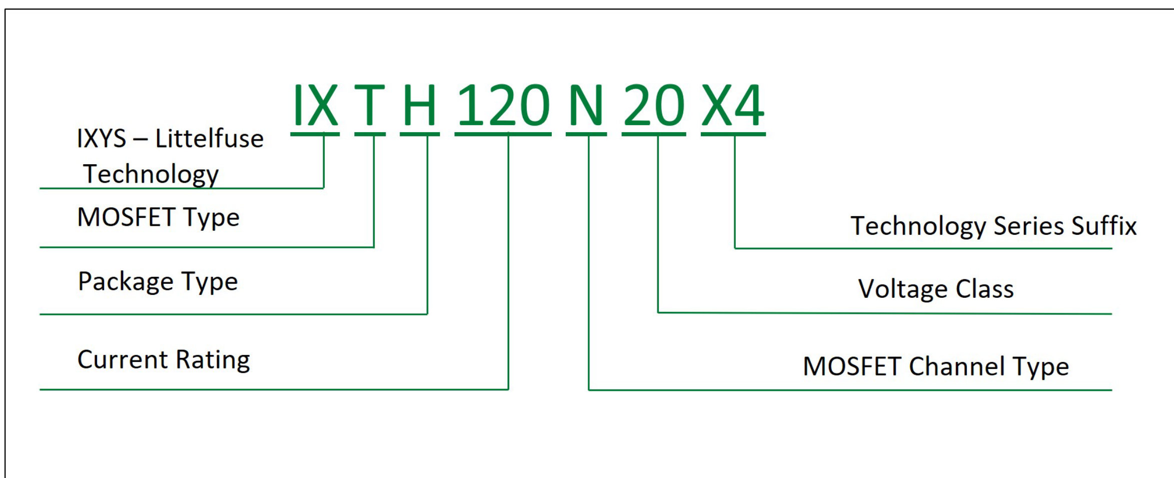

Figure 1. Part Number Designation

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- **Pinout Diagram** provides a visual representation of the device's physical layout including circuit symbol as highlighted in **Figure 2**.

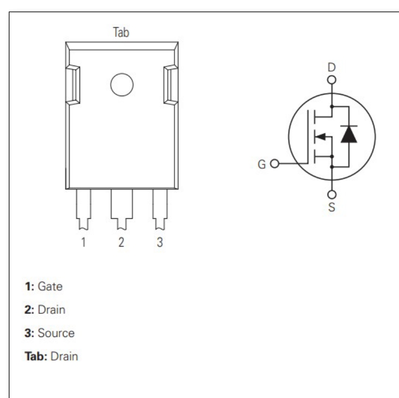

Figure 2. Pinout Diagram of TO-247 and Circuit Symbol of an N-channel Enhancement Mode MOSFET

- **Features and Benefits** encompasses a comprehensive list of features and their corresponding benefits offered by the MOSFET device, which helps user acquire a better understanding of how the MOSFET can meet their specific application requirements to deliver optimal performance and reliability.
- **Key Attributes / Product summary** highlights the key specifications and performance characteristics of the MOSFET, including parameters such as maximum drain-source voltage (V_{DSS}), maximum drain current (I_D) at 25°C, and on-state resistance ($R_{DS(on)}$) as pointed out in **Table 1**.

Table 1. Key Attributes/Product Summary

Characteristic	Value	Unit
V_{DS}	200	V
I_D @ 25 °C	120	A
$R_{DS(on)}$	≤ 9.5	mΩ

2.2. Datasheet Status

There are three distinct types of datasheets, each corresponding to a different stage of the product development or documentation process, depending on the degree of completeness, correctness, or approval.

- **Target datasheet:** During product development, the term *target datasheet* denotes a document laying out the desired product specifications, characteristics, and performance attributes. The development team uses this document to guide their efforts.
- **Preliminary datasheet:** Created before reaching its final, approved format. It is an early or preliminary representation of a product's specifications, features, and characteristics. The difference between a preliminary datasheet and a final datasheet is that certain data values are still missing. The missing values in the preliminary data sheet are noted as to be defined (TBD). These datasheets are made using the engineering samples that are in early phase of development.
- **Final datasheet:** Detailed and authoritative document that contains all the values that were missing in the preliminary datasheet. The parameters specified in the final datasheet are explained in this document. Any major change with respect to a MOSFET's characteristics in the final datasheet is associated with a Product Change Notification (PCN).

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3. MOSFET Datasheet Parameters

This section serves as a thorough exploration of the various parameters detailed within a MOSFET's datasheet. It describes the MOSFET's performance and characteristics, from maximum ratings to static and dynamic parameters, thermal properties, and package-related factors.

3.1. Maximum Ratings

The maximum ratings at which the MOSFET can be operated are listed on the second page of the datasheet in a table that summarizes the electrical and thermal limits of the device. The maximum ratings provided in the data sheets are absolute in nature. If any of the maximum ratings are surpassed, it is to be expected that the semiconductor experiences fatal failure, regardless of whether the remaining maximum ratings are utilized to their full extent. Unless otherwise noted, the values are applicable at a virtual junction temperature (T_{vj}) of 25°C. **Table 2** lists the maximum ratings designated for the IXTH120N20X4.

Table 2. IXTH120N20X4 MOSFET Maximum Ratings

Symbol	Characteristic	Conditions		Value	Unit
V_{DSS}	Drain-source voltage	25 °C ≤ T_{vj} ≤ $T_{vj(max)}$		200	V
V_{GSS}	Gate-source voltage	–		± 20	V
V_{GSM}	Transient gate-source voltage	$t_{transient}$ = 1 ms		± 30	V
I_D	Drain current	–	T_c = 25 °C	120	A
			T_c = 100 °C	89	A
I_{DM}	Peak drain current	T_c = 25 °C, Pulse width limited by $T_{vj(max)}$		240	A
I_S	Diode forward current	V_{GS} = 0 V		120	A
I_{SM}	Diode peak forward current	Pulse width limited by $T_{vj(max)}$		480	A
I_{AS}	Non-repetitive single pulse avalanche current	–		60	A
E_{AS}	Non-repetitive single pulse avalanche energy	–		1	J
dv/dt	Diode dv/dt capability	V_{DS} = 0...... 200 V, I_S ≤ 120 A		20	V/ns
P_{tot}	Total power dissipation	T_c = 25 °C		417	W
T_{vj}	Virtual junction temperature range	–		−55 to +175	°C
$T_{vj(max)}$	Maximum virtual junction temperature	–		175	°C
T_{stg}	Storage temperature range	–		−55 to +175	°C
T_{sld}	Soldering temperature	1.6 mm (0.062 in.) from case 10 s		300	°C
M_s	Mounting torque for screws to heat sink	–		1.3/10	Nm/lb.in

Drain-source voltage (V_{DSS}) is the crucial parameter in datasheets, representing the maximum voltage that can be applied across drain and source while the gate and source are being connected or V_{GS} = 0 V. It sets the limit to prevent breakdown and maintain operational functionality.

Gate-source voltage (V_{GSS}) and **Transient gate-source voltage (V_{GSM})** are visually delineated in **Figure 3**, offering a clear understanding of their roles in MOSFET operation. The gate-source voltage (V_{GSS}) denotes the maximum steady-state voltage that can be applied across gate and source without the gate oxide being damaged. Conversely, transient gate-source voltage (V_{GSM}) refers to the peak voltage that the gate terminal of the MOSFET can endure within a specified transient period ($t_{transient}$) or temporary change in voltage.

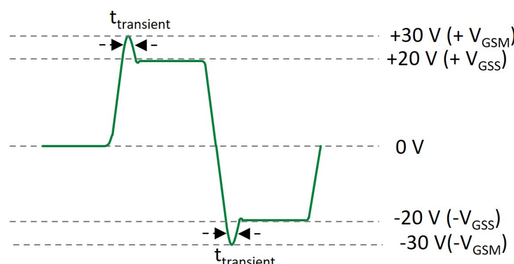

Figure 3. Gate-Source Voltage Definition

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Drain current (I_D) acts as a pivotal metric, outlining the maximum continuous current through the drain at a given case temperature T_c, of 25°C. Its calculation is based on several factors, including the maximum power dissipation P_{tot}, the temperature difference junction to case, the thermal resistance junction to case $R_{th(j\text{-}c)}$, and the maximum on-resistance $R_{DS(on)}$. Additionally, the temperature dependence of the on-state resistance is considered, as detailed in **Equation 1** and **Equation 2**. The drain current can be limited by the current handling capacity of leads or terminals.

$$P_{tot} = \frac{T_{vj(max)} - T_c}{R_{th(j-c)}} = I_D{}^2 \cdot R_{DS(on)}|_{T_{vj}=T_{vj(\max)}} \quad (1)$$

Solving for I_D as

$$I_D = \sqrt{\frac{T_{vj} - T_c}{R_{th(j-c)} \cdot R_{DS(on)}\,|_{T_{vj}=T_{vj(\max)}}}} \quad (2)$$

Peak drain current (I_{DM}) signifies the peak current that the device can handle above the I_D specification under the maximum virtual junction temperature. It varies with the current pulse width and heat dissipation conditions. **Figure 4** demonstrates the forward-bias safe operating area (FBSOA) of a MOSFET, which indicates the maximum pulse width at which the device can handle specific current without experiencing failure.

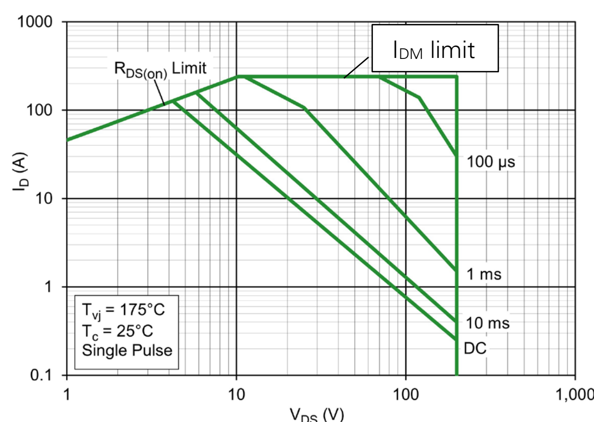

Figure 4. Forward-Bias Safe Operating Curve

Diode forward current (I_S) relates to the maximum DC forward current the body diode can handle in the forward direction at particular case temperature, which is typically equivalent to the MOSFET's continuous drain current I_D.

Diode peak current (I_{SM}) is an indicative of the peak current the diode can handle above diode forward current specification under maximum virtual junction temperature, which is typically equivalent or higher than the MOSFET's peak drain current I_{DM}.

Diode dv/dt capability corresponds to the maximum allowable rate of change of voltage across the body diode during the reverse recovery period without causing undesired effects. The power MOSFET structure contains a parasitic bipolar junction transistor (BJT), which could be activated by an excessive rise rate of the drain-source voltage (dv/dt), particularly after the recovery of the body diode.

Total power dissipation (P_{tot}), as expressed in Equation 1 , encompasses the maximum calculated power that the device can dissipate, serving as a function influenced by both maximum virtual junction temperature $T_{vj(max)}$, and the thermal resistance junction to case $R_{th(j\text{-}c)}$ at a case temperature of 25°C.

Virtual junction temperature (T_{vj}) range is –55 to 150°C or –55 to 175°C in most cases and it is the permissible temperature range in which the MOSFET may be operated continuously. The maximum virtual junction temperature $T_{vj(max)}$ is 150°C or 175°C depending on the technology. The negative temperature limit for Littelfuse discrete MOSFETs is typically –55 °C. The virtual junction temperature influences the electrical parameters of a MOSFET. For instance, at very high temperatures, the device's threshold voltage is reduced, and the leakage current increases, which leads to thermal runaway within the device.

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Storage temperature (T_{stg}) range points to the range of temperatures where the device can be safely stored or transported without adversely affecting its performance or reliability. The range is usually between –55°C to 150°C.

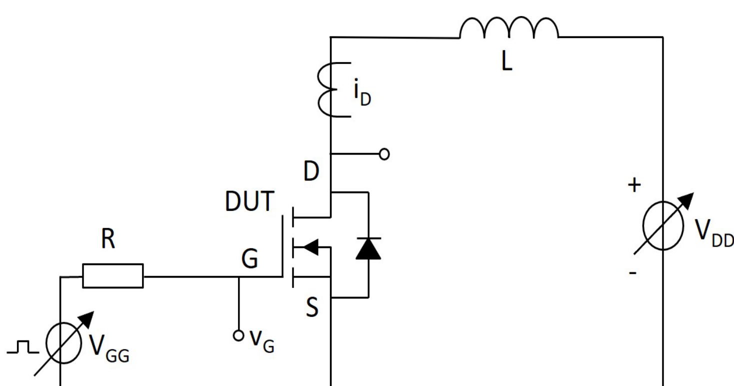
Soldering temperature (T_{sld}) enumerated in the datasheet implies the temperature at which the device can be safely soldered to the Printed Circuit Board (PCB) during the assembly process. The maximum soldering temperature is typically 300°C for devices with leads and 260°C for Surface Mount Devices (SMD).

Mounting torque (M_s) for screws to heatsink is the recommended maximum torque that can be applied during the process of mounting the MOSFET to a heatsink or a PCB. **Mounting torque (M_t)** for screws to terminals is the suggested torque that shall be applied to screwed terminals.

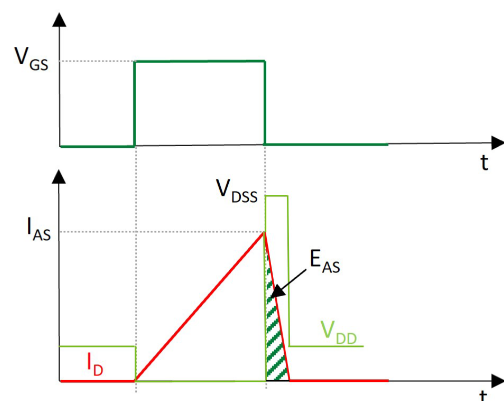
Mounting force (F) is the maximum force for pressure mounted devices, fixed by clips, that shall be applied to the isolated devices.

Non-repetitive single pulse avalanche current (I_{AS}) and Non-repetitive single pulse avalanche energy (E_{AS}) are specified only for avalanche-rated devices. I_{AS} denotes the maximum current that the MOSFET can endure during a single avalanche event without sustaining damage. Whereas E_{AS} quantifies the total energy absorbed by the device during such an event, indicating its ability to withstand high-energy transient events without permanent damage.

In **Figure 5 (a)**, the Unclamped Inductive Switching (UIS) test circuit, used to test the avalanche capability of a power MOSFET is depicted. In **Figure 5 (b)**, the waveforms during avalanche breakdown are presented. A gate pulse turns-on the MOSFET and allows the current (I_D) to ramp up according to the inductor's value (L) and the drain supply voltage (V_{DD}). At the end of gate pulse, the MOSFET turns-off causing the voltage across the MOSFET to rise sharply. The over voltage is clamped at the breakdown voltage (V_{DSS}) until the load current reaches zero and all the energy is dissipated. The green area shaded in **Figure 5 (b)** is the avalanche energy E_{AS}.



(a) Unclamped Inductive Switching



(b) Waveforms during Avalanche Breakdown

Figure 5. Typical Avalanche Test Circuit

Non-repetitive single pulse avalanche energy is calculated from the **Equation 3**:

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}{}^{2} \cdot \frac{V_{DSS}}{(V_{DSS} - V_{DD})} \tag{3}$$

where V_{DSS} is the drain-source avalanche voltage.

Note : When V_{DD} is set to a smaller value compared to V_{DSS}, then E_{AS} is calculated by using the approximation equation of $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2$

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3.2. Static Electrical Characteristics - MOSFET

Static electrical characteristics are the set of parameters and properties that describe the device behavior under steady-state condition. Most of the parameters included in the datasheet, along with their typical ranges of variance is listed in **Table 3**. In accordance with IEC 60747-8{ed3.1}, the characteristics of Power MOSFETs are provided at 25°C and, when necessary, at another higher operating temperature.

Table 3. MOSFET Static Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$V_{(BR)DSS}$	Breakdown voltage, drain-source	V_{GS} = 0 V, I_D = 250 µA		200	–	–	V
$V_{GS(th)}$	Gate-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA		2.5	–	4.5	V
I_{DSS}	Drain-source leakage current	V_{DS} = V_{DSS}, V_{GS} = 0 V	T_{vj} = 25 °C	–	–	25	µA
			T_{vj} ≤ 150 °C	–	–	500	
I_{GSS}	Gate leakage current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, I_D = 0.5 · I_D	T_{vj} = 25 °C	–	–	9.5	mΩ

Breakdown voltage, drain-source ($V_{(BR)DSS}$) corresponds to the minimal blocking voltage between drain and source, measured according to **Figure 6**, at a specified collector current while the gate and source are connected.

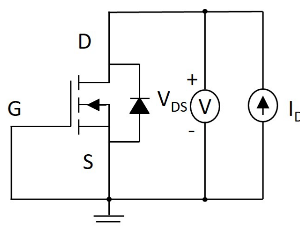

Figure 6. Circuit Diagram to Measure Breakdown Voltage

Gate-source threshold voltage ($V_{GS(th)}$) is the voltage measured across gate to source at which the drain current begins to flow, and the device is at on-state. It has a negative temperature coefficient. The circuit diagram illustrating the measurement of $V_{GS(th)}$ is depicted in **Figure 7**. Initially, the drain pin and the gate pin are short, after which drain current is applied while observing the gate-source voltage ($V_{GS(th)}$) reading.

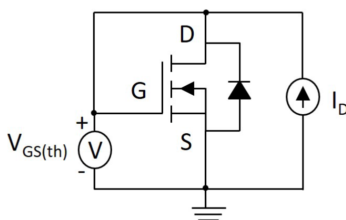

Figure 7. Circuit Diagram to Measure Gate-Source Threshold Voltage

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Drain-source leakage current (I_{DSS}) value indicates the drain current measured at a given drain-source voltage and with the gate to source connected, as illustrated in **Figure 8**. The datasheets specify the value at 25°C and higher virtual junction temperature.

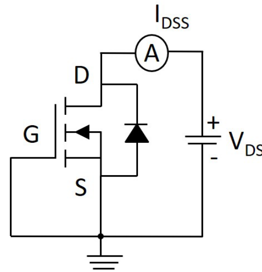

Figure 8. Circuit Diagram to Measure MOSFET's Leakage Current

Gate leakage current (I_{GSS}) refers to the small amount of current that flows between the gate and source when the MOSFET is in an off state. **Figure 9** demonstrates the circuit used to measure the gate leakage current. Initially, the drain-to-source terminal is connected, and then a maximum allowable voltage is applied across the gate and source terminals to monitor the leakage current.

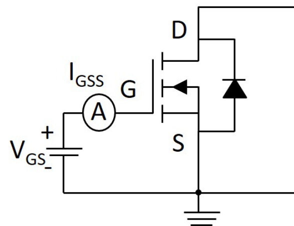

Figure 9. Circuit Diagram to Measure Gate Leakage Current

Drain-source on-state resistance ($R_{DS(on)}$) describes the resistance across the drain and source when the MOSFET is in the on-state. **Figure 10** presents the circuit diagram for measuring the drain-source on-state resistance ($R_{DS(on)}$). Initially, the gate-source voltage (V_{GS}) is set to a defined value, and then the voltage drop across the drain-source voltage $V_{DS(on)}$ is measured, using a given current source (I_D). $R_{DS(on)}$ is calculated using the **Equation 4**:

$$R_{DS(on)} = \frac{V_{DS(on)}}{I_D} \quad (4)$$

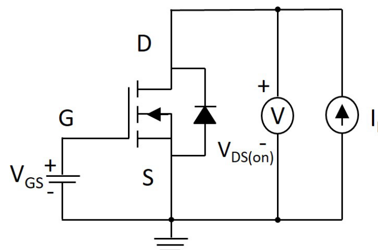

Figure 10. Circuit Diagram to Measure Gate Drain-Source On-State Resistance

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3.3. Dynamic Characteristics

This section of the datasheet provides information on the behavior of the device in dynamic conditions, as shown in **Table 4**. The intrinsic capacitances, gate charge and switching behavior of the MOSFET are pivotal factors influencing the dynamic performance of the device.

Table 4. Dynamic Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$R_{g(int)}$	Internal gate resistance	f = 1 MHz, open drain		–	6	–	Ω
C_{iss}	Input capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	6100	–	pF
C_{oss}	Output capacitance			–	865	–	
C_{rss}	Reverse transfer capacitance			–	1.8	–	
$C_{oss(er)\ eff.}$	Effective output capacitance, energy related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V		–	510	–	pF
$C_{oss(tr)\ eff.}$	Effective output capacitance, time related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V, I_D = constant		–	2000	–	pF
Q_G	Gate charge	V_{DD} = 0.5 · V_{DSS}, V_{GS} = 10 V, I_D = 0.5 · I_D		–	108	–	nC
Q_{GS}	Gate-source charge			–	27	–	
Q_{GD}	Gate-drain charge			–	27	–	
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 0.5 · I_D		72	120	–	S
$t_{d(on)}$	Turn-on delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	13	–	ns
t_r	Rise time		T_{vj} = 25 °C	–	24	–	
t_{on}	Turn-on time		T_{vj} = 25 °C	–	37	–	
$t_{d(off)}$	Turn-off delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	100	–	ns
t_f	Fall time		T_{vj} = 25 °C	–	12	–	
t_{off}	Turn-off time		T_{vj} = 25 °C	–	112	–	

Internal gate resistance ($R_{g(int)}$) signifies the resistance that exists within the device gate structure. The internal gate resistance mentioned in **Figure 11**, constitutes a component of the parasitic elements within the MOSFET. Together with the MOSFET's input capacitance, the gate resistance forms an RC network that determines the voltage change at the MOSFET gate and thus the switching time.

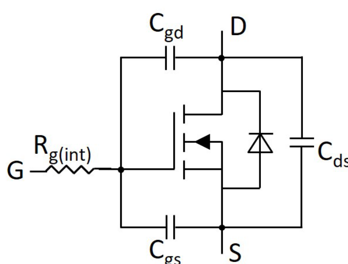

Figure 11. Power MOSFET Parasitic Components

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Capacitance Characteristics play a crucial role in switching characteristics of the MOSFET.

- **Input capacitance (C_{iss})** encompasses both gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs}, representing the total capacitance measured between the gate and source terminals with the drain connected to the source terminal.

$$C_{iss} = C_{gs} + C_{gd} \quad (5)$$

- **Output capacitances (C_{oss})** consists of the drain-to-source capacitance C_{ds} and gate to drain capacitance C_{gd}, indicating the output capacitance which is measured between the drain and source with the gate connected to the source terminal.

$$C_{oss} = C_{ds} + C_{gd} \quad (6)$$

- **Reverse transfer capacitance (C_{rss})** primarily arises from C_{gd}, delineating the capacitance between the gate and drain with the source terminal connected to ground.

$$C_{rss} = C_{gd} \quad (7)$$

Effective output capacitance of the MOSFET includes both energy related and time related parameters, denoted as $C_{oss(er)}$ and $C_{oss\,(tr)}$ respectively. $C_{oss(er)}$ represents a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to specified voltage. Conversely, $C_{oss(tr)}$ signifies a fixed capacitance that gives the same charging time as a C_{oss} while V_{DS} is rising from 0 V to specified voltage and at a constant drain current I_D.

Total gate charge (Q_G) is the total amount of charge that is required during the MOSFET's turn-on and turn-off transition. The switching speed depends on the speed at which a gate driver can charge or discharge the input gate charge. **Figure 12** presents a typical gate charge waveform for a power MOSFET in a resistive-load circuit. The fundamental equation for calculating the gate charge is formulated in **Equation 8**.

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t)dt \quad (8)$$

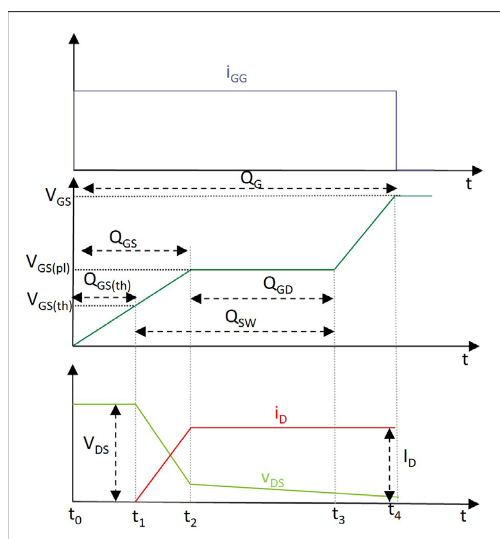

Figure 12. Gate Charge Waveform of Power MOSFET during Turn-on Transition with Resistive Load

As depicted in the gate charge waveform, the total gate charge encloses the **Gate-Source Charge (Q_{GS})**, the **Gate-Drain Charge (Q_{GD})**, and the **Gate Switch charge (Q_{SW})**. Q_{GS} represents the amount of charge that is required to charge the gate-source capacitance (C_{gs}) from its initial voltage to the miller plateau level. Q_{GD} quantifies the charge that is needed to fully charge the gate-drain capacitance (C_{gd}) during switching, ensuring full channel enhancement and sustaining the MOSFET in its conducting state. Lastly, Q_{SW} encapsulates charge stored in the gate capacitance from when the gate-source voltage has reached the gate-source threshold voltage, $V_{GS(th)}$ until the end of the miller plateau.

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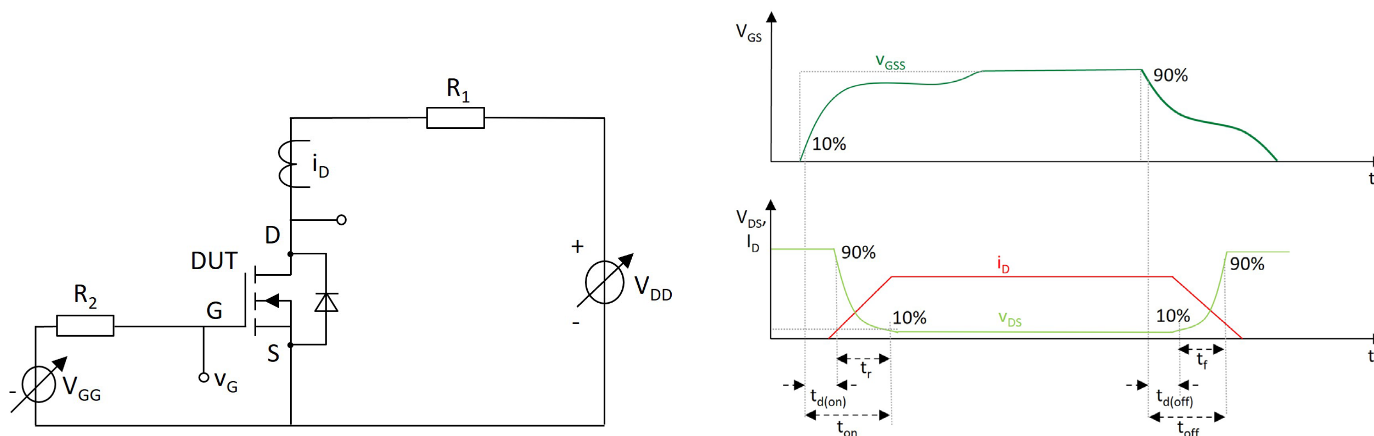
Transconductance (g_{fs}) is described as the change in drain current divided by the change in gate voltage for a constant drain voltage. A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. The transconductance is mathematically expressed as:

$$g_{fs} = \left. \frac{dI_D}{dV_{GS}} \right|_{V_{DS} = constant} \quad (9)$$

MOSFETs, due their physical structure, can change their state from on to off much faster than IGBTs. The correlations of switching time measurement circuit and the switching time definitions are demonstrated **Figure 13**.



(a) Switching Time Measurement Circuit Diagram

(b) Switching Time Definition Waveform

Figure 13. Correlation of Switching Time Measurement Circuit and Switching Time Definition

- **Turn-on delay time ($t_{d(on)}$)** is the time interval when the gate-source voltage (V_{GS}) has reached 10% of its end value, to the time when the drain-source voltage (V_{DS}) has dropped to 90% of its initial value or rated value.
- **Rise time (t_r)** specifies the time interval between the drain-source voltage dropping from 90% to 10% of its initial value. The drain current starts to rise, and a major part of turn-on losses is generated during this period.
- **Turn-off delay time ($t_{d(off)}$)** denotes the time interval between the moment when the gate-source voltage (V_{GS}) has declined to 90% of its initial value and the drain-source voltage has risen to 10% of the supply voltage.
- **Fall time (t_f)** implies the time interval between the drain-source voltage rise from 10% to 90% of its end value. During this period, the drain current starts to fall, and a major part of turn-off losses is generated during this time.

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3.4. Electrical Characteristics – Body Diode

Power MOSFET generally contain a body diode, which provides freewheeling operation in the inductive load switching. Hence, the MOSFET datasheet from Littelfuse also contains the electrical parameters and graphs related to the body diode. **Table 5** shows the electrical characteristics listed in IXTH120N20X4 datasheet.

Table 5. Electrical Characteristics – Body Diode

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{SD}	Diode forward voltage	V_{GS} = 0 V, I_S = 100 A [1]	–	–	1.4	V
t_{rr}	Diode reverse recovery time	V_{DD} = 100 V, I_S = 60 A, $-di_S/dt$ = 200 A/μs	–	190	–	ns
Q_{rr}	Reverse recovery charge		–	3.2	–	μC
I_{rrm}	Peak reverse recovery current		–	33.7	–	A

Note 1: Pulse test, t ≤ 300 μs, duty cycle, d ≤ 2%

Diode forward voltage (V_{SD}), measured under specified conditions including a given forward current (I_S), zero gate-source voltage (V_{GS}), and a virtual junction temperature of 25°C, symbolizes the maximum forward voltage drop across the intrinsic diode, as illustrated in **Figure 14**.

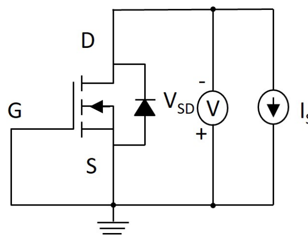
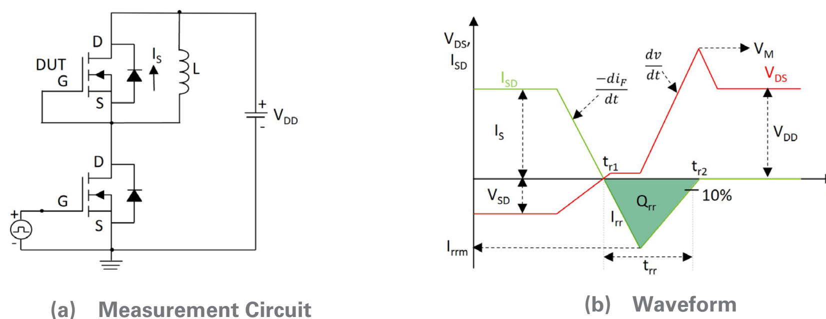


Figure 14. Circuit Diagram to Measure Diode Forward Voltage

Reverse recovery charge (Q_{rr}) characterizes the charge that is built up in the diode during the transition from the conducting or forward bias state to the non-conducting or reverse-biased state. The time that is necessary to remove the charge that persists within the diode during the reverse recovery phase is called **Diode Reverse Recovery Time (t_{rr})**. **Peak Reverse Recovery Current (I_{rrm})** denotes the maximum current flowing in the reverse direction during this period.

The circuit diagram and reverse recovery measurement waveforms are demonstrated in **Figure 15**. Mathematically, the reverse recovered charge, Q_{rr}, is defined as the integral of the reverse recovery current, I_{rr}, during the process of current commutation, with time as the variable. This relationship is expressed by **Equation 10**. The reverse recovery time, t_{rr}, is measured from the point of reverse bias initiation to the moment when the reverse current reaches 10% of its peak value.

$$Q_{rr} = \int_{t_{r1}}^{t_{r2}} I_{rr}(t)dt \quad (10)$$



(a) Measurement Circuit (b) Waveform

Figure 15. Diode Reverse Recovery

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3.5. Thermal Characteristics – Thermal Resistance (R_{th})

R_{th} signifies the thermal characteristics of the MOSFET at steady state, making it an essential parameter for thermal management of the MOSFET. **Table 6** outlines the R_{th} values presented in the datasheet. The heat generated within the silicon chip needs to be dissipated by means of heat sink into the ambient. The thermal dissipation pathway for a power MOSFET in a conventional and isolated discrete package with a heat sink is visually outlined in **Figure 16 (a) and (b)**.

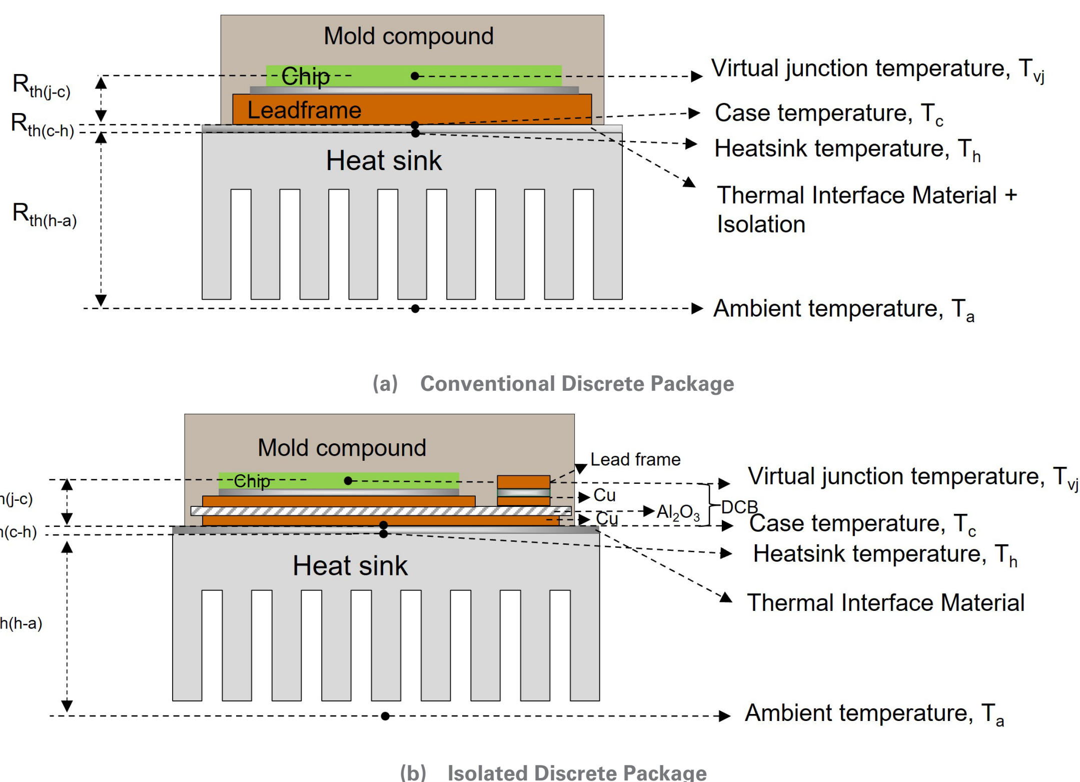
Table 6. Thermal Characteristics

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance junction to case – MOSFET	–	–	–	0.36	K/W
$R_{th(c-h)}$	Thermal resistance case to heat sink – MOSFET	–	–	0.21	–	K/W

Thermal resistance junction to case ($R_{th(j-c)}$) is the thermal resistance from the junction of the die to the outside of the device's case. It describes the passage of heat between the semiconductor chip and the case. Littelfuse specifies a maximum static $R_{th(j-c)}$ at T_{vj} = 125°C.

Thermal resistance case to heatsink ($R_{th(c-h)}$) characterizes the static heat dissipation of a MOSFET and depends on module size, heatsink, case surfaces, thickness parameters of thermal layers between module and heatsink.

Thermal resistance junction to ambient ($R_{th(j-a)}$) is equal to sum of junction to case, $R_{th(j-c)}$, case to heatsink $R_{th(c-h)}$ and heatsink to ambient thermal resistance, $R_{th(h-a)}$. The $R_{th(j-c)}$ is specified in the datasheet whereas $R_{th(c-h)}$ and $R_{th(c-a)}$ is determined by the user's board design and depends on the application.



(a) Conventional Discrete Package

(b) Isolated Discrete Package

Figure 16. Lateral Thermal Resistance Chain within a Semiconductor Package

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3.6. Package – Mechanical Rating

This part of the datasheet covers physical characteristics of the device.

Package weight (G) refers to the mass of the package or housing, including the MOSFET die and the required electrical and thermal connections.

Isolation voltage (V_{isol}) is specified only for isolated devices and represents the isolation voltage between all terminals connected against the cooling surface or base plate. The verification test circuit used to determine the isolation voltage rating between terminals and baseplate is visualized in **Figure 17**.

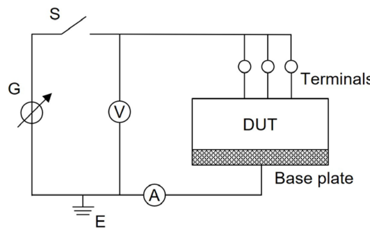

Figure 17. Circuit Diagram for Isolation Withstand Voltage Test

3.7. Characteristics Curves

The essential curve in the datasheet provides graphical portrayal of key performance characteristics of MOSFET devices. In this application note, the graphs, and parameters from the IXTH120N20X4 datasheet are used as reference.

Typical Output Characteristics of IXTH120N20X4, illustrating various modes of operation, are delineated in **Figure 18**. In the Cut-off region, the gate-source voltage (V_{GS}) is less than the gate-threshold voltage ($V_{GS(th)}$) and the device is an open circuit or off. In the *Ohmic region*, the device acts as a resistor with an almost constant on-resistance $R_{DS(on)}$ and which is equal to V_{DS} /I_D. In the linear-mode of operation, the device operates in the *Current-Saturated* region where the drain current (I_D) is a function of the gate-source voltage (V_{GS}) and defined by the **Equation 11**:

$$I_D = K \cdot \left(V_{GS} - V_{GS(th)}\right)^2 = g_{fs} \cdot \left(V_{GS} - V_{GS(th)}\right) \quad (11)$$

In this equation, K is a parameter depending on temperature and device geometry and g_{fs} is the current gain or transconductance. When the drain-source voltage (V_{DS}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. This reduction in surface potential continues as V_{DS} increases until it reaches a critical point, known as the *Channel Pinch-off Voltage*, where the drain voltage equals $\left(V_{GS} - V_{GS(th)}\right)$. At this point, the drain current becomes saturated.

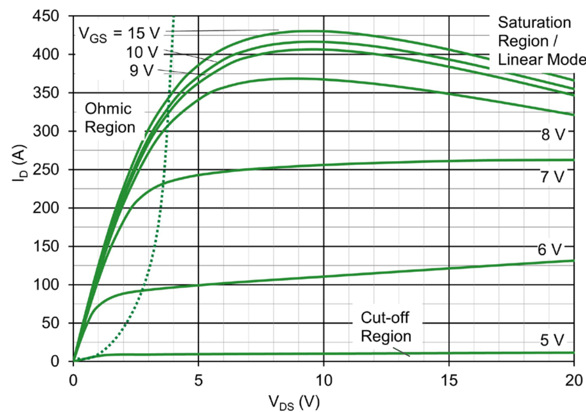

Figure 18. Typical Output Characteristics

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Typical Transfer Characteristics depicted in **Figure 19**, illustrates the relationship between drain current and gate voltage across varying temperatures of –40, 25, and 150°C. The intercepts of these lines at I_D = 0 A provides the threshold voltages for the respective temperature. It can be concluded that the transfer characteristic depends on both temperature and drain current and the threshold voltage decreases with increasing temperature.
In certain scenarios, a cross-over point or zero temperature coefficient point may be present. Below this point, the gate-source voltage exhibits a negative temperature coefficient, implying a decrease in gate-source voltage at higher temperatures for a given drain current. Conversely, above this point, the temperature coefficient for the gate-source voltage becomes positive.

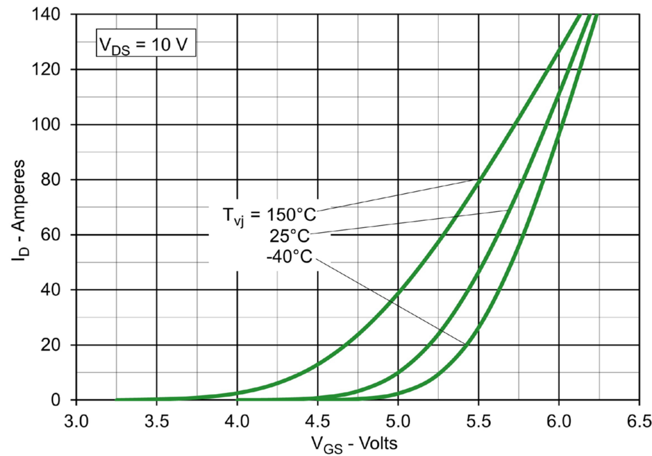

Figure 19. Typical Transfer Characteristics

Typical Drain-Source On-State Resistance (Normalized) vs. Virtual Junction Temperature - The value of $R_{DS(on)}$ is critical in power MOSFETS as it serves as an indicator of the device's capacity to handle current. An important characteristic is an increase in the on-resistance with increasing temperature, as evidenced in **Figure 20**, which portrays a positive temperature coefficient. The positive temperature coefficient of $R_{DS(on)}$ is a beneficial feature when paralleling power MOSFETs because it ensures thermal stability and balanced current sharing.

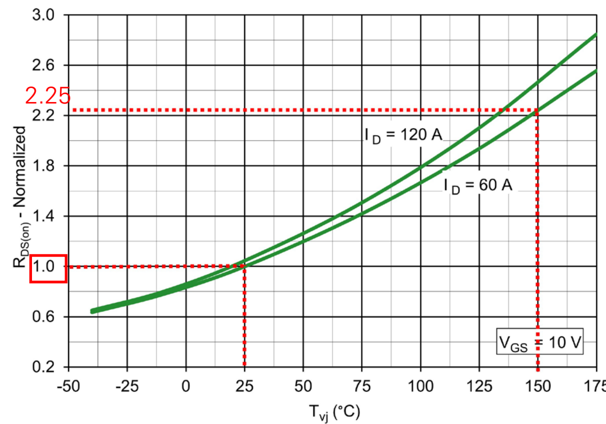

Figure 20. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Virtual junction temperature

From **Figure 20**, $R_{DS(on)}$ vs. T_{vj} (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at T_{vj} = 25°C, and it increases to 2.25 at T_{vj} = 150°C. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., $0.5 \cdot I_{D25}$) is specified as 9.5 mΩ at T_{vj} = 25°C, then it is predicted that it will change to 21.375 mΩ when Tvj = 150°C is applied. The normalized value is obtained from $R_{DS(on)}|T_{vj}$ / $R_{DS(on)}|T_{vj = }$ 25°C.

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Typical Drain-Source On-State Resistance (Normalized) vs. Drain Current presented in **Figure 21** provides information about the relative change in on-state resistance at different drain currents. The calculation of the on-state resistance, $R_{DS(on)}$ as a function of drain current I_D and gate-source voltage V_{GS} can be derived from the typical output characteristic diagram depicted in **Figure 18,** employing Ohm's Law.

$$R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D} \qquad (12)$$

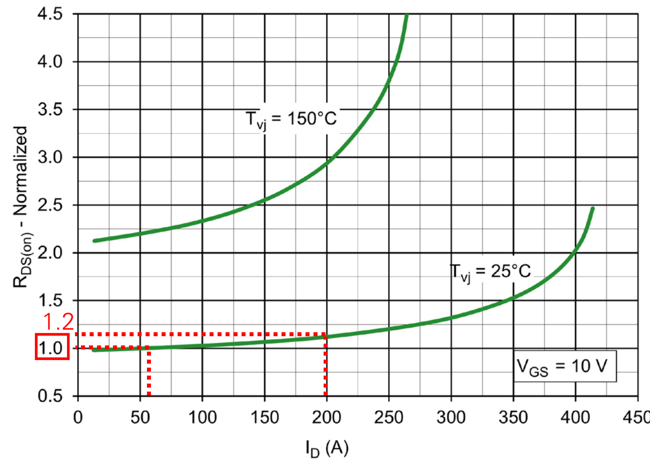

Figure 21. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Drain Current

From **Figure 21**, $R_{DS(on)}$ vs. I_D (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at I_D = 60 A, and it changes to 1.2 at I_D = 200 A. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., $0.5 \cdot I_{D25}$) is specified as 9.5 mΩ, then it is predicted that the resistance $R_{DS(on)}$ will change to 11.4 mΩ when I_D = 200 A is applied. The normalized value is obtained from $R_{DS(on)}|I_D$ / $R_{DS(on)}|I_D$ = 60 A.

Typical Breakdown Voltage and Gate Threshold Voltage (Normalized) vs. Virtual Junction Temperature - The relationship between $V_{(BR)DSS}$ / $V_{GS(th)}$ and T_{vj} is expressed in **Figure 22**. The breakdown-voltage $V_{(BR)DSS}$ features a positive temperature coefficient, whereas gate-source threshold voltage $V_{GS(th)}$ has a negative temperature coefficient. At 25°C, the normalized breakdown-voltage $V_{(BR)DSS}$ is 1, growing to value of 1.14 at 150°C. This signs that breakdown-voltage $V_{(BR)DSS}$ at T_{vj} = 25°C is 200 V and is expected to be 228 V at T_{vj} = 150°C. The value of gate-source threshold voltage $V_{GS(th)}$ is 1 at 25°C and 0.643 at 150°C, respectively. Assuming the device's gate-source threshold voltage $V_{GS(th)}$ is 3.5 V, then the $V_{GS(th)}$ remains at 3.5 V at T_{vj} = 25°C, but is anticipated to decrease to 2.24 V at T_{vj} = 150°C.

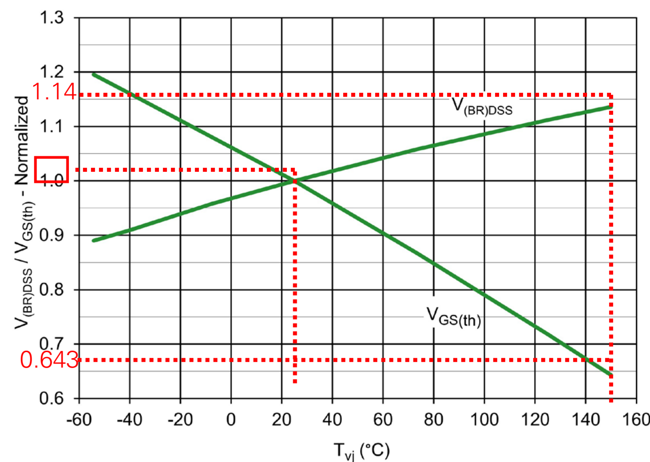

Figure 22. Typical $V_{(BR)DSS}$/$V_{GS(th)}$ (Normalized) vs. Virtual Junction Temperature

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Drain Current vs. Case temperature curve illustrated **Figure 23** depicts the solution of **Equation 2** across different case temperatures, demonstrating that at low case-temperature T_c, the maximum drain current I_D remains constant, while at high case-temperature T_c, it gradually decreases until reaching zero at $T_c = T_{vj(max)}$. However, the actual drain current is restricted by additional factors, including bond wire diameter, chip design, and assembly. It is noteworthy that, in certain instances, the continuous current is constrained by the package leads, although the switched current could potentially be higher.

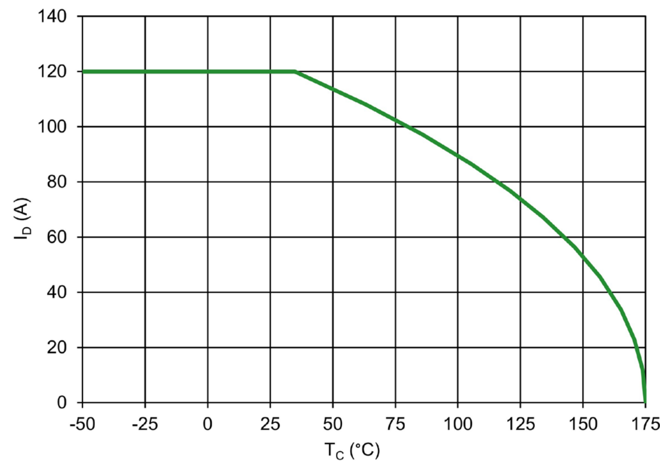

Figure 23. Drain Current vs. Case Temperature

Typical Transconductance - A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. **Figure 24** displays a typical variation of the transconductance with respect to drain current. The reduction in the mobility with increasing temperature adversely affects the transconductance.

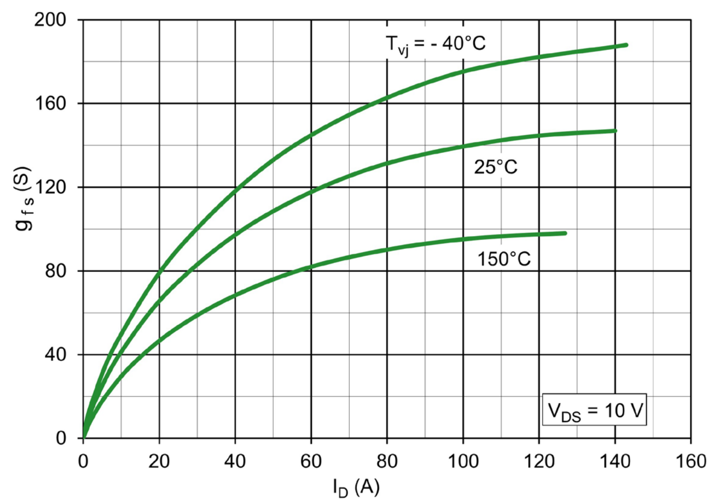

Figure 24. Typical Transconductance Curve

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Typical Gate Charge curve depicts the typical variation of the requisite gate charge to switch on the device at a specified V_{GS} and V_{DD}. A typical gate charge waveform for a power MOSFET can be observed in **Figure 25**. The gate charge reflects the charge stored on the inter-terminal capacitances and is used in designing the gate drive circuit.

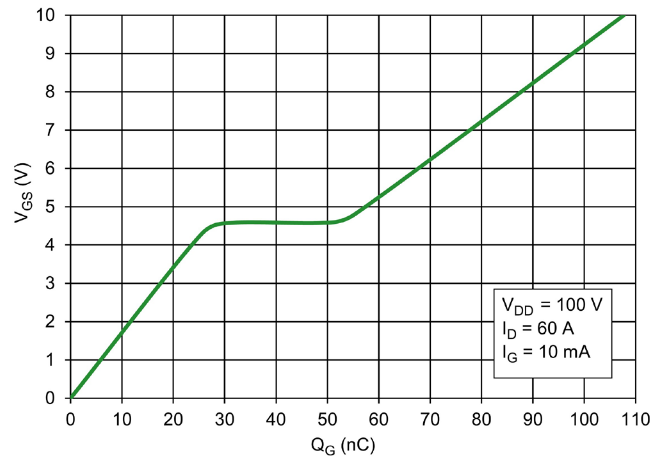

Figure 25. Typical Gate Charge Characteristics

In **Figure 26**, the parasitic **Junction Capacitances Characteristics** are represented as a function of drain-source voltage. Its components include input capacitance (C_{iss}), which consists of gate-source capacitance C_{GS} in parallel with drain-gate capacitance C_{DG}, output capacitance (C_{oss}), which consists of drain-gate capacitance C_{DG} in parallel with drain-source capacitance C_{DS} and reverse transfer capacitance (C_{rss}), which is the drain-gate capacitance C_{DG}.

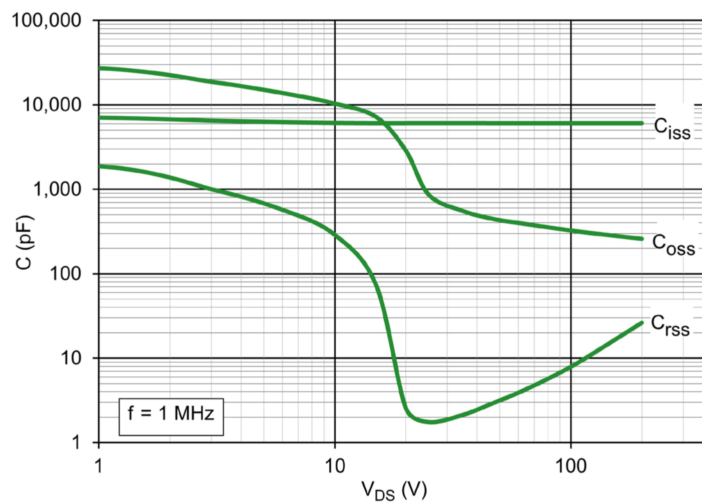

Figure 26. Typical Junction Capacitance

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Forward-Bias Safe Operating Area (FBSOA) is a datasheet figure of merit that defines the maximum allowed operating points. **Figure 27** shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bound by the maximum drain-to-source voltage V_{DSS}, maximum conduction current I_{DM}, maximum drain-source on-state resistance and constant power dissipation lines for various pulse durations.

In **Figure 27**, there is a series of curves that include a DC line along with four single pulse operating lines, 10 ms, 1 ms, and 100 µs. The top of each line is limited by the maximum drain current and is bounded by a positive sloped line defined by the on-state resistance $R_{DS(on)}$ of the device. The right-hand side of each line is terminated at the rated drain-source voltage limit V_{DSS}. Each line has a negative slope and is determined by the maximum power dissipation P_{tot} of the device:

$$P_{tot} = \frac{[T_{vj,max} - T_c]}{Z_{th(j-c)}} = V_{DS} \cdot I_D \quad (13)$$

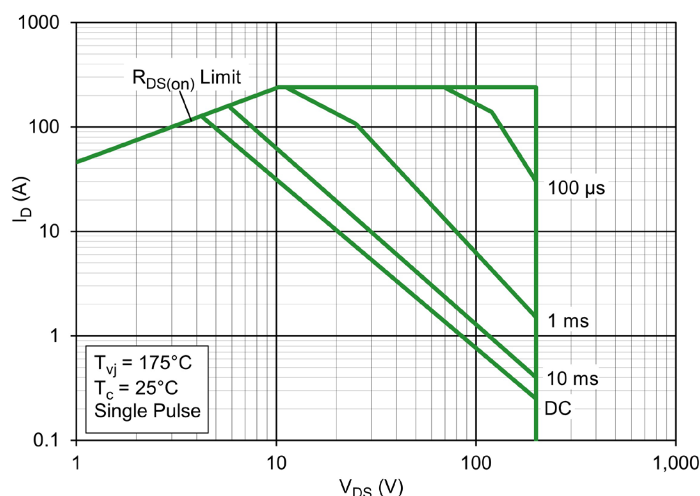

Figure 27. Forward Biased Safe Operating Area (FBSOA) Curve

These theoretical constant power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFET. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, as a result of lateral heat flow. Secondly, material imperfections like die attach voids and thermal grease cavities may cause local decrease of thermal conductivity. Additionally, fluctuations in dopant concentrations, gate oxide thickness and fixed charge will cause fluctuations of the local threshold voltage and the current gain (g_{fs}) of individual MOSFE's cells, which will also affect the local temperatures of the die.

Die temperature variations are mostly harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than the time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications are known to have limited capability to operate in the right-side bottom corner of the FBSOA graph.

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Typical Forward Characteristics of a Reverse Diode plotted against various temperatures are presented in **Figure 28**. This curve aids in comprehending the diode's conduction behavior and its forward voltage drop characteristics. It clearly demonstrates the negative temperature coefficient of diode forward voltage V_{SD} in the low-current region. As a result, it is anticipated that the diode forward voltage will decrease as the temperature increases. In the high-current region that is above the cross-over point (Q), the diode forward voltage will increase as the temperature increases.

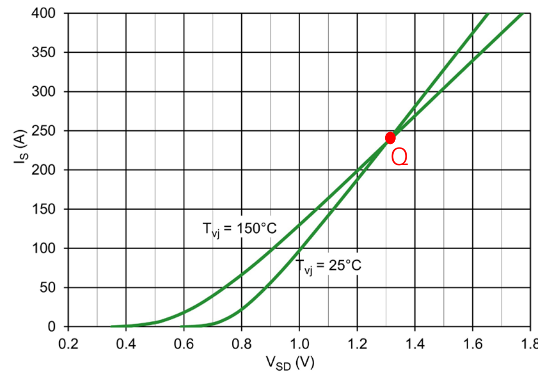

Figure 28. Typical Forward Characteristics of a Reverse Diode

Typical E_{oss} vs. Drain-Source Voltage - E_{oss} refers to the output switching energy. Specifically, it represents the energy that is required to charge or discharge output capacitance of a MOSFET during the switching operation.

$$Q_{oss} = \int_0^{V_{DS}} C(v)\ dv \tag{14}$$

$$E_{oss} = Q_{oss} \cdot V_{DS} \tag{15}$$

Where in this equation, Q_{oss} is the amount of charge required for charging the drain-source capacitance and C(v) is a function of the output capacitance C_{oss} that is dependent on drain to source voltage V_{DS} as shown in **Figure 29**.

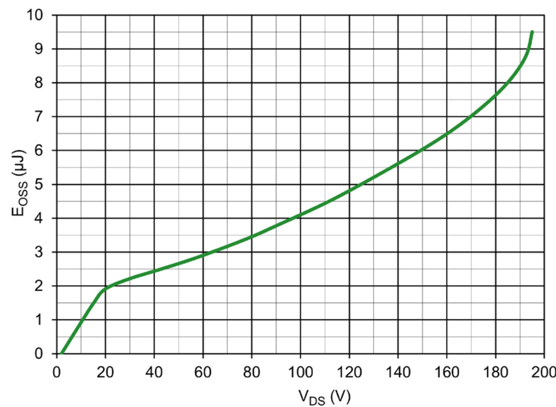

Figure 29. Typical E_{oss} vs. Drain-Source Voltage

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Typical Transient Thermal Impedance - A Power MOSFET has a virtual junction temperature, T_{vj} limitation. It should be operated below the maximum virtual junction temperature, $T_{vj(max)}$ specified in the datasheet to ensure reliability. The heat generated within the silicon chip needs to be dissipated by means of a heat sink into the ambient environment. The virtual junction temperature's rise above the ambient temperature T_a and is directly proportional to this heat flow and the junction-to-ambient thermal resistance, $R_{th(j\text{-}a)}$. The steady-state virtual junction temperature can be calculated by:

$$T_{vj} = P_{tot} \cdot R_{th(j-a)} + T_a|_{T_{vj} \le T_{vj(max)}} \quad (16)$$

Here, P_{tot} is the maximum power dissipated in the junction. The total thermal resistance between junction and ambient is,

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad (17)$$

The steady-state thermal resistance is not sufficient when calculating the peak virtual junction temperatures for pulsed applications. When a power pulse is applied to the device, the peak virtual junction temperature varies depending on peak power and pulse width. The temperature swing due to short pulses of power can be calculated using the thermal impedance Z_{th}.

$$Z_{th(j-c)}(t) = r(t) \cdot R_{th(j-c)} \quad (18)$$

Here, r(t) is a time dependent factor that is defined by the thermal capacity of the device. For short pulses, the r(t)-value is small but for long pulse, it approaches 1, which means that the thermal impedance approaches the steady-state thermal resistance. A typical thermal impedance curve is shown in **Figure 30**, approaching the steady-state value for pulses exceeding a duration of about one second. The thermal impedance can be used to estimate the peak temperature rise for square wave power pulses, which is typical in power supply design circuits.

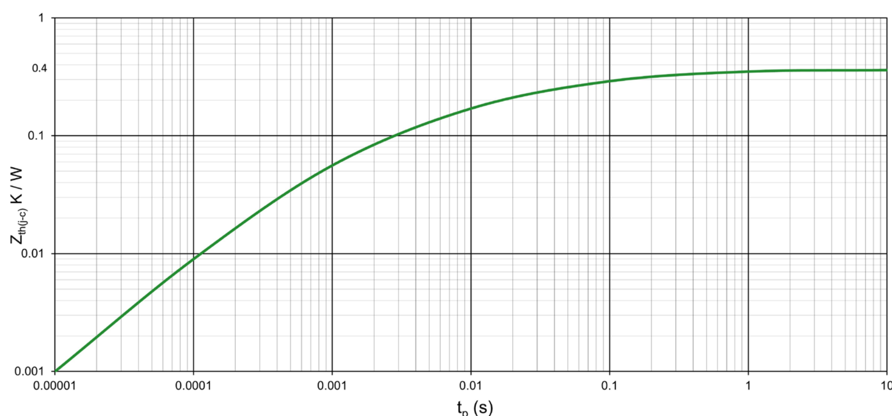

Figure 30. Typical Thermal Impedance

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