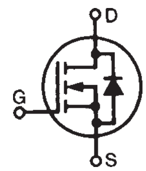
IXYS

LinearL2™ Power MOSFET w/ Extended FBSOA

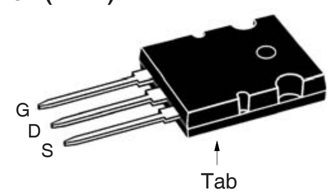
IXTK90N25L2
IXTX90N25L2

V_{DSS} = 250V
I_{D25} = 90A
$R_{DS(on)}$ ≤ 36mΩ

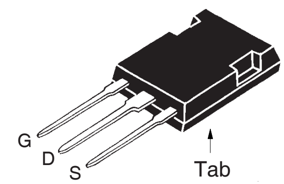


N-Channel Enhancement Mode
Avalanche Rated

TO-264 (IXTK)



PLUS247 (IXTX)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	250	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	250	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	90	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	360	A
I_A	T_C = 25°C	45	A
E_{AS}	T_C = 25°C	3	J
P_D	T_C = 25°C	960	W
T_J		-55...+150	°C
T_{JM}		150	°C
T_{stg}		-55...+150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 /4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	250			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 3mA	2.0		4.5	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±200	nA
I_{DSS}	V_{DS} = V_{DSS}, V_{GS} = 0V			50	µA
	T_J = 125°C			2.5	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 0.5 • I_{D25}, Note 1			36	mΩ

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators

Symbol	Test Conditions ($T_J = 25°C$, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10V, I_D = 0.5 • I_{D25}, Note 1	35	50	65	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		23		nF
C_{oss}			2140		pF
C_{rss}			360		pF
$t_{d(on)}$	**Resistive Switching Times** V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 1Ω (External)		50		ns
t_r			175		ns
$t_{d(off)}$			40		ns
t_f			160		ns
$Q_{g(on)}$	V_{GS}= 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		640		nC
Q_{gs}			125		nC
Q_{gd}			385		nC
R_{thJC}				0.13	°C/W
R_{thCS}			0.15		°C/W

Safe Operating Area Specification

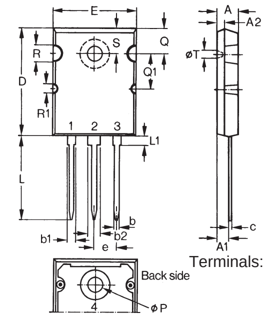
Symbol	Test Conditions	Characteristic Values Min.	Typ.	Max.	
SOA	V_{DS} = 250V, I_D = 2.3A, T_C = 75°C, Tp = 5s	575			W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25°C$, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			90	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			360	A
V_{SD}	I_F = 45A, V_{GS} = 0V, Note 1			1.5	V
t_{rr}	I_F = 45A, -di/dt = 100A/μs, V_R = 80V, V_{GS} = 0V		266		ns
I_{RM}			23		A
Q_{RM}			3.0		μC

Note: 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

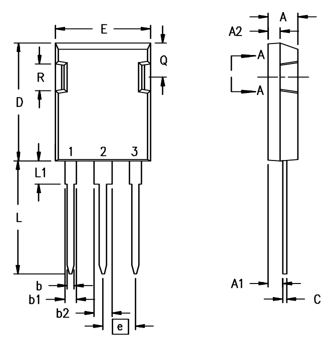
TO-264 AA Outline



Terminals: 1 - Gate
2 - Drain
3 - Source
4 - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

PLUS 247™ Outline



Terminals: 1 - Gate
2 - Drain
3 - Source

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ T_J = 25ºC

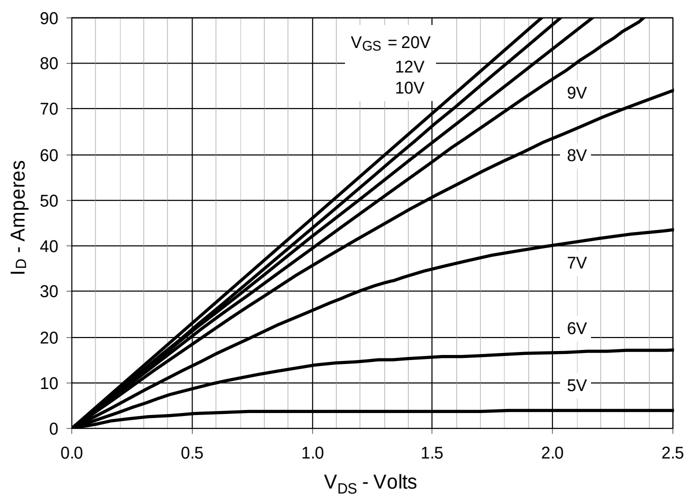


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

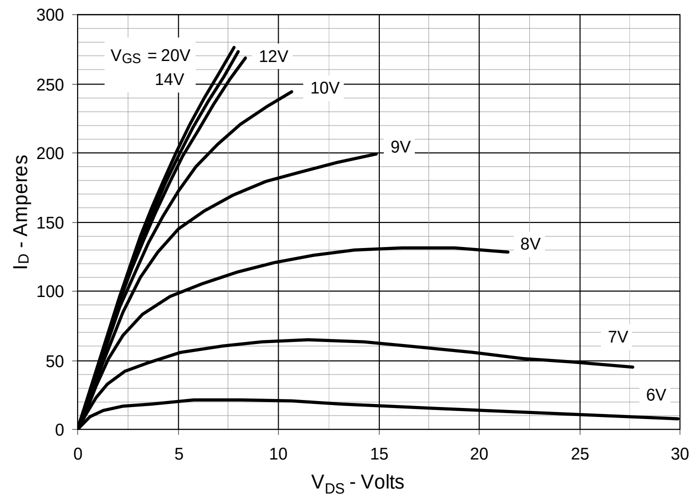


Fig. 3. Output Characteristics @ T_J = 125ºC

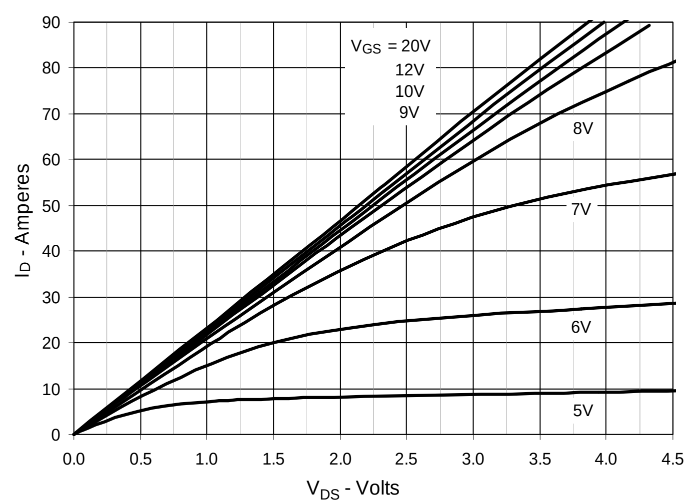


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 45A Value vs. Junction Temperature

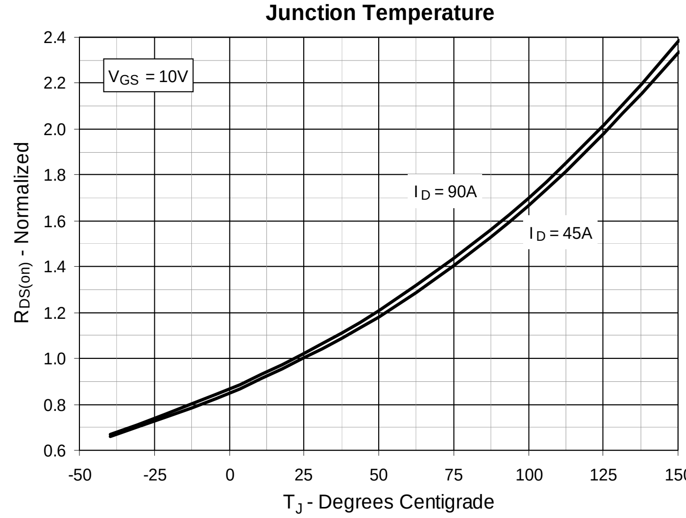


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 45A Value vs. Drain Current

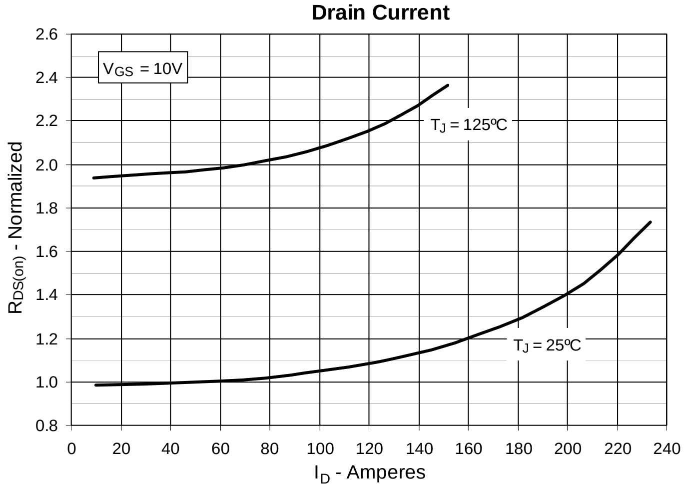


Fig. 6. Maximum Drain Current vs. Case Temperature

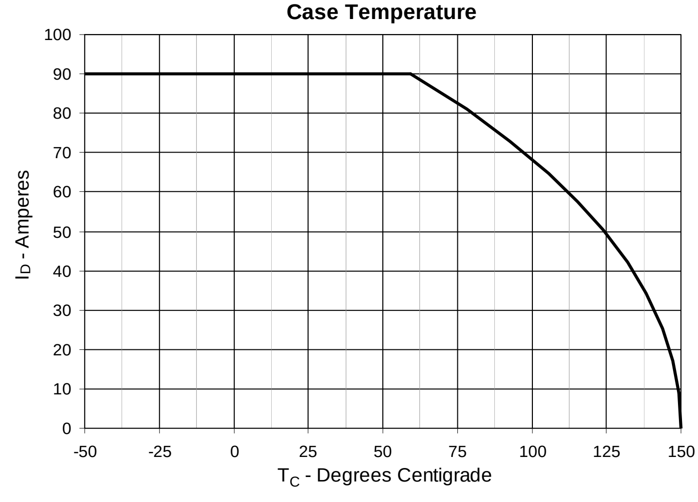


Fig. 7. Input Admittance

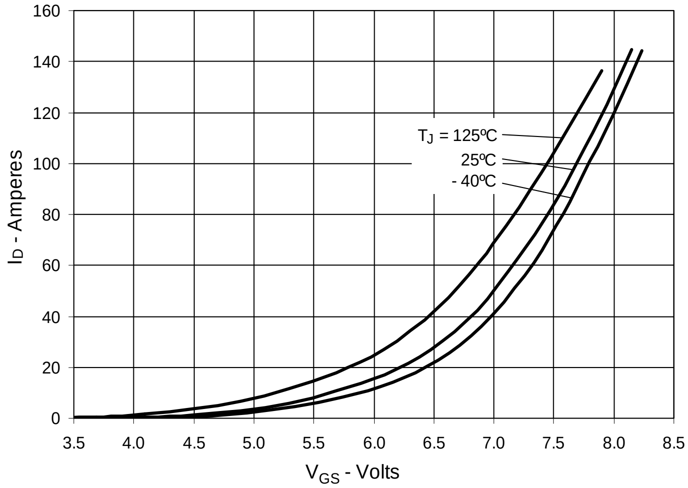


Fig. 8. Transconductance

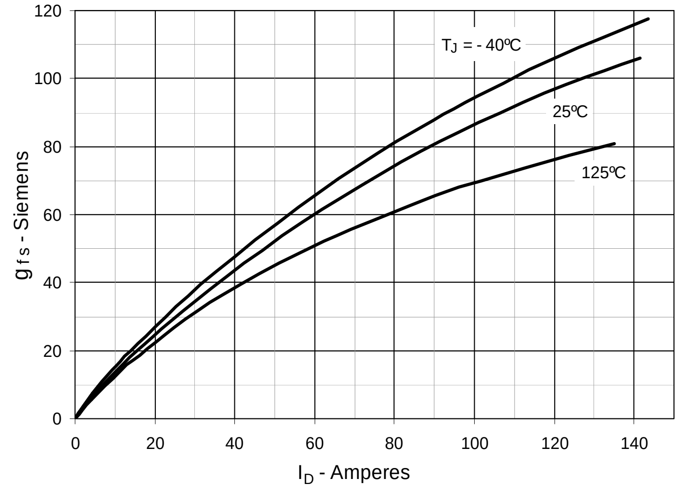


Fig. 9. Forward Voltage Drop of Intrinsic Diode

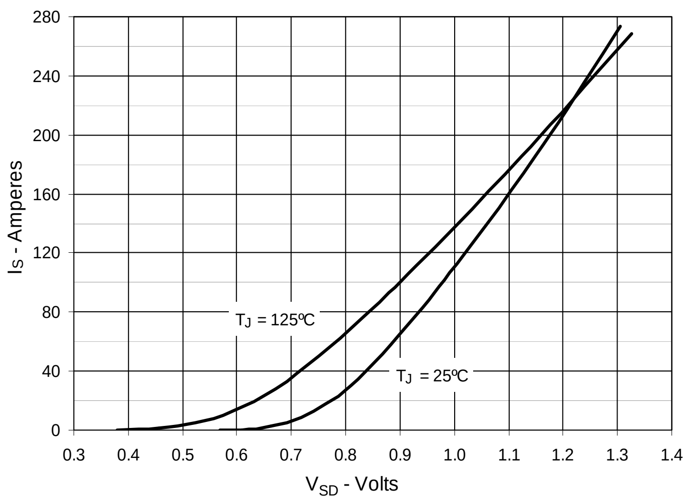


Fig. 10. Gate Charge

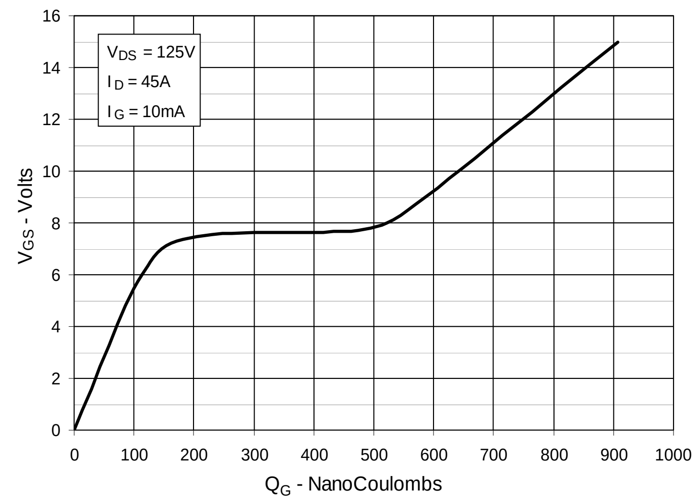


Fig. 11. Capacitance

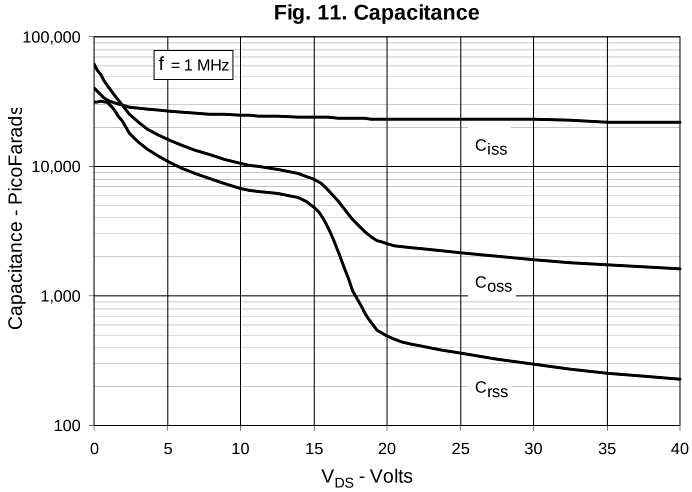


Fig. 12. Maximum Transient Thermal Impedance

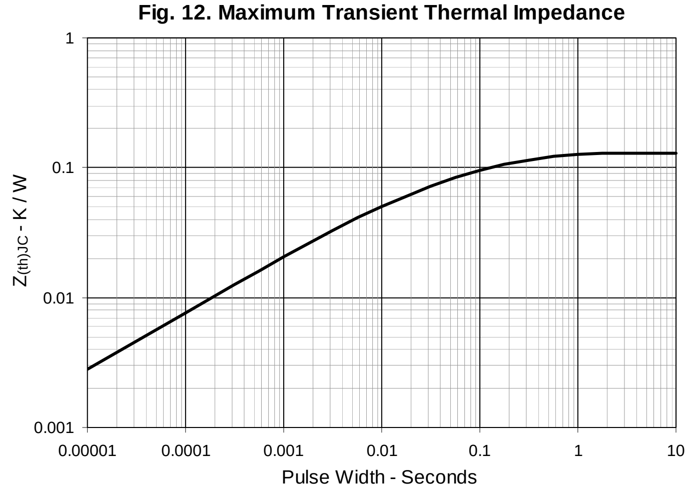


Fig. 13. Forward-Bias Safe Operating Area @ T_C = 25ºC

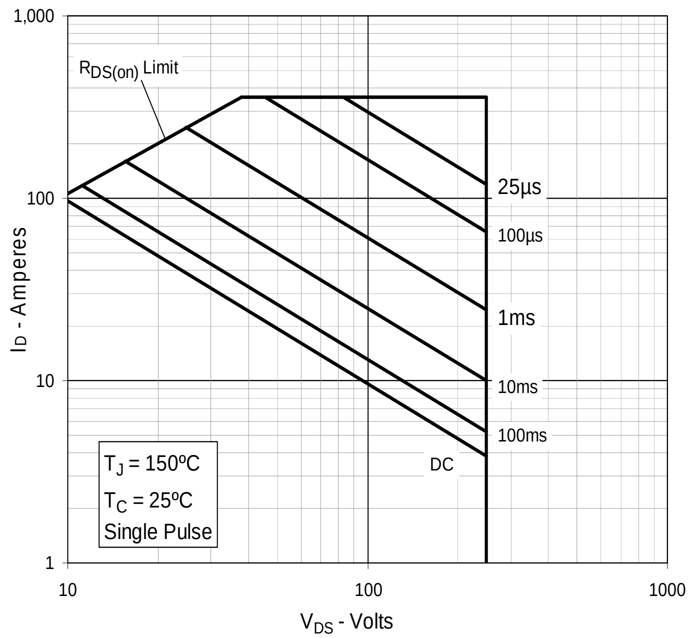
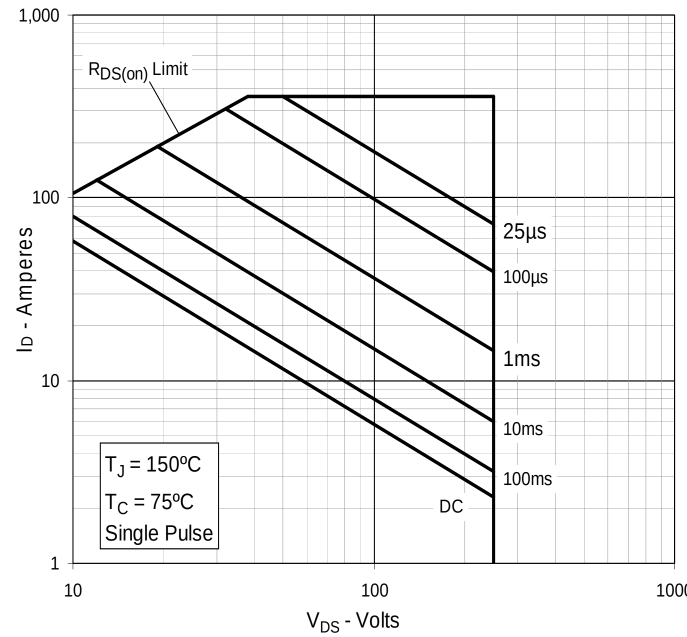


Fig. 14. Forward-Bias Safe Operating Area @ T_C = 75ºC



IXYS
A Littelfuse Technology

MOSFETs 线性区工作模式下的耐受能力

概述

在有些应用中，如电子负载，需要功率 MOSFET 工作在线性区。针对这些应用，Littelfuse 开发出一新型的MOSFET，扩展了它的FBSOA(正偏安全工作区)，从而更加适合此类应用。

应用

- 音频功放
- 电子负载
- 线性稳压器

目标受众

有别于常见应用于开关模式的 MOSFET, 此文章为工程师提供使用于线性模式的 MOSFET 的信息。

联系方式

有关此主题的更多信息，请联系 Littelfuse 功率半导体产品和应用专家团队：

- 北美洲 – NA_PowerSemi_Tech@Littelfuse.com
- 中美洲及南美洲 – CSA_PowerSemi_Tech@Littelfuse.com
- 欧洲，中东及非洲– EMEA_PowerSemi_Tech@Littelfuse.com

  亚洲、澳大利亚和太平洋岛屿– APAC_PowerSemi_Tech@Littelfuse.com

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1. 介绍

功率 MOSFET 最常用于开关模式应用中，它们起到开关的作用。然而，在电子负载、线性稳压器或 A 类放大器等应用中，功率 MOSFET 必须在其线性区域工作。在这种工作模式下，MOSFET 会承载较高的热应力。由于较高的漏源极电压和漏极电流同时出现，导致芯片承载较高的热应力。

当热电应力超过临界极限时，硅中会出现热点，导致器件失效。 为防止此类失效，工作在线性区域的 MOSFET 需要高功率耗散能力和扩展的正向偏置安全工作区 (FBSOA)。

Littelfuse 开发了一系列线性功率 MOSFET，通过抑制电热不稳定性的正反馈，实现了扩展的 FBSOA。这些新型 MOSFET 的设计特点是晶体管晶胞具有不同阈值电压，并且根据电流的热分布效应，晶胞在晶圆上也遵循不均匀分布的设计。

每个晶体管的晶胞的源极都设计有一个镇流电阻，以限制其电流。 图 1 显示了 MOSFET 结构的示意图。 n 和 p 掺杂区形成了一个寄生的 NPN 晶体管。

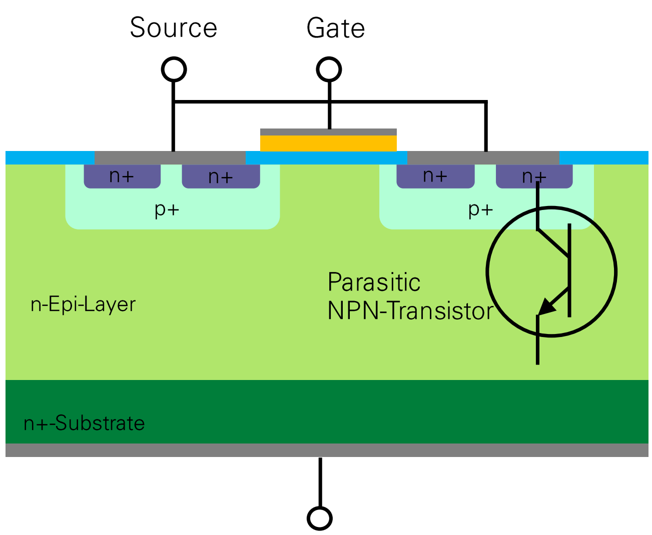

图 1.包含寄生双极结晶体管(BJT)的 MOSFET 结构

每个晶胞的寄生双极结晶体管(BJT)被旁路掉，因此它在极端的电应力条件下不会打开。此外，每个功率 MOSFET 的热响应都是单独测试的，以确保不会出现焊料空洞，从而避免出现局部热点。线性 MOSFET 的有效性可以在为电源测试而开发的电子负载的设计中得到验证。

2. 二次击穿

在功率 MOSFET 中，术语二次击穿是指 MOSFET 的阻断电压能力突然降低，随后 MOSFET 失去电流控制。 尽管在大多数应用中，MOSFET 通常不会遭受二次击穿，但这种潜在的破坏性情况可能是由于硅中的热点或"电流聚集"而发生的，而这反过来又会激活 MOSFET 的寄生 BJT 的导通，从而失去门极对电流的控制。

通常情况下，当电流试图集中到一个局部区域时，由于正温度系数的影响，热点温度的升高会提高热点的电阻，并将电流重新分配到远离热点的位置。[1]这一属性有助于多个 MOSFET 的并联操作。

然而，电子负载、A 类和 AB 类放大器等应用会导致功率 MOSFET 在其线性区域工作，在该区域，它们必须消耗比更常见的通断开关更高的功率水平。在这种情况下，电流聚集和热点的形成可能无法自我校正，这可能会导致器件失效。

在线性模式下，功率 MOSFET 由于同时承载高电压和大电流而产生的较高热应力。当热应力超过临界极限时，芯片中就会出现热点，导致器件失效。[2]

图 2 描绘了 n 沟道功率 MOSFET 的典型输出特性，其中描述了不同的工作模式。

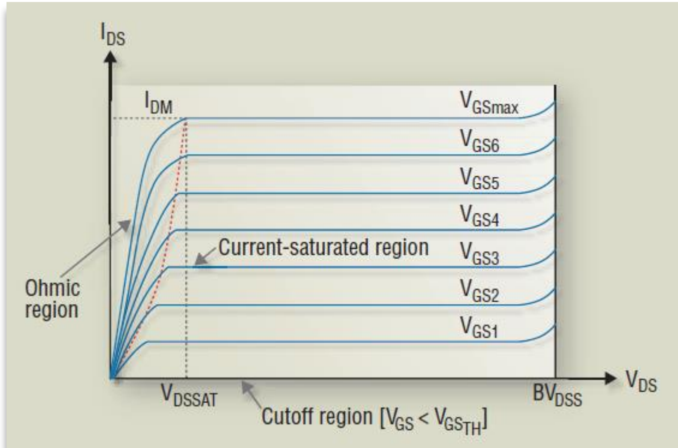

图 2. N 沟道 MOSFET 的三种可能工作模式

在截止区，栅源电压V_{GS}低于阈值电压$V_{GS_{TH}}$，器件处于关断状态。 在欧姆区，器件特性类似于电阻，具有几乎恒定的导通电阻 $R_{DS_{ON}}$，它等于漏极电压 V_{DS} 除以漏极电流I_{DS}。 在线性工作模式下，器件工作在电流饱和区，其中I_{DS} 是栅源电压 V_{GS} 的函数，定义如下：

$$\boldsymbol{I_{DS} = K\left(V_{GS} - V_{GS_{TH}}\right)^2 = g_{FS}(V_{GS} - V_{GS_{TH}})} \quad (1)$$

其中 K 是一个取决于温度和器件几何形状的参数，g_{FS}是电流增益或跨导。

当 V_{DS} 增加时，漏极电压与栅极电压偏置相反，并降低了沟道中的表面电压。 沟道反型层电荷随着V_{DS} 的增加而减少，最终在漏极电压等于 $V_{GS} - V_{GS_{TH}}$时变为零。 该点称为通道夹断点，漏极电流在此处饱和。[3]

FBSOA 是定义最大允许工作点的数据表。图 3 显示了 n 沟道功率 MOSFET 的典型 FBSOA 特性。它受最大漏极到源极电压V_{DSS}，最大导通电流I_{DM}和不同工作持续时间的恒定功率耗散线的限制。

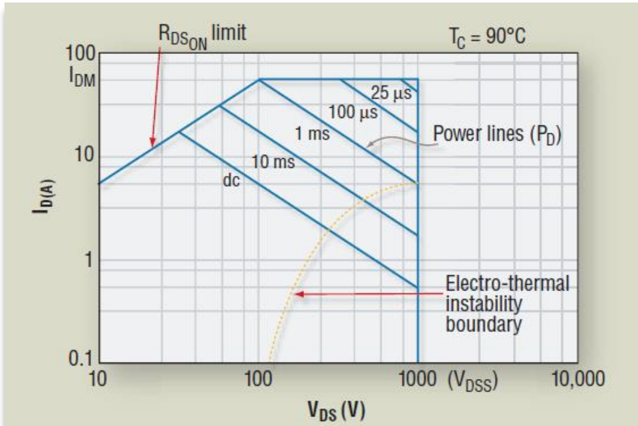

图 3. 为开关模式设计优化的功率 MOSFET，因热不均匀性，导致在实际的 FBSOA 应用中承载能力有限。

在图 3 中，这组曲线代表一条直流线和四条单脉冲工作线：10 ms、1 ms、100 µs 和 25 µs。 每条线的顶部被截断以限制最大漏极电流，并以由器件导通电阻定义的正斜率线为界。每条线路的右侧均终止于额定漏极到源极电压极限。 每条线都有一个负斜率，由器件 P_D的最大允许功耗决定：

$$P_D = \frac{(T_{Jmax} - T_C)}{Z_{thJC}} = V_{DS} \cdot I_D \quad (2)$$

其中，Z_{thJC} 是结到壳瞬态热阻抗，T_{Jmax} 是 MOSFET 的最大允许结温。

这些理论恒定功率曲线是在假设结温在整个功率 MOSFET 芯片上基本均匀的情况下从计算得出的。 由于多种原因，这种假设并不总是有效的，尤其是对于大芯片 MOSFET。 首先，焊接到功率封装安装片的 MOSFET 芯片边缘的温度通常低于芯片中心，这是横向热流的结果。 其次，材料缺陷，比如芯片焊接空洞或导热硅脂气泡，可能会引起热导率局部降低，从而导致芯片上某些特定点温度升高。 第三，掺杂浓度和栅氧化层厚度的波动，以及存储电荷会导致局部阈值电压和 MOSFET 晶胞的电流增益 g_{FS} 的波动，这也会影响芯片的局部温度。

在开关模式下，芯片温度的波动大多是无害的。 然而，这些波动可能会在线性模式中触发灾难性失效。 在图 3 中 FBSOA 图表的右下角，即电热不稳定性 (ETI) 边界右侧的区域，发现针对开关模式应用优化的功率 MOSFET 的承载能力有限。

ETI 可以理解为功率 MOSFET 表面强制进入线性工作模式的正反馈机制的结果：

- 局部结温升高
- 结温升高会导致$V_{GS_{TH}}$ 局部降低，因为 MOSFET 的阈值电压具有负温度系数
- 降低$V_{GS_{TH}}$会导致局部电流密度的增加，使得$J_{DS} \sim (V_{GS} - V_{GS_{TH}})^2$
- 局部电流密度的增加导致局部功耗增加，从而导致结温进一步局部升高

根据功率脉冲的持续时间、传热条件和 MOSFET 晶胞设计的特点，ETI 可能会导致所有 MOSFET 电流集中并形成热点。 这通常会导致受影响区域中的 MOSFET 晶胞失去栅极控制并开启寄生 BJT，从而导致器件损坏。

针对这些问题，Littelfuse 开发了一种新型的功率 MOSFET 结构和工艺，通过抑制 ETI 的正反馈来提供扩展的 FBSOA。这些新型 MOSFET 的设计特点是晶体管晶胞呈不均匀分布，以及调整具有不同阈值电压的晶胞布局。[3]这种设计已被用于开发一系列具有扩展 FBSOA 的功率 MOSFET，非常适用于线性工作模式。

Littelfuse 这些 MOSFET 的规格书包含了特有的高温 FBSOA 图。 例如，图 4 展示了 Littelfuse IXTK22N100L 线性功率 MOSFET 的 FBSOA 图，并标记了其测试的直流工作点。

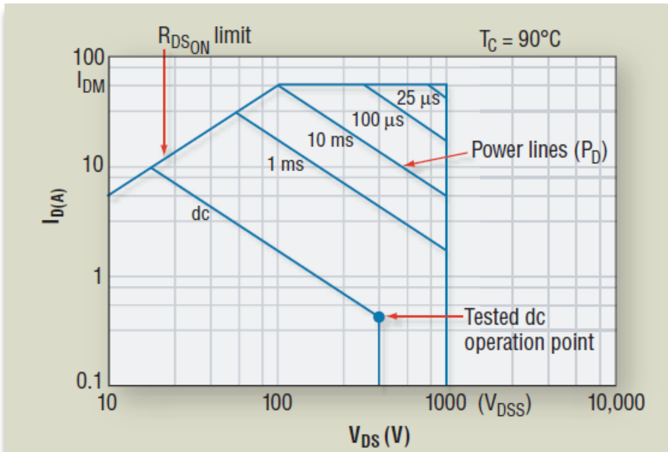

图 4. IXTK22N100L 线性功率 MOSFET 通过抑制电热不稳定性的正反馈来扩展 FBSOA

为了说明 Littelfuse 线性功率 MOSFET 设计的有效性，表 1 列出了一些具有扩展 FBSOA 功能的器件的主要规格。

表 1. 具有扩展 FBSOA 的 N 沟道功率 MOSFET

产品编号	V_{DSS} (V)	I_D (A)	$R_{\theta JC}$ (K/W)	T_C = 90° C 时，SOA 规格功率	封装类型
IXTH24N50L	500	24	0.31	200 at V_{DS} = 400 V, I_D = 0.5 A	TO-247
IXTN46N50L	500	46	0.18	240 at V_{DS} = 400 V, I_D = 0.6 A	SOT-227B
IXTK22N100L	1000	22	0.18	240 at V_{DS} = 800 V, I_D = 0.3 A	TO-264
IXTN30N100L	1000	30	0.156	300 at V_{DS} = 600 V, I_D = 0.5 A	SOT-227B

根据公式 2，额定电压为 1000 V 的单个功率 MOSFET（例如 IXTK22N100L）可提供 700 W 的额定功率。此额定功率通常用于开关模式的电路设计，但不适用于线性模式的应用。 对于线性模式，Littelfuse 提供了高温下的 FBSOA，例如 IXTK22N100L 在V_{DS} 等于 800 V、I_D 等于 0.3 A 以及T_C 等于 90°C 时为 240 W。

3. 应用实例

电子负载，通常用于测试电源，使用 Littelfuse 扩展 FBSOA 的线性 MOSFET，可以大幅提高可靠性。电子负载本质上是一个可编程电阻器，通常由多个高压功率 MOSFET 并联来实现。在此应用中，由于器件几何结构和机械装配的变化，电流在每个 MOSFET 中平均分配的可能性很小，这反过来又会导致器件参数(如击穿电压和电流增益)的变化。

为确保均流，通常采用反馈机制，即在每个 MOSFET 源极串联一个电阻。 该电阻检测每个 MOSFET 中的电流并反馈一个电压，其值基于动态范围的调整、输出端的噪声水平、最小负载电阻和系统的稳定性。 它通常设计用于 1 到 2 V 之间的最大额定值。系统的温度稳定性由电阻的温度系数决定。 [2]

以 2 A、600 V 稳压电源为例，需要使用由多个功率 MOSFET 并联组成电子负载来进行测试。该电子负载要求击穿电压至少为 600 V 的功率 MOSFET 能够消耗全部输出功率。输出功率定义为:

$$\boldsymbol{P_O = I_O \cdot V_O}$$

其中I_O等于 2A，V_O等于 600 V。这使得总功耗达到: $P_O = 2 \cdot 600\mathrm{W} = 1200W$

对于此应用，可以使用 IXTK22N100L 功率 MOSFET。 该器件具有 1000 V 的额定电压、22 A 的额定电流、240 W 的 FBSOA（或简称为 SOA）额定值和 700 W 的额定功耗。在图 5 中，FBSOA 显示其 SOA 点在 V_{DS} 等于 800 V，I_D 等于 0.3 A，T_C 等于 90°C，具有 240 W 的能力。 其 700 W 的额定功耗仅适用于开关模式应用，因此对于线性模式，由于功耗高，必须使用 SOA 额定值。 假设此额定值有 20% 的安全裕度，这会将其允许的 SOA 额定值降低到 192 W。

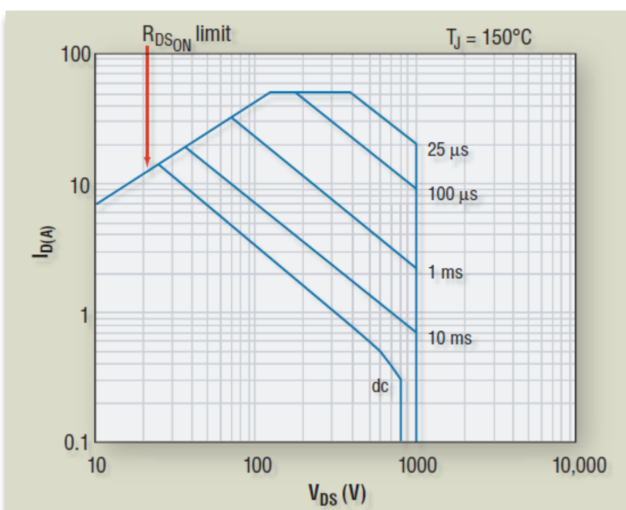

图 5. IXTK22N100L FBSOA 在 V_{DS} = 800 V、I_D = 0.3 A、TC = 90° C 时具有 240 W 功率耗散能力，以及其 SOA 工作 点

电源的最大输出功率为 1440 W，安全裕度为 20%，额定功率为 1200 W。可以看出，单个 MOSFET（如 IXTK22N100L）无法承载此总功率。因此，需要多个并联的功率 MOSFET 来承载总功率。 此应用所需的 MOSFET 数量为 1440 W 除以 192 W/器件等于 7.5 个器件，实际上需选用 8 个器件并联。

电子负载电路的典型结构如图 6 所示。 [2]

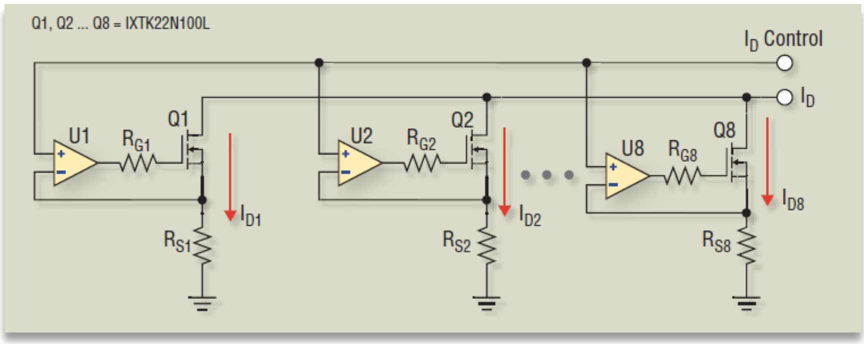

图 6. 使用线性 MOSFET 设计电子负载以测试 2 A 和 600 V 电源

图 6 中所示的栅极电阻器连接在每个运算放大器输出和 MOSFET 的每个栅极之间，用于限制栅极电流。 它是可调节的，其值可以在 5 Ω 和 50 Ω 之间选择。 源极电阻 RS1 到 RS8 检测每个 MOSFET 中的漏极电流。 电阻的容差决定了功率 MOSFET 之间的相对匹配。 源极电阻两端的电压施加到驱动功率 MOSFET 的每个运算放大器的反相输入端，同相输入端连接到流向运算放大器同相端的控制漏极电流。 [2]

Littelfuse 线性功率 MOSFET 通过扩展 FBSOA，克服了线性应用中传统功率 MOSFET 的局限性。 这种特性是通过晶体管晶胞的非均匀分布和使用具有不同阈值电压的晶胞来实现的，这有助于抑制 ETI 的正反馈。

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[3]Brega，B.Jayant等著，“Power Semiconductor Devices”，PWS出版公司，1996。

[4]Zommer，Nathan等著，“Monolithic Semiconductor Device and Method of Manufacturing Same”，美国专利号：US4860072, 1989年8月。

Littelfuse Discrete Power MOSFET Datasheet Explanation

Objectives

The primary objective of this application note is to enhance the comprehension and analysis of power MOSFET datasheet parameters and graphs. By breaking down the technical specification into digestible insights, designers can gain deeper insights into the functionality and performance characteristics of MOSFETs. This application note provides a general recommendation about how to read and understand a datasheet with all its parameters and diagrams. The information presented plays a pivotal role in determining the operational limits and thresholds of the device.

Applications

This application note is applicable to all scenarios where power MOSFETs are utilized.

Target Audience

This document is intended for designers and developers who are utilizing Power MOSFETs within their respective applications.

Contact Information

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1. Introduction

In the realm of modern electronics and power systems, an extensive understanding of semiconductor components, particularly the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), is crucial for achieving optimal system-performance and -efficiency. MOSFETs play a pivotal role in switching applications, offering versatile solutions. This document serves as a guide, delving into the detailed parameters presented in MOSFET datasheets. It aims to empower engineers and designers to make informed decisions and effectively leverage MOSFET capabilities in diverse applications.

Littelfuse furnishes datasheets with parameters that are essential and useful for selecting the appropriate device as well as for predicting its performance in specific application. This facilitates designers in comparing products from various suppliers and gaining valuable insights into the operational constraints of the device.

The outlined values in the datasheet describe the device's behavior under varying virtual junction temperature and testing conditions. Additionally, the dynamic characterization tests undergo execution utilizing precise configurations aimed at precise measurement of switching losses. As a result, discrepancies in these metrics manifest between the intended user applications.

The graphs included in the datasheet represent typical performance characteristics and can be used to extrapolate from one set of operating conditions to another. This application note explains parameters based on the IXTH120N20X4 datasheet which is an N-channel enhancement mode, power MOSFET. All the parameters mentioned in a Littelfuse datasheet are measured according to *IEC 60747-8* standards.

2. Essential Datasheet Insight

This section serves as an overview of important information found on the first page of the datasheet, including the datasheet status.

2.1. Key Information

The first page of the datasheet includes details such as the part number, pinout diagram, features and benefits, applications, and key attributes of the product.

- **Part Number** indicates the manufacturer, MOSFET type, package type, current rating, channel type, voltage class, technology series and a suffix for some special packages that gives extra information such as high voltage package, over molded package, and w/ 4 leads. Designation of MOSFET part number is drafted in **Figure 1**. The detailed information about this can be found as part number nomenclature - discrete Si MOSFET on Littelfuse website.

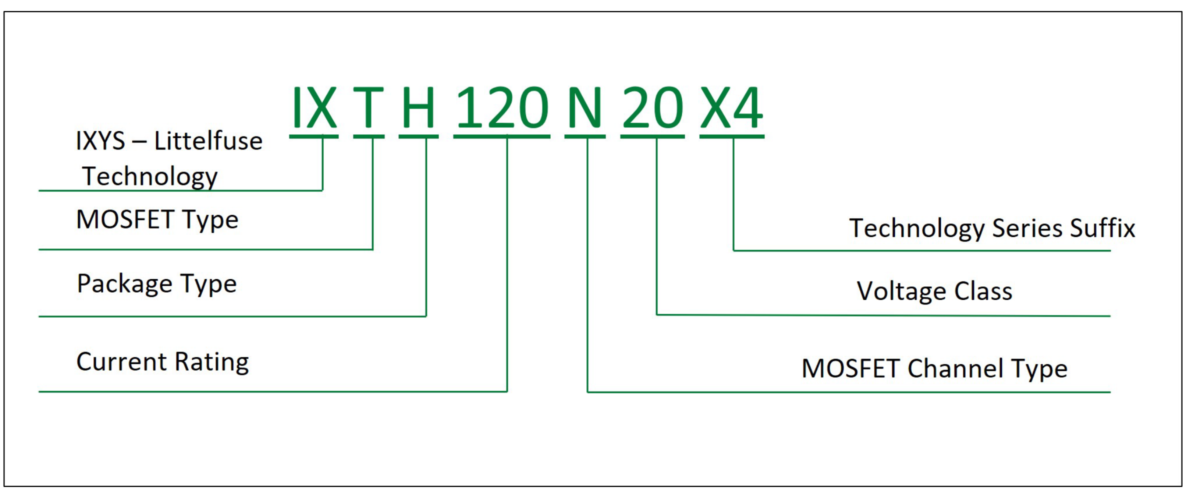


Figure 1. Part Number Designation

- **Pinout Diagram** provides a visual representation of the device’s physical layout including circuit symbol as highlighted in **Figure 2**.

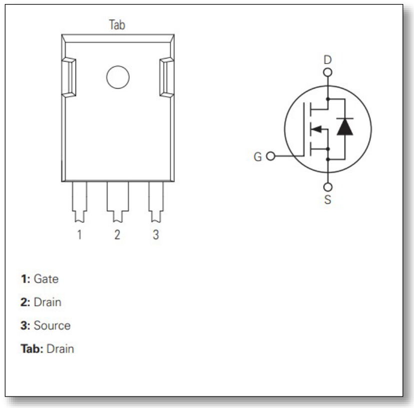


Figure 2. Pinout Diagram of TO-247 and Circuit Symbol of an N-channel Enhancement Mode MOSFET

- **Features and Benefits** encompasses a comprehensive list of features and their corresponding benefits offered by the MOSFET device, which helps user acquire a better understanding of how the MOSFET can meet their specific application requirements to deliver optimal performance and reliability.
- **Key Attributes / Product summary** highlights the key specifications and performance characteristics of the MOSFET, including parameters such as maximum drain-source voltage (V_{DSS}), maximum drain current (I_D) at 25°C, and on-state resistance ($R_{DS(on)}$) as pointed out in **Table 1**.

Table 1. Key Attributes/Product Summary

Characteristic	Value	Unit
V_{DS}	200	V
I_D @ 25 °C	120	A
$R_{DS(on)}$	≤ 9.5	mΩ

2.2. Datasheet Status

There are three distinct types of datasheets, each corresponding to a different stage of the product development or documentation process, depending on the degree of completeness, correctness, or approval.

- **Target datasheet:** During product development, the term *target datasheet* denotes a document laying out the desired product specifications, characteristics, and performance attributes. The development team uses this document to guide their efforts.
- **Preliminary datasheet:** Created before reaching its final, approved format. It is an early or preliminary representation of a product's specifications, features, and characteristics. The difference between a preliminary datasheet and a final datasheet is that certain data values are still missing. The missing values in the preliminary data sheet are noted as to be defined (TBD). These datasheets are made using the engineering samples that are in early phase of development.
- **Final datasheet:** Detailed and authoritative document that contains all the values that were missing in the preliminary datasheet. The parameters specified in the final datasheet are explained in this document. Any major change with respect to a MOSFET’s characteristics in the final datasheet is associated with a Product Change Notification (PCN).

3. MOSFET Datasheet Parameters

This section serves as a thorough exploration of the various parameters detailed within a MOSFET's datasheet. It describes the MOSFET's performance and characteristics, from maximum ratings to static and dynamic parameters, thermal properties, and package-related factors.

3.1. Maximum Ratings

The maximum ratings at which the MOSFET can be operated are listed on the second page of the datasheet in a table that summarizes the electrical and thermal limits of the device. The maximum ratings provided in the data sheets are absolute in nature. If any of the maximum ratings are surpassed, it is to be expected that the semiconductor experiences fatal failure, regardless of whether the remaining maximum ratings are utilized to their full extent. Unless otherwise noted, the values are applicable at a virtual junction temperature (T_{vj}) of 25°C. **Table 2** lists the maximum ratings designated for the IXTH120N20X4.

Table 2. IXTH120N20X4 MOSFET Maximum Ratings

Symbol	Characteristic	Conditions		Value	Unit
V_{DSS}	Drain-source voltage	25 °C ≤ T_{vj} ≤ $T_{vj(max)}$		200	V
V_{GSS}	Gate-source voltage	–		± 20	V
V_{GSM}	Transient gate-source voltage	$t_{transient}$ = 1 ms		± 30	V
I_D	Drain current	–	T_c = 25 °C	120	A
			T_c = 100 °C	89	A
I_{DM}	Peak drain current	T_c = 25 °C, Pulse width limited by $T_{vj(max)}$		240	A
I_S	Diode forward current	V_{GS} = 0 V		120	A
I_{SM}	Diode peak forward current	Pulse width limited by $T_{vj(max)}$		480	A
I_{AS}	Non-repetitive single pulse avalanche current	–		60	A
E_{AS}	Non-repetitive single pulse avalanche energy	–		1	J
dv/dt	Diode dv/dt capability	V_{DS} = 0...... 200 V, I_S ≤ 120 A		20	V/ns
P_{tot}	Total power dissipation	T_c = 25 °C		417	W
T_{vj}	Virtual junction temperature range	–		−55 to +175	°C
$T_{vj(max)}$	Maximum virtual junction temperature	–		175	°C
T_{stg}	Storage temperature range	–		−55 to +175	°C
T_{sld}	Soldering temperature	1.6 mm (0.062 in.) from case 10 s		300	°C
M_s	Mounting torque for screws to heat sink	–		1.3/10	Nm/lb.in

Drain-source voltage (V_{DSS}) is the crucial parameter in datasheets, representing the maximum voltage that can be applied across drain and source while the gate and source are being connected or V_{GS} = 0 V. It sets the limit to prevent breakdown and maintain operational functionality.

Gate-source voltage (V_{GSS}) and **Transient gate-source voltage (V_{GSM})** are visually delineated in **Figure 3**, offering a clear understanding of their roles in MOSFET operation. The gate-source voltage (V_{GSS}) denotes the maximum steady-state voltage that can be applied across gate and source without the gate oxide being damaged. Conversely, transient gate-source voltage (V_{GSM}) refers to the peak voltage that the gate terminal of the MOSFET can endure within a specified transient period ($t_{transient}$) or temporary change in voltage.

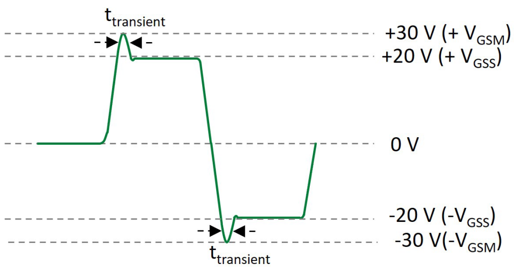


Figure 3. Gate-Source Voltage Definition

Drain current (I_D) acts as a pivotal metric, outlining the maximum continuous current through the drain at a given case temperature T_c, of 25°C. Its calculation is based on several factors, including the maximum power dissipation P_{tot}, the temperature difference junction to case, the thermal resistance junction to case $R_{th(j-c)}$, and the maximum on-resistance $R_{DS(on)}$. Additionally, the temperature dependence of the on-state resistance is considered, as detailed in **Equation 1** and **Equation 2**. The drain current can be limited by the current handling capacity of leads or terminals.

$$P_{tot} = \frac{T_{vj(max)} - T_c}{R_{th(j-c)}} = I_D{}^2 \cdot R_{DS(on)}|_{T_{vj}=T_{vj(\max)}} \quad (1)$$

Solving for I_D as

$$I_D = \sqrt{\frac{T_{vj} - T_c}{R_{th(j-c)} \cdot R_{DS(on)}\,|_{T_{vj}=T_{vj(\max)}}}} \quad (2)$$

Peak drain current (I_{DM}) signifies the peak current that the device can handle above the I_D specification under the maximum virtual junction temperature. It varies with the current pulse width and heat dissipation conditions. **Figure 4** demonstrates the forward-bias safe operating area (FBSOA) of a MOSFET, which indicates the maximum pulse width at which the device can handle specific current without experiencing failure.

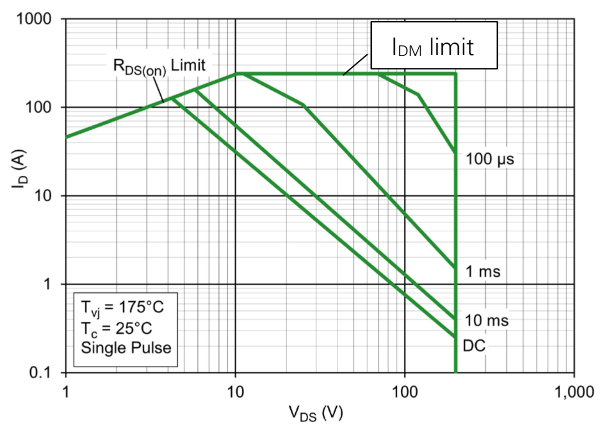


Figure 4. Forward-Bias Safe Operating Curve

Diode forward current (I_S) relates to the maximum DC forward current the body diode can handle in the forward direction at particular case temperature, which is typically equivalent to the MOSFET's continuous drain current I_D.

Diode peak current (I_{SM}) is an indicative of the peak current the diode can handle above diode forward current specification under maximum virtual junction temperature, which is typically equivalent or higher than the MOSFET's peak drain current I_{DM}.

Diode dv/dt capability corresponds to the maximum allowable rate of change of voltage across the body diode during the reverse recovery period without causing undesired effects. The power MOSFET structure contains a parasitic bipolar junction transistor (BJT), which could be activated by an excessive rise rate of the drain-source voltage (dv/dt), particularly after the recovery of the body diode.

Total power dissipation (P_{tot}), as expressed in Equation 1 , encompasses the maximum calculated power that the device can dissipate, serving as a function influenced by both maximum virtual junction temperature $T_{vj(max)}$, and the thermal resistance junction to case $R_{th(j-c)}$ at a case temperature of 25°C.

Virtual junction temperature (T_{vj}) range is –55 to 150°C or –55 to 175°C in most cases and it is the permissible temperature range in which the MOSFET may be operated continuously. The maximum virtual junction temperature $T_{vj(max)}$ is 150°C or 175°C depending on the technology. The negative temperature limit for Littelfuse discrete MOSFETs is typically –55 °C. The virtual junction temperature influences the electrical parameters of a MOSFET. For instance, at very high temperatures, the device's threshold voltage is reduced, and the leakage current increases, which leads to thermal runaway within the device.

Storage temperature (T_{stg}) range points to the range of temperatures where the device can be safely stored or transported without adversely affecting its performance or reliability. The range is usually between –55°C to 150°C.

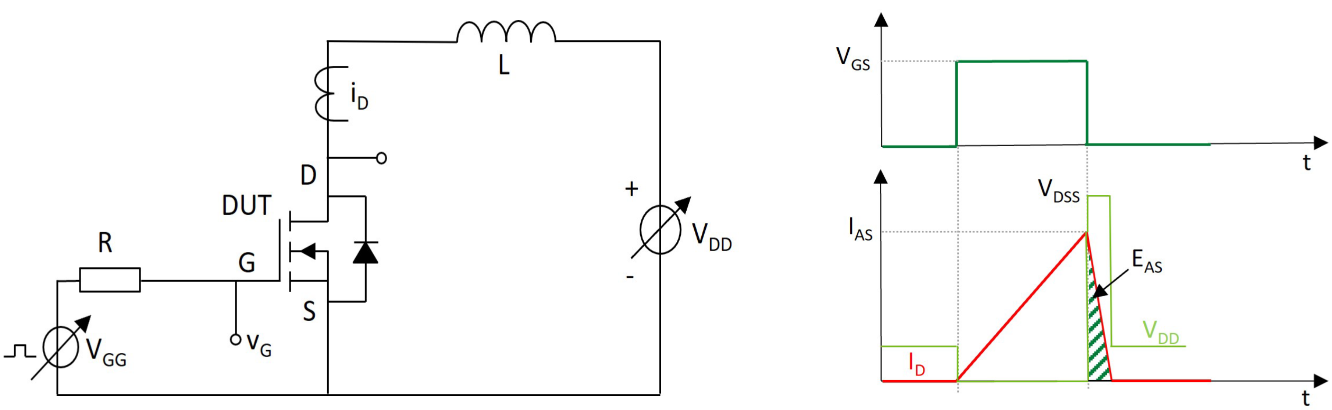
Soldering temperature (T_{sld}) enumerated in the datasheet implies the temperature at which the device can be safely soldered to the Printed Circuit Board (PCB) during the assembly process. The maximum soldering temperature is typically 300°C for devices with leads and 260°C for Surface Mount Devices (SMD).

Mounting torque (M_s) for screws to heatsink is the recommended maximum torque that can be applied during the process of mounting the MOSFET to a heatsink or a PCB. **Mounting torque (M_t)** for screws to terminals is the suggested torque that shall be applied to screwed terminals.

Mounting force (F) is the maximum force for pressure mounted devices, fixed by clips, that shall be applied to the isolated devices.

Non-repetitive single pulse avalanche current (I_{AS}) and Non-repetitive single pulse avalanche energy (E_{AS}) are specified only for avalanche-rated devices. I_{AS} denotes the maximum current that the MOSFET can endure during a single avalanche event without sustaining damage. Whereas E_{AS} quantifies the total energy absorbed by the device during such an event, indicating its ability to withstand high-energy transient events without permanent damage.

In **Figure 5 (a)**, the Unclamped Inductive Switching (UIS) test circuit, used to test the avalanche capability of a power MOSFET is depicted. In **Figure 5 (b)**, the waveforms during avalanche breakdown are presented. A gate pulse turns-on the MOSFET and allows the current (I_D) to ramp up according to the inductor's value (L) and the drain supply voltage (V_{DD}). At the end of gate pulse, the MOSFET turns-off causing the voltage across the MOSFET to rise sharply. The over voltage is clamped at the breakdown voltage (V_{DSS}) until the load current reaches zero and all the energy is dissipated. The green area shaded in **Figure 5 (b)** is the avalanche energy E_{AS}.



(a) Unclamped Inductive Switching   **(b) Waveforms during Avalanche Breakdown**

Figure 5. Typical Avalanche Test Circuit

Non-repetitive single pulse avalanche energy is calculated from the **Equation 3**:

$$E_{AS} = \frac{1}{2} \cdot L \cdot {I_{AS}}^2 \cdot \frac{V_{DSS}}{(V_{DSS} - V_{DD})} \qquad 3$$

where V_{DSS} is the drain-source avalanche voltage.

Note : When V_{DD} is set to a smaller value compared to V_{DSS}, then E_{AS} is calculated by using the approximation equation of $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2$

3.2. Static Electrical Characteristics - MOSFET

Static electrical characteristics are the set of parameters and properties that describe the device behavior under steady-state condition. Most of the parameters included in the datasheet, along with their typical ranges of variance is listed in **Table 3**. In accordance with IEC 60747-8{ed3.1}, the characteristics of Power MOSFETs are provided at 25°C and, when necessary, at another higher operating temperature.

Table 3. MOSFET Static Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$V_{(BR)DSS}$	Breakdown voltage, drain-source	V_{GS} = 0 V, I_D = 250 µA		200	–	–	V
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DS} = V_{GS}$, I_D = 250 µA		2.5	–	4.5	V
I_{DSS}	Drain-source leakage current	$V_{DS} = V_{DSS}$, V_{GS} = 0 V	T_{vj} = 25 °C	–	–	25	µA
			T_{vj} ≤ 150 °C	–	–	500	
I_{GSS}	Gate leakage current	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±100	nA
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, I_D = 0.5 · I_D	T_{vj} = 25 °C	–	–	9.5	mΩ

Breakdown voltage, drain-source ($V_{(BR)DSS}$) corresponds to the minimal blocking voltage between drain and source, measured according to **Figure 6**, at a specified collector current while the gate and source are connected.

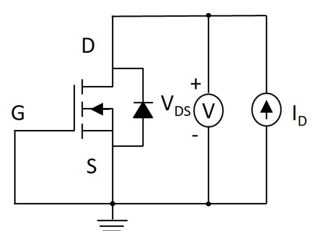


Figure 6. Circuit Diagram to Measure Breakdown Voltage

Gate-source threshold voltage ($V_{GS(th)}$) is the voltage measured across gate to source at which the drain current begins to flow, and the device is at on-state. It has a negative temperature coefficient. The circuit diagram illustrating the measurement of $V_{GS(th)}$ is depicted in **Figure 7**. Initially, the drain pin and the gate pin are short, after which drain current is applied while observing the gate-source voltage ($V_{GS(th)}$) reading.

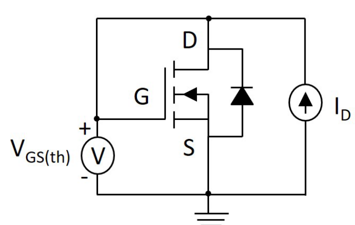


Figure 7. Circuit Diagram to Measure Gate-Source Threshold Voltage

Drain-source leakage current (I_{DSS}) value indicates the drain current measured at a given drain-source voltage and with the gate to source connected, as illustrated in **Figure 8**. The datasheets specify the value at 25°C and higher virtual junction temperature.

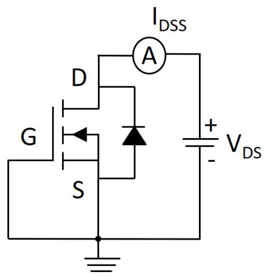


Figure 8. Circuit Diagram to Measure MOSFET's Leakage Current

Gate leakage current (I_{GSS}) refers to the small amount of current that flows between the gate and source when the MOSFET is in an off state. **Figure 9** demonstrates the circuit used to measure the gate leakage current. Initially, the drain-to-source terminal is connected, and then a maximum allowable voltage is applied across the gate and source terminals to monitor the leakage current.

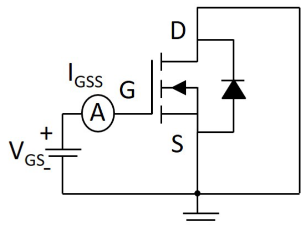


Figure 9. Circuit Diagram to Measure Gate Leakage Current

Drain-source on-state resistance ($R_{DS(on)}$) describes the resistance across the drain and source when the MOSFET is in the on-state. **Figure 10** presents the circuit diagram for measuring the drain-source on-state resistance ($R_{DS(on)}$). Initially, the gate-source voltage (V_{GS}) is set to a defined value, and then the voltage drop across the drain-source voltage $V_{DS(on)}$ is measured, using a given current source (I_D). $R_{DS(on)}$ is calculated using the **Equation 4**:

$$R_{DS(on)} = \frac{V_{DS(on)}}{I_D} \quad (4)$$

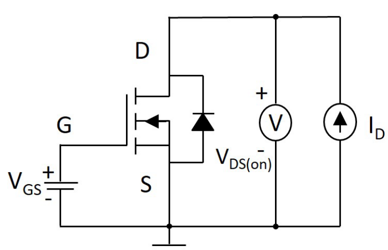


Figure 10. Circuit Diagram to Measure Gate Drain-Source On-State Resistance

3.3. Dynamic Characteristics

This section of the datasheet provides information on the behavior of the device in dynamic conditions, as shown in **Table 4**. The intrinsic capacitances, gate charge and switching behavior of the MOSFET are pivotal factors influencing the dynamic performance of the device.

Table 4. Dynamic Electrical Characteristics

Symbol	Characteristic	Conditions		Value			Unit
				Min.	Typ.	Max.	
$R_{g(int)}$	Internal gate resistance	f = 1 MHz, open drain		–	6	–	Ω
C_{iss}	Input capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	6100	–	pF
C_{oss}	Output capacitance			–	865	–	
C_{rss}	Reverse transfer capacitance			–	1.8	–	
$C_{oss(er)\ eff.}$	Effective output capacitance, energy related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V		–	510	–	pF
$C_{oss(tr)\ eff.}$	Effective output capacitance, time related	V_{DS} = 0...0.8 · V_{DSS}, V_{GS} = 0 V, I_D = constant		–	2000	–	pF
Q_G	Gate charge	V_{DD} = 0.5 · V_{DSS}, V_{GS} = 10 V, I_D = 0.5 · I_D		–	108	–	nC
Q_{GS}	Gate-source charge			–	27	–	
Q_{GD}	Gate-drain charge			–	27	–	
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 0.5 · I_D		72	120	–	S
$t_{d(on)}$	Turn-on delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	13	–	ns
t_r	Rise time		T_{vj} = 25 °C	–	24	–	
t_{on}	Turn-on time		T_{vj} = 25 °C	–	37	–	
$t_{d(off)}$	Turn-off delay time	Resistive load, V_{DD} = 100 V, V_{GS} = 10 V, I_D = 0.5 · I_D, $R_{g(ext)}$ = 2 Ω	T_{vj} = 25 °C	–	100	–	ns
t_f	Fall time		T_{vj} = 25 °C	–	12	–	
t_{off}	Turn-off time		T_{vj} = 25 °C	–	112	–	

Internal gate resistance ($R_{g(int)}$) signifies the resistance that exists within the device gate structure. The internal gate resistance mentioned in **Figure 11**, constitutes a component of the parasitic elements within the MOSFET. Together with the MOSFET's input capacitance, the gate resistance forms an RC network that determines the voltage change at the MOSFET gate and thus the switching time.

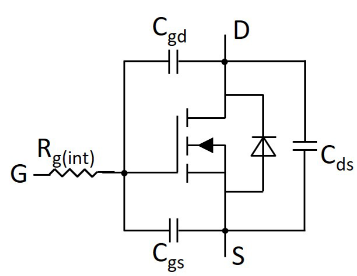


Figure 11. Power MOSFET Parasitic Components

Capacitance Characteristics play a crucial role in switching characteristics of the MOSFET.

- **Input capacitance (C_{iss})** encompasses both gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs}, representing the total capacitance measured between the gate and source terminals with the drain connected to the source terminal.

$$C_{iss} = C_{gs} + C_{gd} \quad (5)$$

- **Output capacitances (C_{oss})** consists of the drain-to-source capacitance C_{ds} and gate to drain capacitance C_{gd}, indicating the output capacitance which is measured between the drain and source with the gate connected to the source terminal.

$$C_{oss} = C_{ds} + C_{gd} \quad (6)$$

- **Reverse transfer capacitance (C_{rss})** primarily arises from C_{gd}, delineating the capacitance between the gate and drain with the source terminal connected to ground.

$$C_{rss} = C_{gd} \quad (7)$$

Effective output capacitance of the MOSFET includes both energy related and time related parameters, denoted as $C_{oss(er)}$ and $C_{oss\ (tr)}$ respectively. $C_{oss(er)}$ represents a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to specified voltage. Conversely, $C_{oss(tr)}$ signifies a fixed capacitance that gives the same charging time as a C_{oss} while V_{DS} is rising from 0 V to specified voltage and at a constant drain current I_D.

Total gate charge (Q_G) is the total amount of charge that is required during the MOSFET's turn-on and turn-off transition. The switching speed depends on the speed at which a gate driver can charge or discharge the input gate charge. **Figure 12** presents a typical gate charge waveform for a power MOSFET in a resistive-load circuit. The fundamental equation for calculating the gate charge is formulated in **Equation 8**.

$$Q_G = \int_{t_0}^{t_4} i_{GG}(t)dt \quad (8)$$

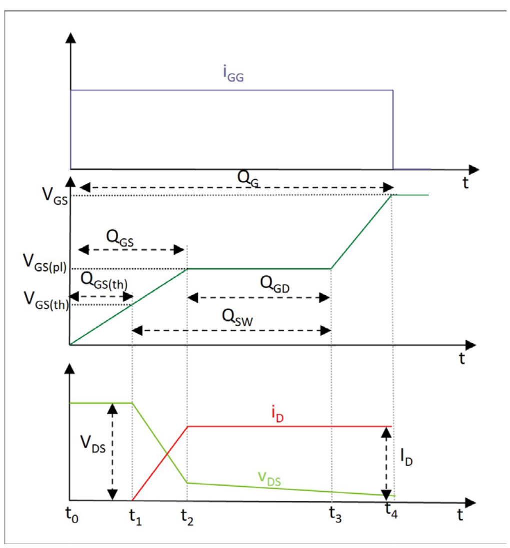


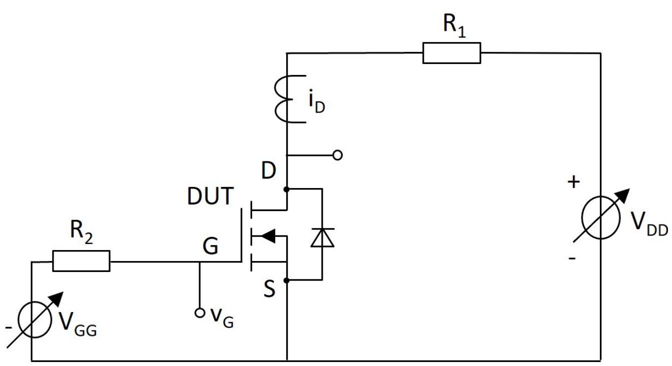
Figure 12. Gate Charge Waveform of Power MOSFET during Turn-on Transition with Resistive Load

As depicted in the gate charge waveform, the total gate charge encloses the **Gate-Source Charge (Q_{GS})**, the **Gate-Drain Charge (Q_{GD})**, and the **Gate Switch charge (Q_{SW})**. Q_{GS} represents the amount of charge that is required to charge the gate-source capacitance (C_{gs}) from its initial voltage to the miller plateau level. Q_{GD} quantifies the charge that is needed to fully charge the gate-drain capacitance (C_{gd}) during switching, ensuring full channel enhancement and sustaining the MOSFET in its conducting state. Lastly, Q_{SW} encapsulates charge stored in the gate capacitance from when the gate-source voltage has reached the gate-source threshold voltage, $V_{GS(th)}$ until the end of the miller plateau.

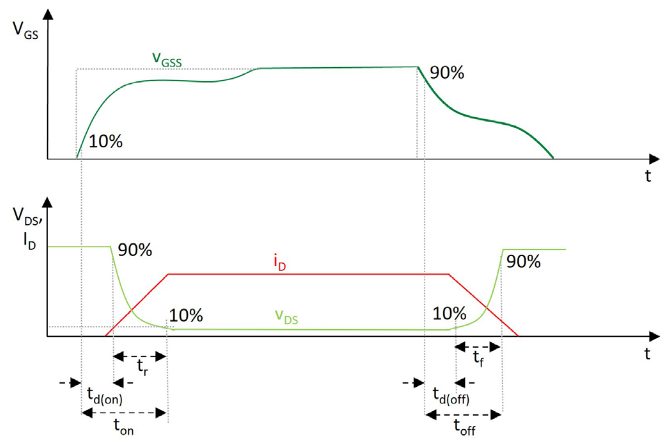
Transconductance (g_{fs}) is described as the change in drain current divided by the change in gate voltage for a constant drain voltage. A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. The transconductance is mathematically expressed as:

$$g_{fs} = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS} = constant} \tag{9}$$

MOSFETs, due their physical structure, can change their state from on to off much faster than IGBTs. The correlations of switching time measurement circuit and the switching time definitions are demonstrated **Figure 13**.



(a) Switching Time Measurement Circuit Diagram



(b) Switching Time Definition Waveform

Figure 13. Correlation of Switching Time Measurement Circuit and Switching Time Definition

- **Turn-on delay time ($t_{d(on)}$)** is the time interval when the gate-source voltage (V_{GS}) has reached 10% of its end value, to the time when the drain-source voltage (V_{DS}) has dropped to 90% of its initial value or rated value.
- **Rise time (t_r)** specifies the time interval between the drain-source voltage dropping from 90% to 10% of its initial value. The drain current starts to rise, and a major part of turn-on losses is generated during this period.
- **Turn-off delay time ($t_{d(off)}$)** denotes the time interval between the moment when the gate-source voltage (V_{GS}) has declined to 90% of its initial value and the drain-source voltage has risen to 10% of the supply voltage.
- **Fall time (t_f)** implies the time interval between the drain-source voltage rise from 10% to 90% of its end value. During this period, the drain current starts to fall, and a major part of turn-off losses is generated during this time.

3.4. Electrical Characteristics – Body Diode

Power MOSFET generally contain a body diode, which provides freewheeling operation in the inductive load switching. Hence, the MOSFET datasheet from Littelfuse also contains the electrical parameters and graphs related to the body diode. **Table 5** shows the electrical characteristics listed in IXTH120N20X4 datasheet.

Table 5. Electrical Characteristics – Body Diode

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{SD}	Diode forward voltage	V_{GS} = 0 V, I_S = 100 A [1]	–	–	1.4	V
t_{rr}	Diode reverse recovery time	V_{DD} = 100 V, I_S = 60 A, $-di_S/dt$ = 200 A/μs	–	190	–	ns
Q_{rr}	Reverse recovery charge		–	3.2	–	μC
I_{rrm}	Peak reverse recovery current		–	33.7	–	A

Note 1: Pulse test, t ≤ 300 μs, duty cycle, d ≤ 2%

Diode forward voltage (V_{SD}), measured under specified conditions including a given forward current (I_S), zero gate-source voltage (V_{GS}), and a virtual junction temperature of 25°C, symbolizes the maximum forward voltage drop across the intrinsic diode, as illustrated in **Figure 14**.

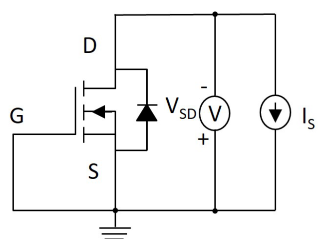
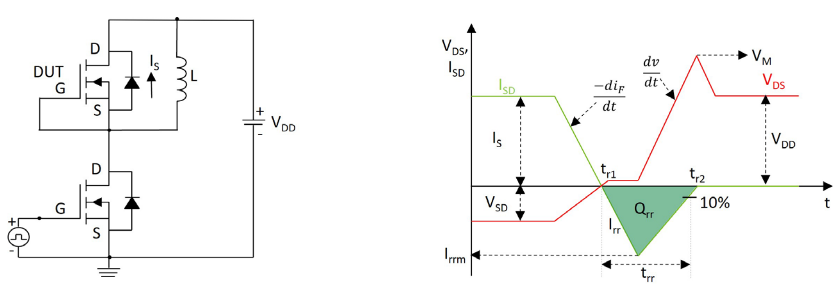


Figure 14. Circuit Diagram to Measure Diode Forward Voltage

Reverse recovery charge (Q_{rr}) characterizes the charge that is built up in the diode during the transition from the conducting or forward bias state to the non-conducting or reverse-biased state. The time that is necessary to remove the charge that persists within the diode during the reverse recovery phase is called **Diode Reverse Recovery Time (t_{rr})**. **Peak Reverse Recovery Current (I_{rrm})** denotes the maximum current flowing in the reverse direction during this period.

The circuit diagram and reverse recovery measurement waveforms are demonstrated in **Figure 15**. Mathematically, the reverse recovered charge, Q_{rr}, is defined as the integral of the reverse recovery current, I_{rr}, during the process of current commutation, with time as the variable. This relationship is expressed by **Equation 10**. The reverse recovery time, t_{rr}, is measured from the point of reverse bias initiation to the moment when the reverse current reaches 10% of its peak value.

$$Q_{rr} = \int_{t_{r1}}^{t_{r2}} I_{rr}(t)dt \quad (10)$$



(a) Measurement Circuit

(b) Waveform

Figure 15. Diode Reverse Recovery

3.5. Thermal Characteristics – Thermal Resistance (R_{th})

R_{th} signifies the thermal characteristics of the MOSFET at steady state, making it an essential parameter for thermal management of the MOSFET. **Table 6** outlines the R_{th} values presented in the datasheet. The heat generated within the silicon chip needs to be dissipated by means of heat sink into the ambient. The thermal dissipation pathway for a power MOSFET in a conventional and isolated discrete package with a heat sink is visually outlined in **Figure 16 (a) and (b)**.

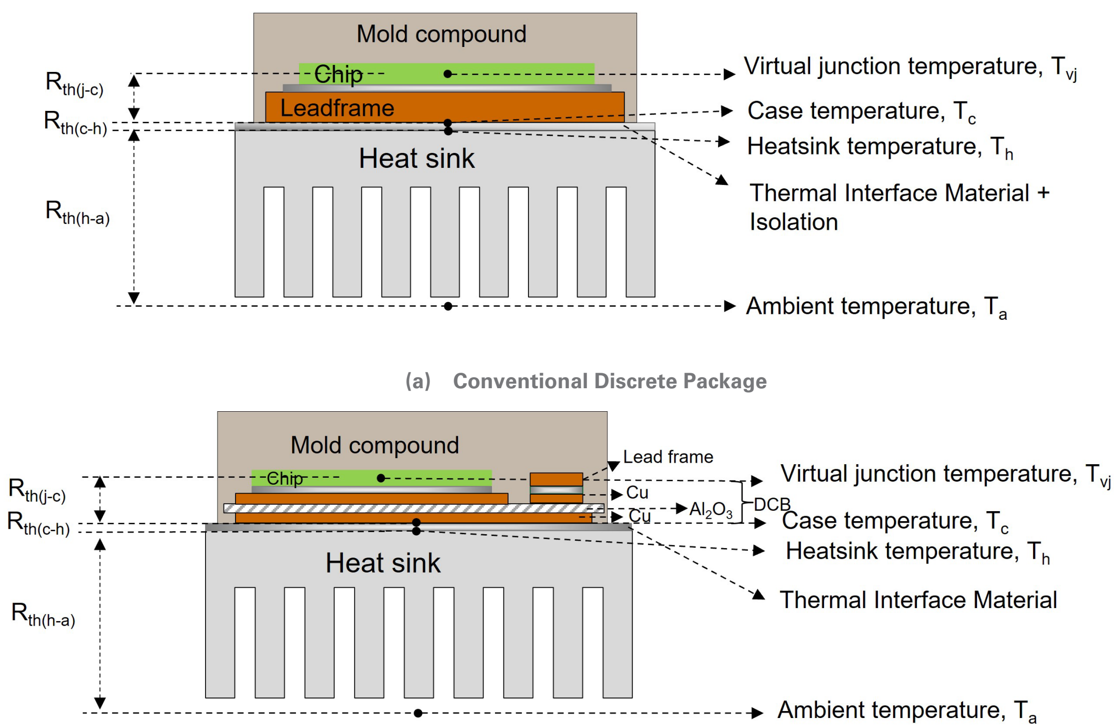
Table 6. Thermal Characteristics

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance junction to case – MOSFET	–	–	–	0.36	K/W
$R_{th(c-h)}$	Thermal resistance case to heat sink – MOSFET	–	–	0.21	–	K/W

Thermal resistance junction to case ($R_{th(j-c)}$) is the thermal resistance from the junction of the die to the outside of the device's case. It describes the passage of heat between the semiconductor chip and the case. Littelfuse specifies a maximum static $R_{th(j-c)}$ at T_{vj} = 125°C.

Thermal resistance case to heatsink ($R_{th(c-h)}$) characterizes the static heat dissipation of a MOSFET and depends on module size, heatsink, case surfaces, thickness parameters of thermal layers between module and heatsink.

Thermal resistance junction to ambient ($R_{th(j-a)}$) is equal to sum of junction to case, $R_{th(j-c)}$, case to heatsink $R_{th(c-h)}$ and heatsink to ambient thermal resistance, $R_{th(h-a)}$. The $R_{th(j-c)}$ is specified in the datasheet whereas $R_{th(c-h)}$ and $R_{th(c-a)}$ is determined by the user's board design and depends on the application.



(a) Conventional Discrete Package

(b) Isolated Discrete Package

Figure 16. Lateral Thermal Resistance Chain within a Semiconductor Package

3.6. Package – Mechanical Rating

This part of the datasheet covers physical characteristics of the device.

Package weight (G) refers to the mass of the package or housing, including the MOSFET die and the required electrical and thermal connections.

Isolation voltage (V_{isol}) is specified only for isolated devices and represents the isolation voltage between all terminals connected against the cooling surface or base plate. The verification test circuit used to determine the isolation voltage rating between terminals and baseplate is visualized in **Figure 17**.

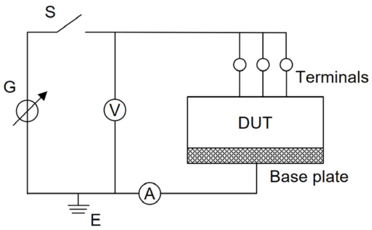


Figure 17. Circuit Diagram for Isolation Withstand Voltage Test

3.7. Characteristics Curves

The essential curve in the datasheet provides graphical portrayal of key performance characteristics of MOSFET devices. In this application note, the graphs, and parameters from the IXTH120N20X4 datasheet are used as reference.

Typical Output Characteristics of IXTH120N20X4, illustrating various modes of operation, are delineated in **Figure 18**. In the Cut-off region, the gate-source voltage (V_{GS}) is less than the gate-threshold voltage ($V_{GS(th)}$) and the device is an open circuit or off. In the *Ohmic region*, the device acts as a resistor with an almost constant on-resistance $R_{DS(on)}$ and which is equal to V_{DS} /I_D. In the linear-mode of operation, the device operates in the *Current-Saturated* region where the drain current (I_D) is a function of the gate-source voltage (V_{GS}) and defined by the **Equation 11**:

$$I_D = K \cdot \left(V_{GS} - V_{GS(th)}\right)^2 = g_{fs} \cdot \left(V_{GS} - V_{GS(th)}\right) \quad (11)$$

In this equation, K is a parameter depending on temperature and device geometry and g_{fs} is the current gain or transconductance. When the drain-source voltage (V_{DS}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. This reduction in surface potential continues as V_{DS} increases until it reaches a critical point, known as the *Channel Pinch-off Voltage*, where the drain voltage equals $\left(V_{GS} - V_{GS(th)}\right)$. At this point, the drain current becomes saturated.

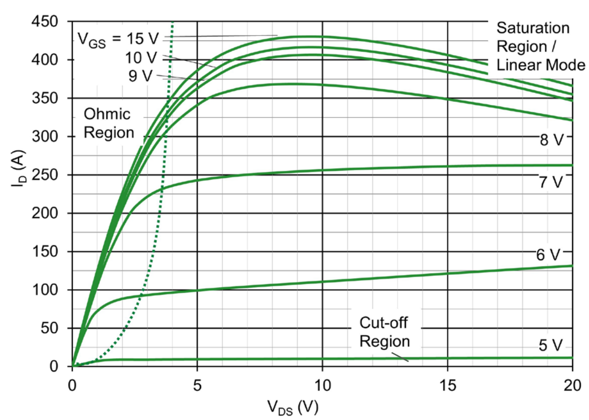


Figure 18. Typical Output Characteristics

Typical Transfer Characteristics depicted in **Figure 19**, illustrates the relationship between drain current and gate voltage across varying temperatures of –40, 25, and 150°C. The intercepts of these lines at I_D = 0 A provides the threshold voltages for the respective temperature. It can be concluded that the transfer characteristic depends on both temperature and drain current and the threshold voltage decreases with increasing temperature.

In certain scenarios, a cross-over point or zero temperature coefficient point may be present. Below this point, the gate-source voltage exhibits a negative temperature coefficient, implying a decrease in gate-source voltage at higher temperatures for a given drain current. Conversely, above this point, the temperature coefficient for the gate-source voltage becomes positive.

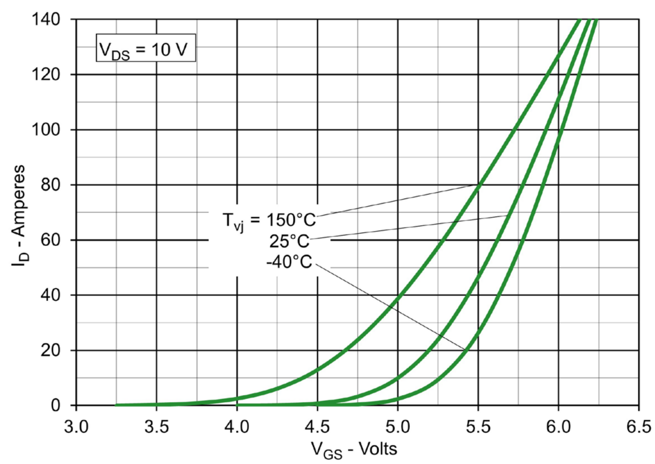


Figure 19. Typical Transfer Characteristics

Typical Drain-Source On-State Resistance (Normalized) vs. Virtual Junction Temperature - The value of $R_{DS(on)}$ is critical in power MOSFETS as it serves as an indicator of the device's capacity to handle current. An important characteristic is an increase in the on-resistance with increasing temperature, as evidenced in **Figure 20**, which portrays a positive temperature coefficient. The positive temperature coefficient of $R_{DS(on)}$ is a beneficial feature when paralleling power MOSFETs because it ensures thermal stability and balanced current sharing.

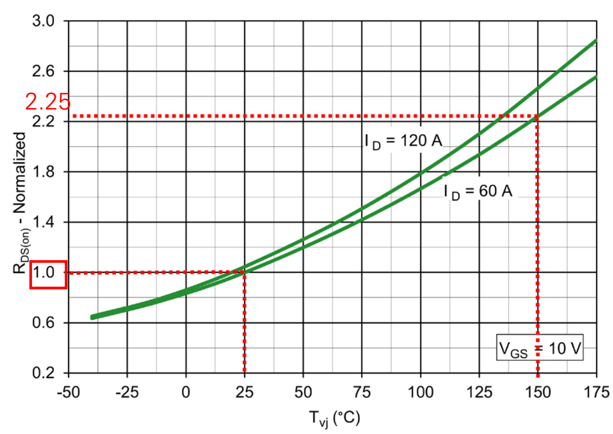


Figure 20. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Virtual junction temperature

From **Figure 20**, $R_{DS(on)}$ vs. T_{vj} (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at T_{vj} = 25°C, and it increases to 2.25 at T_{vj} = 150°C. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., $0.5 \cdot I_{D25}$) is specified as 9.5 mΩ at T_{vj} = 25°C, then it is predicted that it will change to 21.375 mΩ when Tvj = 150°C is applied. The normalized value is obtained from $R_{DS(on)}|T_{vj}$ / $R_{DS(on)}|T_{vj}$ = 25°C.

Typical Drain-Source On-State Resistance (Normalized) vs. Drain Current presented in **Figure 21** provides information about the relative change in on-state resistance at different drain currents. The calculation of the on-state resistance, $R_{DS(on)}$ as a function of drain current I_D and gate-source voltage V_{GS} can be derived from the typical output characteristic diagram depicted in **Figure 18,** employing Ohm's Law.

$$R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D} \tag{12}$$

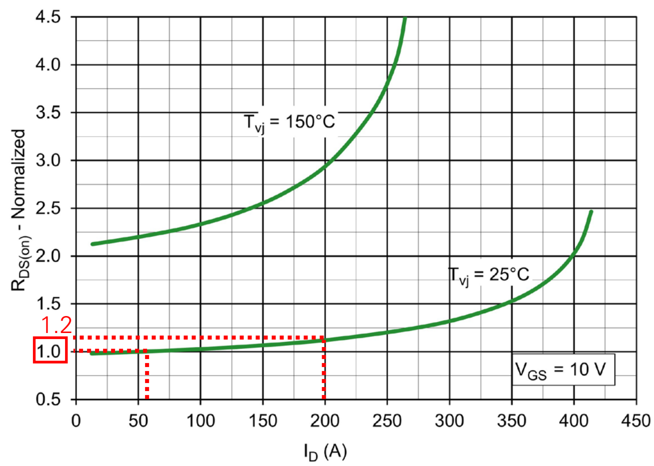


Figure 21. Typical Drain-source On-State Resistance (Normalized to I_D = 60 A) vs. Drain Current

From **Figure 21**, $R_{DS(on)}$ vs. I_D (normalized to I_D = 60 A), it is found that $R_{DS(on)}$ is 1 at I_D = 60 A, and it changes to 1.2 at I_D = 200 A. In the IXTH120N20X4 datasheet, if the resistance $R_{DS(on)}$ at I_D = 60 A (i.e., $0.5 \cdot I_{D25}$) is specified as 9.5 mΩ, then it is predicted that the resistance $R_{DS(on)}$ will change to 11.4 mΩ when I_D = 200 A is applied. The normalized value is obtained from $R_{DS(on)}|I_D$ / $R_{DS(on)}|I_D$ = 60 A.

Typical Breakdown Voltage and Gate Threshold Voltage (Normalized) vs. Virtual Junction Temperature - The relationship between $V_{(BR)DSS}$ / $V_{GS(th)}$ and T_{vj} is expressed in **Figure 22**. The breakdown-voltage $V_{(BR)DSS}$ features a positive temperature coefficient, whereas gate-source threshold voltage $V_{GS(th)}$ has a negative temperature coefficient. At 25°C, the normalized breakdown-voltage $V_{(BR)DSS}$ is 1, growing to value of 1.14 at 150°C. This signs that breakdown-voltage $V_{(BR)DSS}$ at T_{vj} = 25°C is 200 V and is expected to be 228 V at T_{vj} = 150°C. The value of gate-source threshold voltage $V_{GS(th)}$ is 1 at 25°C and 0.643 at 150°C, respectively. Assuming the device's gate-source threshold voltage $V_{GS(th)}$ is 3.5 V, then the $V_{GS(th)}$ remains at 3.5 V at T_{vj} = 25°C, but is anticipated to decrease to 2.24 V at T_{vj} = 150°C.

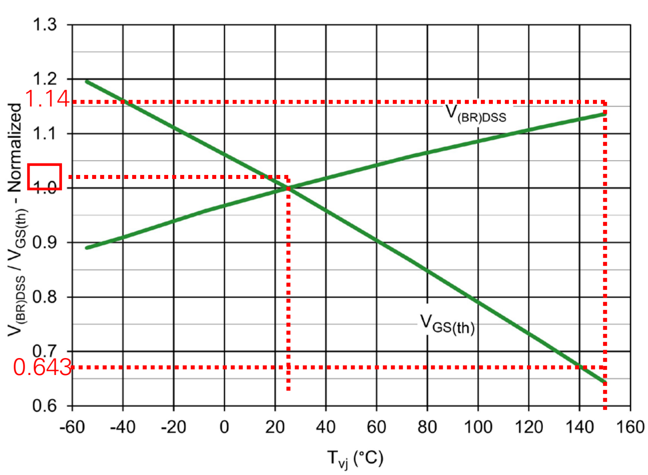


Figure 22. Typical $V_{(BR)DSS}$/$V_{GS(th)}$ (Normalized) vs. Virtual Junction Temperature

Drain Current vs. Case temperature curve illustrated **Figure 23** depicts the solution of **Equation 2** across different case temperatures, demonstrating that at low case-temperature T_c, the maximum drain current I_D remains constant, while at high case-temperature T_c, it gradually decreases until reaching zero at $T_c = T_{vj(max)}$. However, the actual drain current is restricted by additional factors, including bond wire diameter, chip design, and assembly. It is noteworthy that, in certain instances, the continuous current is constrained by the package leads, although the switched current could potentially be higher.

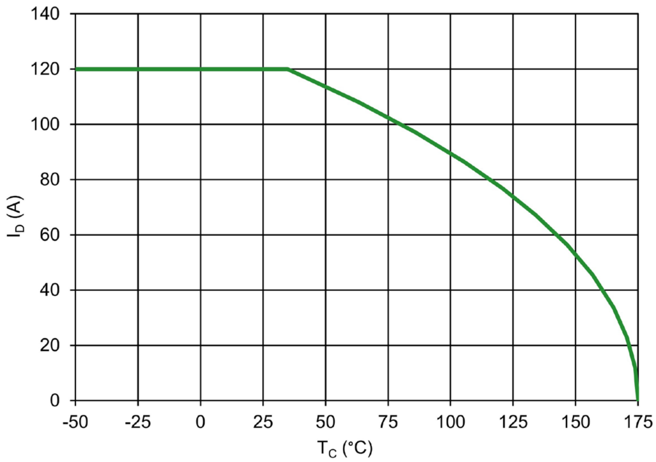


Figure 23. Drain Current vs. Case Temperature

Typical Transconductance - A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. **Figure 24** displays a typical variation of the transconductance with respect to drain current. The reduction in the mobility with increasing temperature adversely affects the transconductance.

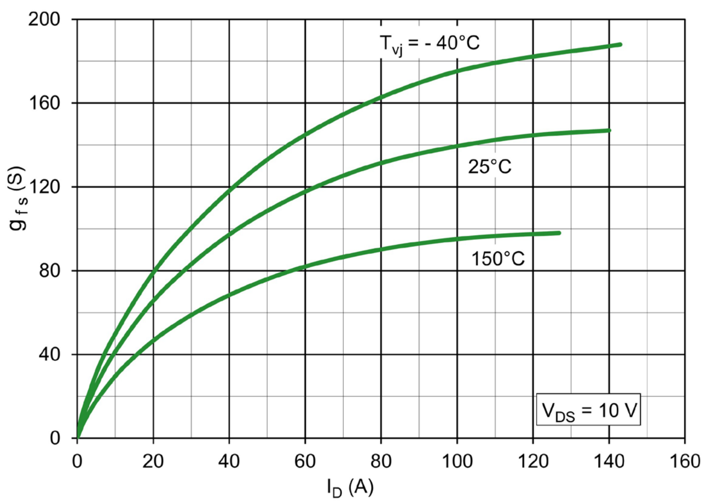


Figure 24. Typical Transconductance Curve

Typical Gate Charge curve depicts the typical variation of the requisite gate charge to switch on the device at a specified V_{GS} and V_{DD}. A typical gate charge waveform for a power MOSFET can be observed in **Figure 25**. The gate charge reflects the charge stored on the inter-terminal capacitances and is used in designing the gate drive circuit.

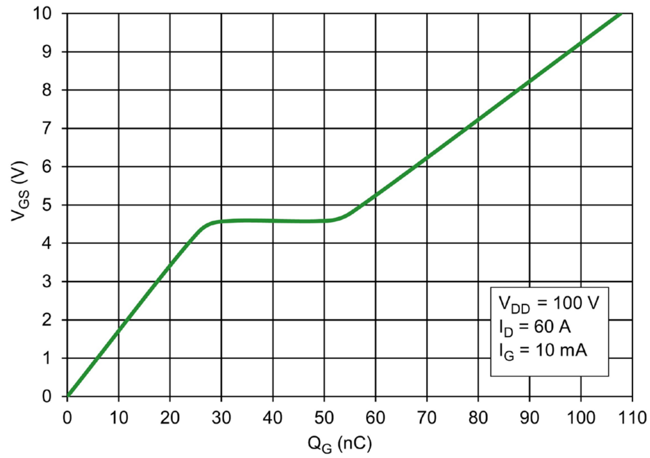


Figure 25. Typical Gate Charge Characteristics

In **Figure 26**, the parasitic **Junction Capacitances Characteristics** are represented as a function of drain-source voltage. Its components include input capacitance (C_{iss}), which consists of gate-source capacitance C_{GS} in parallel with drain-gate capacitance C_{DG}, output capacitance (C_{oss}), which consists of drain-gate capacitance C_{DG} in parallel with drain-source capacitance C_{DS} and reverse transfer capacitance (C_{rss}), which is the drain-gate capacitance C_{DG}.

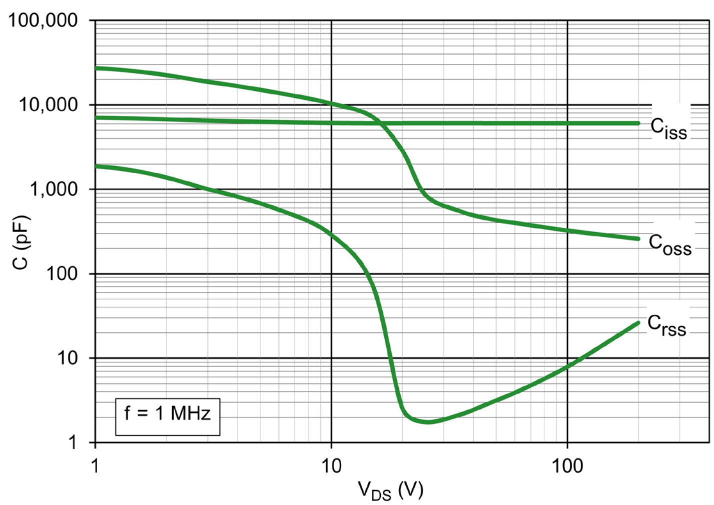


Figure 26. Typical Junction Capacitance

Forward-Bias Safe Operating Area (FBSOA) is a datasheet figure of merit that defines the maximum allowed operating points. **Figure 27** shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bound by the maximum drain-to-source voltage V_{DSS}, maximum conduction current I_{DM}, maximum drain-source on-state resistance and constant power dissipation lines for various pulse durations.

In **Figure 27**, there is a series of curves that include a DC line along with four single pulse operating lines, 10 ms, 1 ms, and 100 µs. The top of each line is limited by the maximum drain current and is bounded by a positive sloped line defined by the on-state resistance $R_{DS(on)}$ of the device. The right-hand side of each line is terminated at the rated drain-source voltage limit V_{DSS}. Each line has a negative slope and is determined by the maximum power dissipation P_{tot} of the device:

$$P_{tot} = \frac{[T_{vj,max} - T_c]}{Z_{th(j-c)}} = V_{DS} \cdot I_D \quad (13)$$

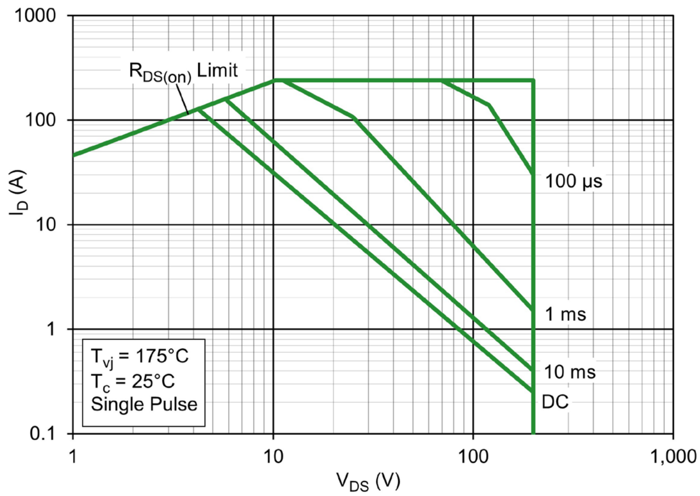


Figure 27. Forward Biased Safe Operating Area (FBSOA) Curve

These theoretical constant power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFET. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, as a result of lateral heat flow. Secondly, material imperfections like die attach voids and thermal grease cavities may cause local decrease of thermal conductivity. Additionally, fluctuations in dopant concentrations, gate oxide thickness and fixed charge will cause fluctuations of the local threshold voltage and the current gain (g_{fs}) of individual MOSFE's cells, which will also affect the local temperatures of the die.

Die temperature variations are mostly harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than the time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications are known to have limited capability to operate in the right-side bottom corner of the FBSOA graph.

Typical Forward Characteristics of a Reverse Diode plotted against various temperatures are presented in **Figure 28**. This curve aids in comprehending the diode's conduction behavior and its forward voltage drop characteristics. It clearly demonstrates the negative temperature coefficient of diode forward voltage V_{SD} in the low-current region. As a result, it is anticipated that the diode forward voltage will decrease as the temperature increases. In the high-current region that is above the cross-over point (Q), the diode forward voltage will increase as the temperature increases.

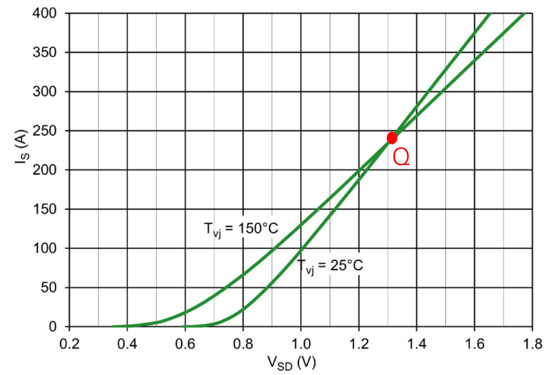


Figure 28. Typical Forward Characteristics of a Reverse Diode

Typical E_{oss} vs. Drain-Source Voltage - E_{oss} refers to the output switching energy. Specifically, it represents the energy that is required to charge or discharge output capacitance of a MOSFET during the switching operation.

$$Q_{oss} = \int_{0}^{V_{DS}} C(v)\ dv \qquad (14)$$

$$E_{oss} = Q_{oss} \cdot V_{DS} \qquad (15)$$

Where in this equation, Q_{oss} is the amount of charge required for charging the drain-source capacitance and C(v) is a function of the output capacitance C_{oss} that is dependent on drain to source voltage V_{DS} as shown in **Figure 29**.

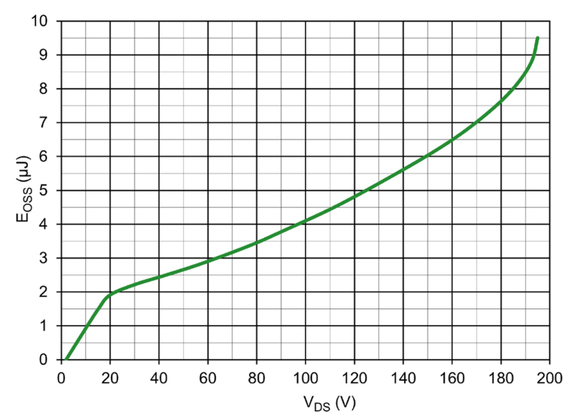


Figure 29. Typical E_{oss} vs. Drain-Source Voltage

Typical Transient Thermal Impedance - A Power MOSFET has a virtual junction temperature, T_{vj} limitation. It should be operated below the maximum virtual junction temperature, $T_{vj(max)}$ specified in the datasheet to ensure reliability. The heat generated within the silicon chip needs to be dissipated by means of a heat sink into the ambient environment. The virtual junction temperature's rise above the ambient temperature T_a and is directly proportional to this heat flow and the junction-to-ambient thermal resistance, $R_{th(j\text{-}a)}$. The steady-state virtual junction temperature can be calculated by:

$$T_{vj} = P_{tot} \cdot R_{th(j-a)} + T_a|_{T_{vj} \leq T_{vj(max)}} \quad (16)$$

Here, P_{tot} is the maximum power dissipated in the junction. The total thermal resistance between junction and ambient is,

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad (17)$$

The steady-state thermal resistance is not sufficient when calculating the peak virtual junction temperatures for pulsed applications. When a power pulse is applied to the device, the peak virtual junction temperature varies depending on peak power and pulse width. The temperature swing due to short pulses of power can be calculated using the thermal impedance Z_{th}.

$$Z_{th(j-c)}(t) = r(t) \cdot R_{th(j-c)} \quad (18)$$

Here, r(t) is a time dependent factor that is defined by the thermal capacity of the device. For short pulses, the r(t)-value is small but for long pulse, it approaches 1, which means that the thermal impedance approaches the steady-state thermal resistance. A typical thermal impedance curve is shown in **Figure 30**, approaching the steady-state value for pulses exceeding a duration of about one second. The thermal impedance can be used to estimate the peak temperature rise for square wave power pulses, which is typical in power supply design circuits.

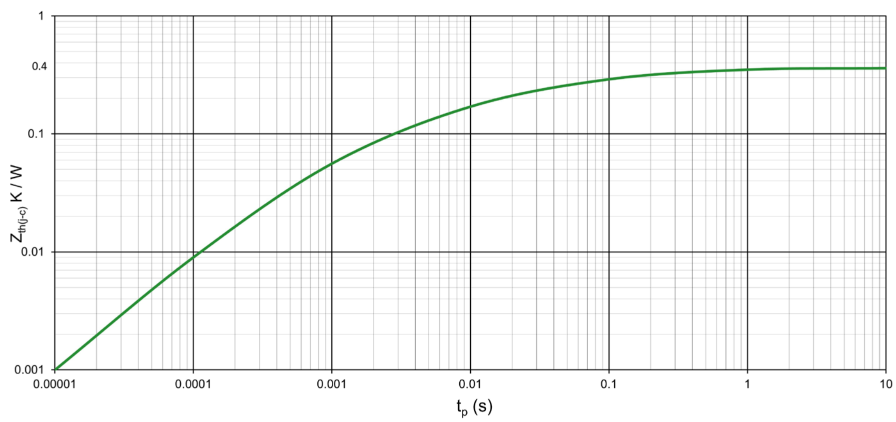


Figure 30. Typical Thermal Impedance

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