SMPD 封装的安装和散热解决方案

目标

本应用指南讨论了表面贴装功率器件（SMPD）封装的各种安装解决方案。安装说明分别针对单个器件和多个器件提供。公差图解释了围绕SMPD进行设计时的重要细节。通过一个简单的实验，简要说明了在给定设计下确定热阻的步骤。

应用

- 电机驱动
- 光伏逆变器
- UPS系统
- 直流–直流转换器

目标受众

本文件适用于SMPD封装功率半导体器件的潜在用户，他们需要熟悉合适的安装和散热解决方案，以确保器件正确的安装和散热。

联系方式

有关安装SMPD类型器件的更多信息，请联系Littelfuse Power Semiconductor产品和应用专家团队：

- 北美洲 – NA_PowerSemi_Tech@Littelfuse.com
- 中南美洲– CSA_PowerSemi_Tech@Littelfuse.com
- 欧洲，中东和非洲– EMEA_PowerSemi_Tech@Littelfuse.com
- 亚洲、澳大利亚和太平洋岛屿 – APAC_PowerSemi_Tech@Littelfuse.com

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1. 介绍

表面贴装功率器件（SMPD）封装是IXYS（Littelfuse 公司）于2013年1月推出的创新解决方案。SMPD扩展了IXYS功率半导体器件的ISOPLUS™封装系列。它的特点是直接铜邦定（DCB）基板，带有铜引线框架、铝邦定线和塑封材料。DCB基板是电绝缘，并允许一个基板上的多个半导体芯片形成不同的电路拓扑。将铜引线框架与铝邦定线相结合，形成了一种表面安装型器件，简化了焊接和组装。塑封提供良好的密封和半导体保护。DCB基板的背面裸铜设计，使得半导体器件和散热器可以大面积连接。图1显示了一个SMPD封装示意图。

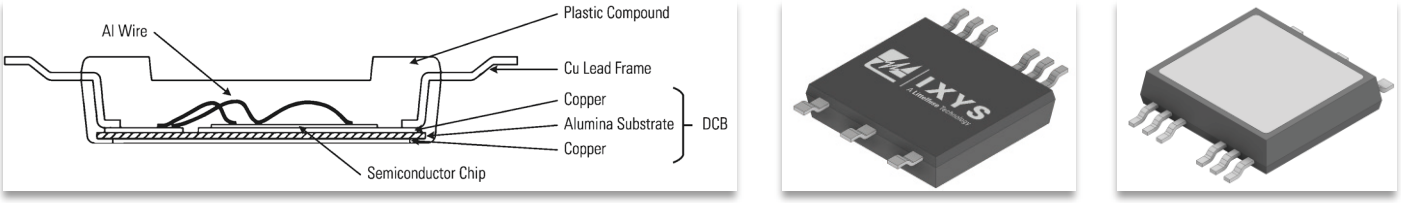


图1. 封装示意图

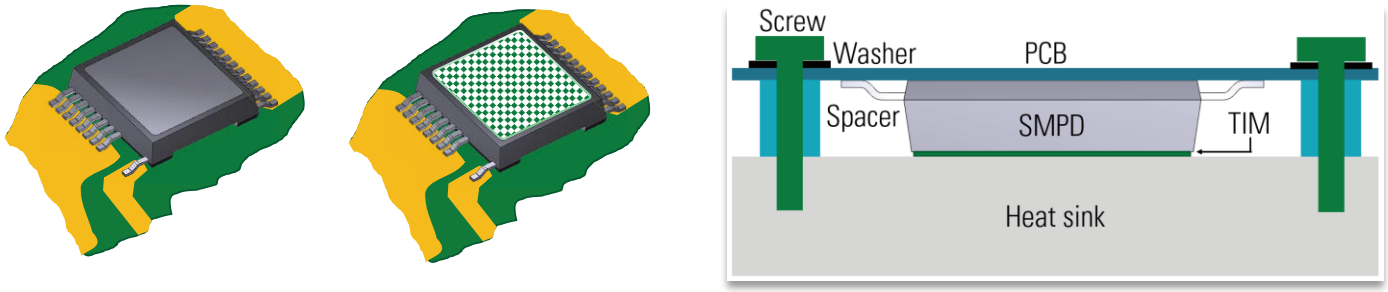
SMPD封装为电力电子应用提供了如下独特的性能：

- 2500 V的高电压绝缘强度
- 与TO-247或TO-264等标准封装相比，热阻更低
- 增强了定制拓扑的灵活性
- 与TO型封装相比，具有更高的载流能力
- 内部结构旨在减少寄生电感和寄生电容等寄生效应，从而提高EMI性能

所有这些优点使SMPD成为硅和碳化硅功率半导体的优选封装。

2. 推荐的PCB和散热器安装

SMPD是一种表面贴片封装 。这些器件采用最先进的工艺焊接到PCB上，需要一层热界面材料(TIM)来确保从器件到散热器的高导热率。在焊接和使用TIM完成后，可以通过安装螺钉将组件安装到散热器上。图2显示了一个散热器组件的示例。



(a) SMPD-X焊接至PCB上　(b) 热界面材料的使用　(c) 使用螺钉和垫片将器件翻转安装到散热器上

图2. 将SMPD安装到散热器上的顺序

2.1. 焊接说明

作为SMD器件，所有SMPD封装都可以用三种不同的方法进行焊接:

- 使用260-287℃的烙铁进行选择性焊接--注意确保烙铁的加热功率和热容量与元件的尺寸相适应，对管脚加热不超过10秒。
- 使用符合IEN61760-1的温度曲线进行波峰焊——防止DCB区域粘连焊料。卡普顿式胶带可以用来防止污染。
- 使用IPG/JEDEC J-STD-020E中所述的温度曲线进行回流焊

Littelfuse强烈建议使用符合RoHS和REACH标准的无铅焊料。

2.2. 布局建议

SMPD-B封装可以支持多种拓扑，包括单管和多管器件， 以及升压或半桥等更复杂的拓扑。 例如，图3显示了集成1200V IGBT半桥的SMPD-B。SMPD-B封装设计用于工作电压高达630V rms的应用。

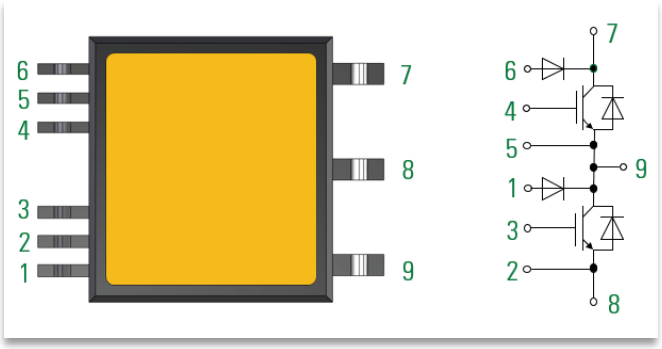
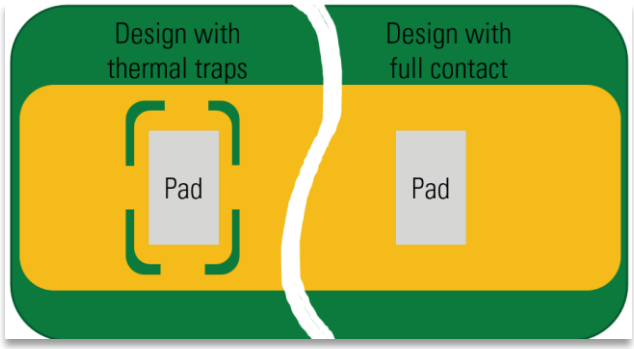


图3. SMPD-B封装外形和拓扑结构，IXA40PG1200HGLB



(a) 装有thermal traps (b) 完全接触

图4. 焊接区域

使用圆角形状作为焊盘被认为是一种良好的做法，由于SMPD-B封装用于高压应用，圆角有助于降低矩形角上的电场应力，高压焊盘是引脚7、8和9，建议拐角半径为0.6毫米或25密耳，对于PCB走线的角度和多边形铜箔，建议采用相同的做法。

一种常见的方法是在较大的铜区域应用thermal traps，以改进焊接工艺。如图4所示，这些thermal traps可防止焊接产生的热量逸出到更大的铜区域，从而有助于防止形成冷焊点。但是可用于承载电流的横截面会减小。

需要注意的是，thermal traps 的设计要适中， 以便有效地阻挡焊接过程中产生地热量， 同时以保持足够的横截面来通过电流。

SMPD的内部结构设计也是为了将热量传递到引脚，以增强散热效果。引脚处的thermal traps可能会阻止热量正常散发；因此，最好采用全接触面积的设计。

2.3. 绝缘管理

设计PCB布局时需要考虑两个主要参数：

- 电气间隙 —— 两点之间最短的距离
- 爬电距离 —— 沿着固体材料表面上从一点到另外一点不间断的最短路径

在高电压环境中，必须防止不同电压级别之间的电弧放电。电弧发生在电气间隙距离上，因此最终系统中的预期电压水平决定了焊盘和走线之间的距离，以及带电体和散热器或其它接地器件之间的距离。即使两点之间的间隙选择得足够大，绝缘强度也会在较长的时间内被导电颗粒降低。这取决于污染程度，这与该器件使用的环境条件有关。

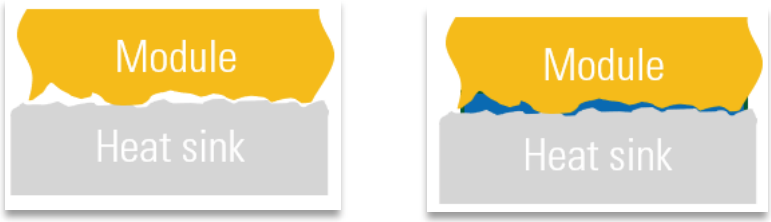
IEC60664–1深入探讨了在目标设计中确定爬电距离和电气间隙时需要考虑的相关条件。

2.4. 热界面材料的使用

为了获得合适的散热器接触表面，必须使用热界面材料(TIM)，它降低了壳体与散热器之间的热阻R_{thch}。热界面材料有热垫和热脂/化合物两种。与不绝缘的分立封装不同，SMPD封装采用DCB结构，该结构使用一层陶瓷作为电气绝缘。该封装具有高达2500 V的绝缘电压，可选择使用非绝缘型的热界面材料，不建议使用绝缘型的热界面的材料，例如用于分立封装器件的硅胶垫。与热脂/化合物或导电热垫相比，这些材料本质上表现出更高的热阻。

热界面材料应均匀地涂在器件基板或散热器表面。理想情况下，使用丝网印刷可实现准确和可复制的结果。

由于不需要与TIM层进行电气绝缘，因此建议使用非常薄的TIM层，以便材料刚好填充器件铜垫和散热器之间的间隙和空隙，如图5所示。



(a) 没有TIM，空气间隙仍然存在　　(b) 使用TIM，间隙被填充，接触面积增加，热阻降低

图5. 利用热界面材料(TIM)改善热传导

如果考虑使用固体隔热垫，则最好使用具有高导热性的较软材料，以更好地填充间隙。隔热垫应尽可能薄，以提供尽可能低的热阻。安装机械装置还需要在热界面材料上提供适当的压力，以确保低热阻值。

2.5. 散热器的要求

当SMPD器件焊接到PCB板时，DCB基板的铜侧保持裸露，以便更好地进行热管理。散热需要安装散热器，如图6所示。SMPD器件中没有安装孔；因此，散热器应该使用螺钉或类似的机械方式安装在靠近器件的位置。PCB中相应的安装孔需要成为布局的一部分。为确保较低的热阻，散热器的接触表面必须平坦、平整且干净。对于安装区域，散热器表面质量必须达到或超过图6中给出的值。

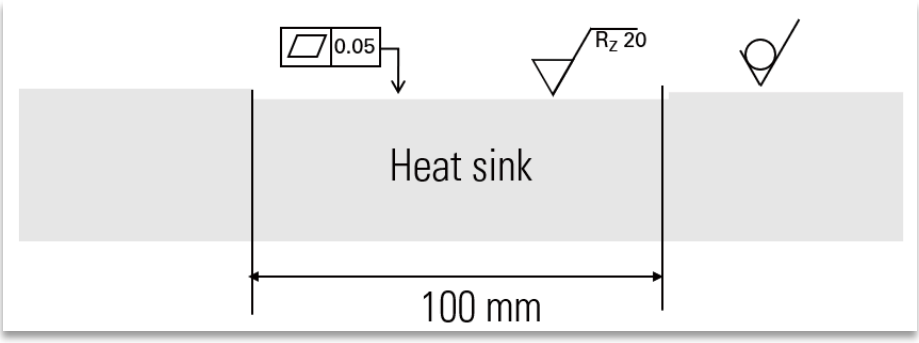


图6. 安装SMPD的散热器表面要求

安装前，建议用合适的清洁剂清洁表面。

3. 推荐的安装方法

安装SMPD可以通过多种使用成熟的方法方便地完成。可以使用螺钉或夹具获得低热阻所需的压力来完成。

3.1. 使用夹具安装单个器件

在DC–DC转换器中使用的单个器件可以使用合适的夹具连接到散热器上。设计图如图7所示。

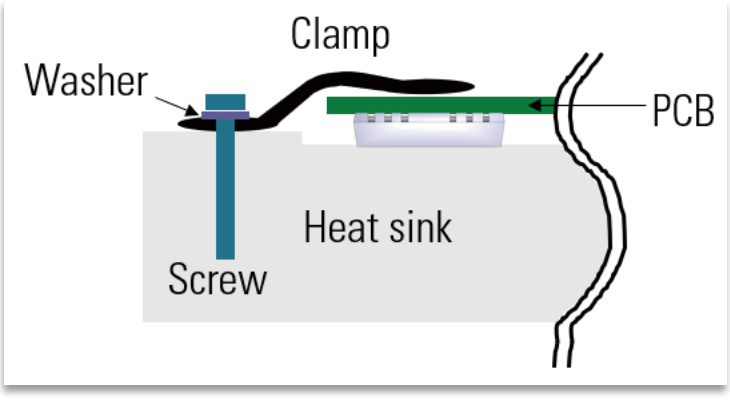


图7. 使用夹具安装SMPD

有几家制造商提供各种材料、形状和尺寸的夹具，可供考虑。施加在模块上的力需要安全地超过50牛顿。如图8所示，这个最小的力对于实现正确的热连接是必要的。

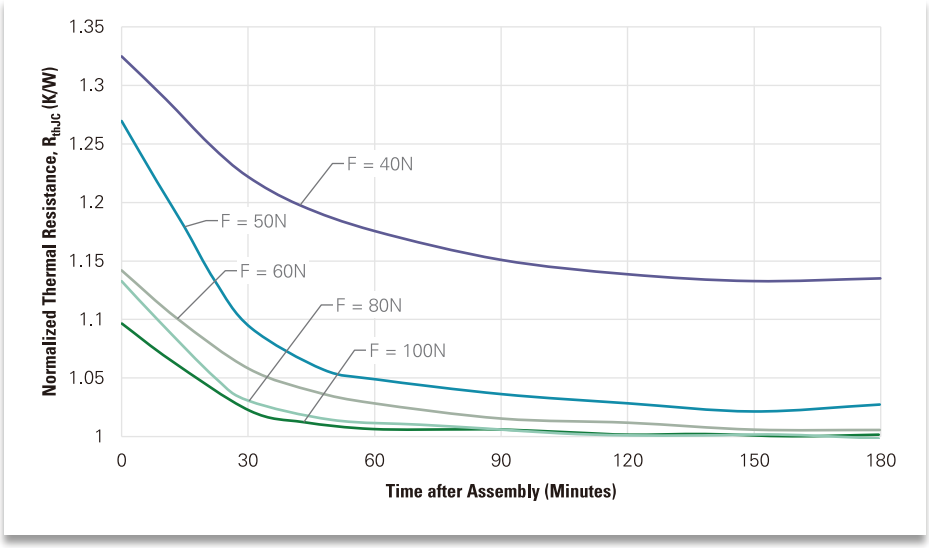


图8. 作用力和热阻之间的关系，R_{thJC}

3.2. 使用螺钉安装SMPD

通常，用螺钉安装SMPD，使用PCB施加必要的压力是一种选择。这样做时，需要考虑两个重要的细节:

- 为了建立适当的热接触，需要实现压力的均匀分布
- 需要放置垫片，防止PCB过度弯曲，同时保证施加必要的压力。

如图9所示，不使用垫片可能会导致PCB发生不必要的弯曲。需要防止这种情况，因为安装在弯曲区域的PCB板和元件的机械应力可能会导致现场瞬间缺陷或早期失效。

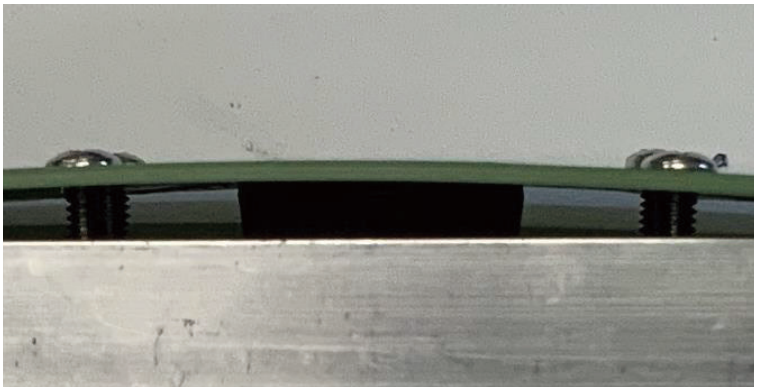


图9. 因缺少垫片导致PCB弯曲

在图10中，提供了两个被认为是做得比较好的示例。

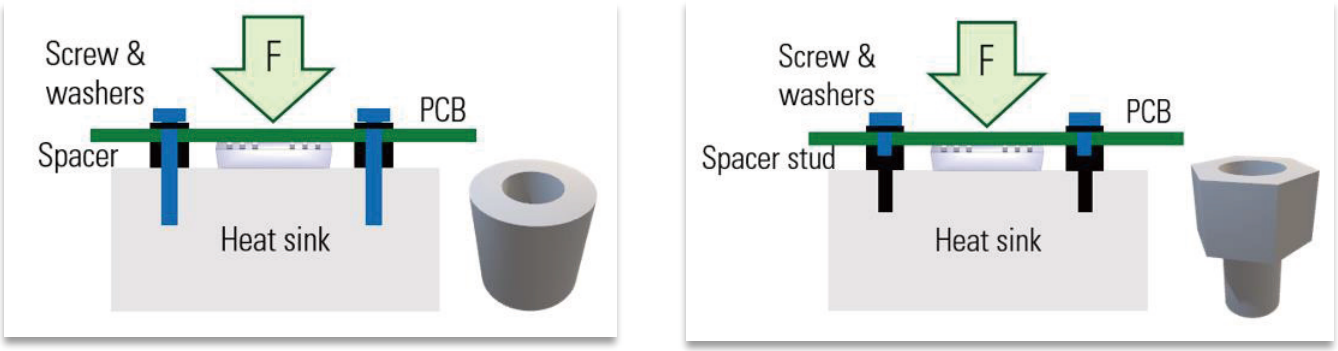


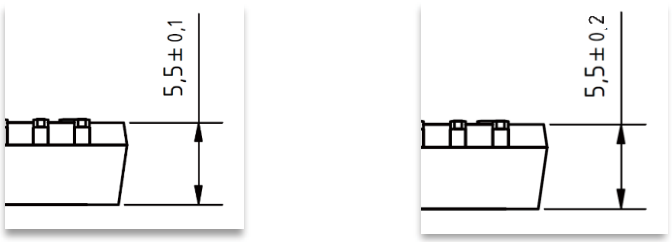
图10. 使用圆柱形垫片或螺旋式垫片螺柱安装SMPD

虽然用两个圆柱形垫片安装单个器件是一项简单的任务，但为焊接了多个器件的PCB对齐垫片却是一项挑战。在这种情况下，将间隔螺柱拧入散热器并保持在原位是一个很好的解决方案。这种螺柱有公/母或公/公两种结构，其选择取决于设计人员的偏好。

此外，间隔螺柱可以由非导电材料制成。这样可以将散热器与PCB隔离。因此，固定PCB的金属螺钉或螺母不会与散热器进行电连接。这对于PCB布线时的电气间隙和爬电距离有帮助。

如果组件的所有元件都不导电，就不用再考虑绝缘距离了。使用塑料元件进行安装仍然需要达到每个器件的安装力。

为了保证图10所示方向上的力F，有必要详细研究封装和垫片公差。数据手册中给出的图纸包括封装高度和相关公差。对于SMPD–B、SMPD–X和miniSMPD，详细信息如图11所示。



(a) SMPD-B (b) SMPD-X and miniSMPD

图11. 封装高度和公差

合适的垫片必须保证其高度始终略低于SMPD封装的高度。由于垫片本身具有公差，因此必须注意封装和垫片的任何可能组合保持在有效范围内。

SMPD–B封装的高度为5.5 ± 0.1毫米，垫片必须保持在5.4毫米以下，包括其自身的公差。合适的元件可以是标称高度为5.4毫米、公差为–0.1毫米的圆柱体。在最坏的情况下，这可能导致高度为5.6毫米的封装和5.3毫米的垫片的组合，高度差为0.3毫米。在SMPD–X和miniSMPD的情况下，由于这些封装的公差较大，这一差异会增加到0.5毫米。

通过将垫片移离封装，可以调整PCB的弯曲角度，使其保持在合理的范围内。图12中的图表总结了这种相关性。

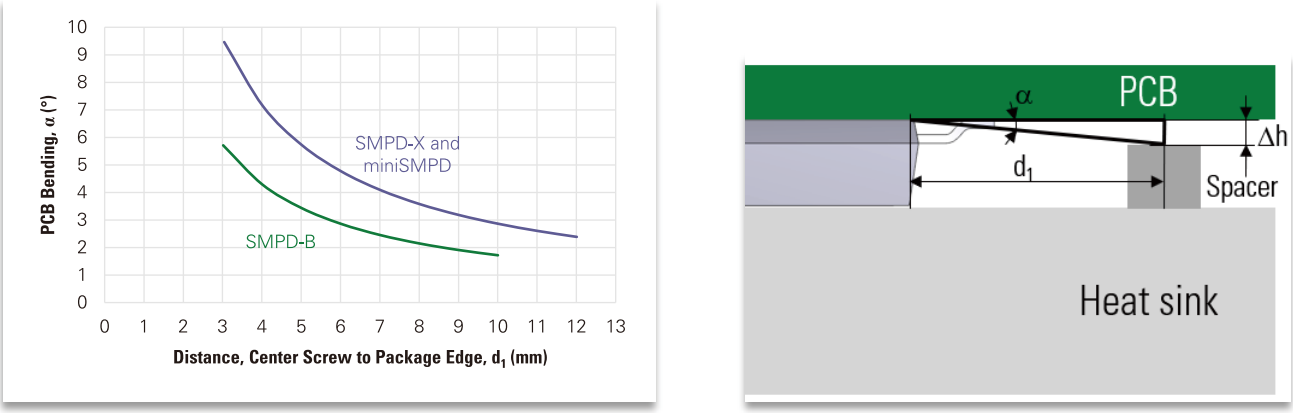


图12. 垫片距离对PCB弯曲的影响

该图基于最差假设，即Δh由最大厚度的封装和最小长度的垫片组合而成。为了保持较低的机械应力，两种封装配有的模块边缘和安装螺钉中心之间的最小距离为d1=8 mm。做为预防措施，应防止将敏感元件(如陶瓷电容器)放置在受压区域。

注：通过添加热界面材料的可压缩板或垫片来补偿公差不是最佳做法。如果其厚度足以补偿0.1毫米或更大的间隙，则元件导热性能将降低。

不可压缩的热垫需要被视为额外的高度，并增加了需要考虑的设计公差。

单个设计中可以使用多种拓扑结构的多个SMPD。变频器中的一个典型拓扑结构和相关SMPD器件如图13所示。

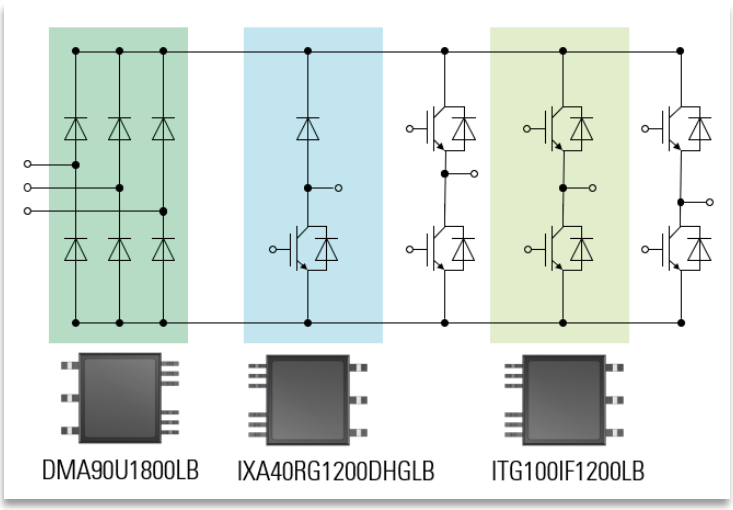


图13. 由SMPD器件组成的变频器的功率部分

安装多个器件时，必须注意模块的DCB尽可能对准同一平面。由于PCB的柔性，器件之间的微小偏差将得到补偿。

在图13中给出的示例中，组成输出级的三个功率半导体通常安装在彼此靠近的位置，而输入整流器和制动单元可以放置在便于PCB布线的位置。

排成一行的器件可以用螺钉沿其中心线固定，如图14所示。这也可以扩展到更多的模块。

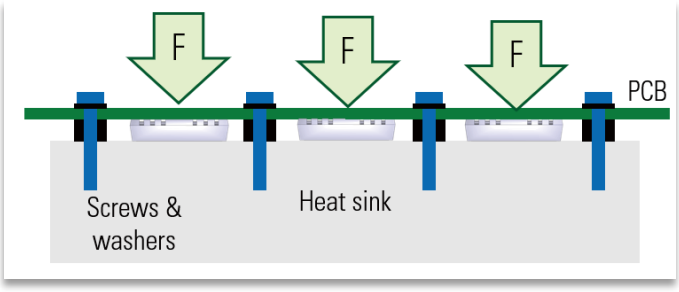


图14. 使用n+1个螺钉连续安装n个器件

当安装排成一行的多个器件时，使用支架对多个器件施加压力是另一种选择，如图15所示。

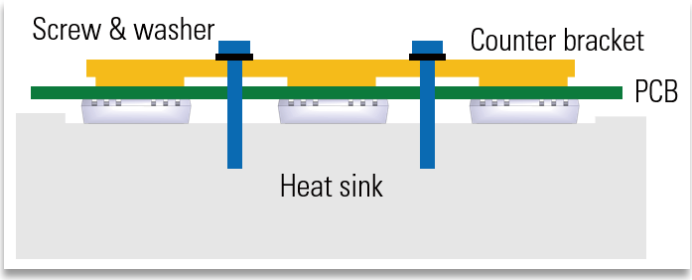


图15. 使用支架安装多个SMPD

一个精心设计的支架只对模块覆盖的区域施加力，模块之间的空间保持无压力，因此不需要加圆柱形垫片支撑，PCB不会弯曲。

支架最好由非导电材料制成，可以考虑PBT、ASA或ABS等工业热塑性塑料，并且可以通过3D打印轻松创建评估样板。用纸质塑料等固体材料研磨支架是另一种选择。在大规模生产中，定制的注塑部件仍然是一种选择。

为了保持螺钉孔小，公制螺钉M3已被证明是足够使用的。建议使用垫圈和弹簧锁垫圈，以防止长时间使用后出现松动。

一种合适的组合包括:

- 符合ISO 4672 / DIN 912标准的长度合适的公制螺钉M3，伸入散热器螺纹至少3 mm
- 符合ISO 7092/DIN 433的垫圈
- ISO 7090 / DIN 127中描述的弹簧锁垫圈。

对于螺钉，建议使用性能等级为6.8或更高的螺钉，扭矩为0.9Nm。如果首选英制螺钉，则螺钉4–32最接近3mm，建议扭矩为8lb–in。

3.3. 围绕SMPD构建的整体方法

在新建的设计中，还有一个选项可用。设计有合适弹簧元件的外壳可以将PCB保持在适当位置，同时具有施加所需压力的机械特征。同时，外壳可充当散热器。图16总体上展示了这个想法。

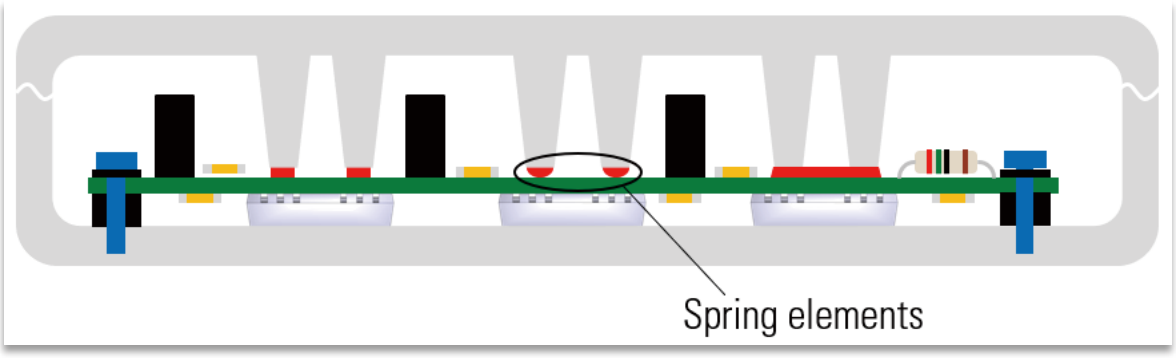


图16. 多功能封闭外壳将PCB固定到位，并在需要的地方施加压力

弹簧元件可以由螺旋金属弹簧制成，或者它们可以是较软的材料，如橡胶或合适的热塑性塑料，如TPU。

4. 热性能验证

在任何应用或设计系统中，热都是半导体的主要考虑因素。验证热界面材料的性能是否符合预期，以及半导体的结温是否保持在预期范围内，这一点非常重要。为了证实基于模拟的估计，需要在给定的设计系统内进行测量。

由于从外部无法接触到SMPD内的芯片，因此间接测量是深入了解热性能的合适方法。

该测量方法从半导体结到周围环境的总热阻 R_{thja}有关，包括热界面材料和为设计系统选择的散热器。一旦准确知道了该值，芯片的结温T_{vj} 就可以从以下方程式中计算出来：

$$T_{vj} = T_{amb} + P_v \cdot \sum R_{th} = T_{amb} + P_v \cdot R_{thja}$$

在这个等式中， P_v 代表芯片中的损耗，T_{amb}代表环境温度。

4.1. 准备和校准

首先，需要确定恒定电流下芯片正向电压与温度的关系。电流需要保持恒定，以减少变量的数量，因为正向电压取决于电流和温度。

例如，考虑在SMPD–B封装中采用半桥配置的两个MOSFET的MCB20P1200LB。

为了进行校准，该器件安装在加热板上，以精确控制温度。在稳定状态下，芯片温度和加热板温度达到相同的值。加热芯片的损耗由加热板的控制来补偿，因此在稳定状态下，两个温度再次相同。稳定状态通常在几分钟内达到。

MOSFET的特点是本身集成了体二极管，由于它们在给定电流下的正向电压与温度呈线性关系，因此它们非常适合这种测试。在测量过程中安全关闭MOSFET是必要的，以防止电流流过MOSFET的沟道，因为这将降低最终结果的准确性。施加–5V的栅极源电压就足够了。图17包括用于校准的原理图和确定的热相关性。在测量中，温度以每级10°K的速度上升。

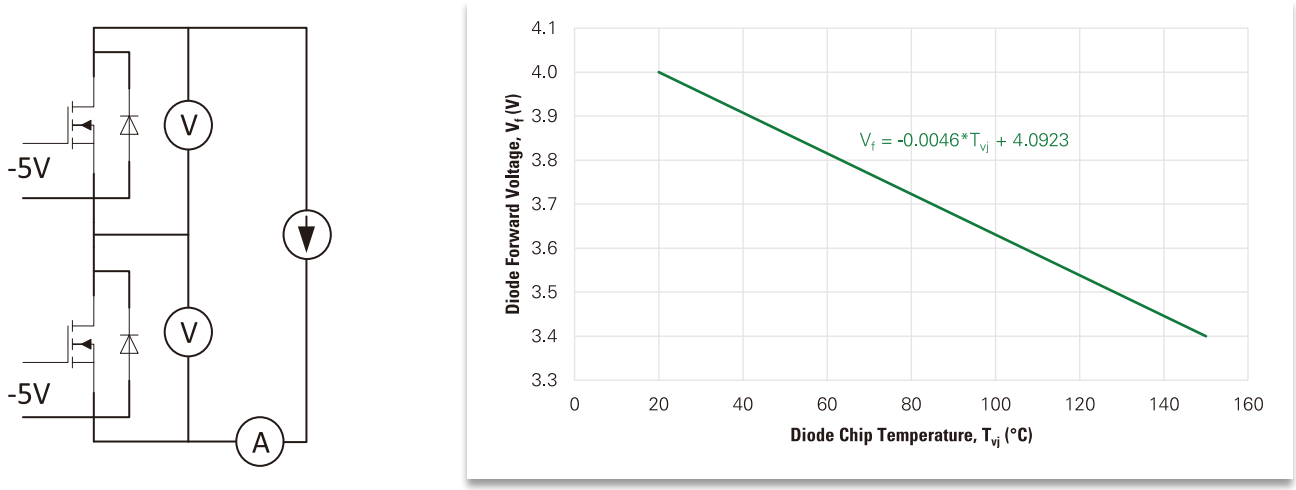


图17. 测试电路和确定的热相关性原理图

线性相关 $V_f = f(T_{vj}, I_D = 5A)$ 可以改写为 $T_{vj} = f(V_f, I_D = 5A)$.

4.2. 确定最终系统中的热阻

该测量只能在最终系统中进行，该系统由安装的PCB、热表面材料和散热器组成。现在在已知和测量的环境温度T_{amb}下重复该过程。将用于校准的相同恒定电流注入功率半导体，观察二极管两端的电压，直到达到稳定状态。这是在二极管两端的电压保持恒定时实现的。根据散热条件，这可能需要几分钟的时间。

在稳定状态下，损耗由$P_v = V_f \cdot I_D$决定， 给定热阻、温度变量和损耗之间的线性相关性， 由此产生的热阻R_{thja}可计算为:

$$P_v = \frac{\Delta T}{R_{thja}} = \frac{T_{vj} - T_{amb}}{R_{thja}} \Leftrightarrow R_{thja} = \frac{T_{vj} - T_{amb}}{P_v}$$

对MOSFETs 类器件而言，因其二极管是内生的，因此测试热阻只有一个值。但对IGBT 类器件，因其二极管是外加的，需要进行两次测量，分别确定IGBT 和 二极管的热阻。

一旦系统的最终的热阻被测定，就可以针对不同的设计条件，调整到合适的器件工作点。

5. 结论

通过SMPD封装，Littelfuse扩大了ISOPLUS™系列。这一功率半导体元件系列允许采用模块化方法来设计各种电力电子应用。

将热量分散到更大的区域可以提高热性能，同时让工程师不必顾虑器件太靠近的问题，这在CBI型功率模块中很常见。

绝缘结构以及DCB和引线框架的组合是在工业驱动器或非车载EV充电器等具有挑战性的应用中构建最紧凑设计的关键。

SMPD封装可以通过多种方式轻松安装，让工程师在设计布局时有更大的自由度。

欲了解更多信息，请访问 www.Littelfuse.com/powersemi

Mounting and Cooling Solutions for SMPD Packages

Objectives

This application note discusses various mounting solutions for Surface Mount Power Device (SMPD) packages. Mounting instructions are provided for single- and multi-device mounting respectively. A view into tolerances explains important detail when designing around the SMPD. A brief explanation of a procedure is given to determine the thermal resistance with a given design by conducting a simple experiment.

Applications

- Motor drives
- PV inverters
- UPS systems
- DC-DC converters

Target Audience

This document is intended for potential adopters of power semiconductors in the SMPD package who want to determine the appropriate mounting and cooling solution to ensure proper package mounting and thermal performance.

Contact Information

For more information on the topic of mounting SMPD-style devices, contact the Littelfuse Power Semiconductor team of product and applications experts:

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- Central & South America – CSA_PowerSemi_Tech@Littelfuse.com
- Europe. Middle East, & Africa – EMEA_PowerSemi_Tech@Littelfuse.com
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1. Introduction

The Surface Mounted Power Device (SMPD) package is an innovative solution that was introduced by IXYS (A Littelfuse Technology) in January 2013. SMPD expands the ISOPLUS™ package family for power semiconductor devices. It features Direct Copper Bonded (DCB) substrate with copper lead frame, aluminum bond wires, and a plastic molding compound. The DCB substrate inherently offers electrical insolation and allows multiple semiconductor chips on one substrate to form different circuit topologies. Combining a copper lead frame with aluminum bond-wires results in a surface mounting type of device for simplified soldering and assembly. The plastic mold compound provides excellent sealing and semiconductor protection. The backside copper of the DCB substrate is exposed and acts as large-area connection between the semiconductor and a heat sink. An illustration of the SMPD package is shown in **Figure 1**.

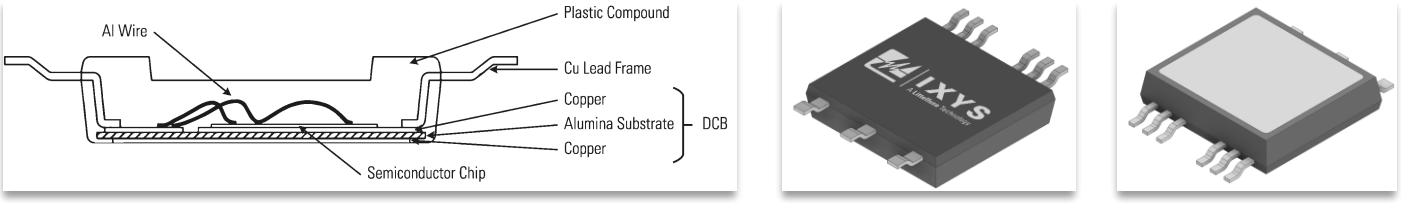


Figure 1. SMPD Package Illustration

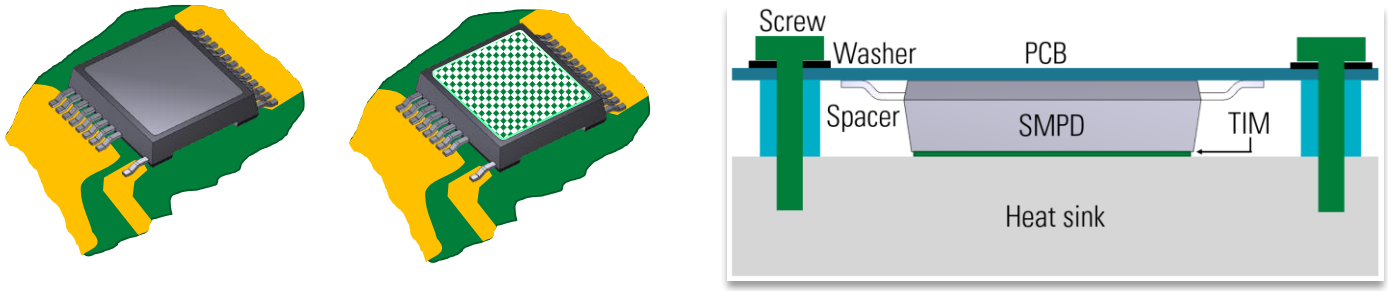
The SMPD package provides unique features for power electronic applications. These include:

- High electric insulation strength of 2500 V
- Lower thermal resistance compared to standard packages like TO-247 or TO-264
- Enhanced flexibility regarding customized topologies
- Higher current carrying capability compared to TO-style packages
- Internal construction is designed to reduce parasitic effects like stray inductance and parasitic capacitances, leading to improved EMI-performance

All these advantages make the SMPD package an exceptional candidate for both Si and SiC power semiconductors.

2. Recommended PCB and Heat Sink Assembly

The SMPD package is a surface mounted package. The devices are soldered to PCB in state-of-the-art processes. A layer of Thermal Interface Material (TIM) is needed to ensure a high thermal conductivity from the thermal pad to the heatsink. After soldering and applying TIM is completed, the assembly can be mounted to a heatsink by mounting screws. An example of heat sink assembly is shown in **Figure 2.**



(a) SMPD-X Soldered to PCB

(b) Thermal Interface Material Applied

(c) Flipped Assembly Mounted to the Heat Sink using Screws and Spacers

Figure 2. Sequence of Mounting the SMPD to a Heat Sink

2.1. Soldering Instructions

As SMD-components, all SMPD-packages can be soldered using three different approaches:

- Selective soldering with a soldering iron set to 260-287°C – Take care to ensure that heating power and thermal capacity of the soldering iron are suitable for the size of the component. Apply heat to the pins for no longer than 10 seconds.
- Wave-soldering using a temperature profile according to IEN61760-1 – Protect the DCB-area from capturing solder alloy. Kapton-style tape can be attached to prevent contamination.
- Reflow-soldering using a temperature profile as described in IPC/JEDEC J-STD-020E

Littelfuse strongly recommends using lead-free soldering alloys that are RoHS and REACH compliant.

2.2. SMPD Layout Recommendations

The SMPD-B package can carry a variety of topologies including single switches, co-packs of switch and freewheeling diodes, and more complex topologies like booster-stages or half bridges. As an example, **Figure 3** displays the SMPD-B with an integrated 1200V IGBT-based half-bridge. The SMPD-B-package is designed for applications with a working voltage up to 630V_{rms}.

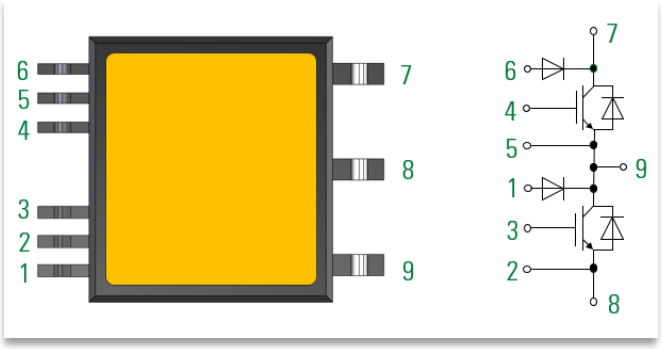
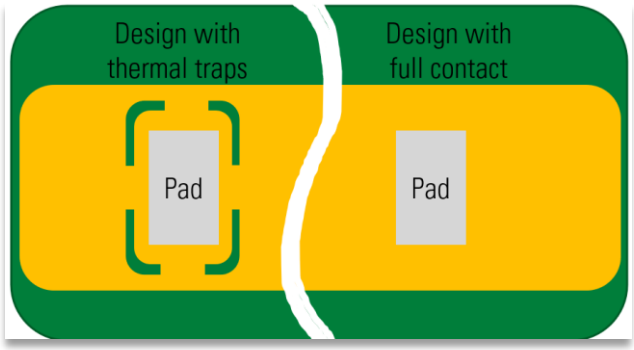


Figure 3. SMPD-B Package Outline and Topology, IXA40PG1200HGLB



(a) With thermal traps (b) With full contact

Figure 4. Solder Area

Using shapes with rounded corners as soldering pads is considered good practice. As the SMPD-B package is used in high voltage applications, rounded corners help reduce the electric field stress seen on rectangular corners. The high voltage pads are pins 7, 8, and 9. A corner radius of 0.6mm or 25mil is recommended. The same practice is advised for the angles of PCB traces and copper polygons.

A common approach involves applying thermal traps in larger copper areas to improve the soldering process. These traps, as seen in **Figure 4**, prevent the heat from soldering to escape into larger copper areas and thus help to prevent the formation of cold solder spots. Inherently, the cross section available to carry electric current is reduced.

Care has to be taken to design the thermal traps large enough to efficiently block the heat during soldering and at the same time small enough to keep a sufficient cross section to carry current.

The SMPD's internal construction is designed to also carry heat to the pins during operation to enhance cooling. Thermal traps at the pins may prevent this heat from being dissipated properly; therefore, a design with a full contact area is preferred.

2.3. Isolation Management

Two major parameters require to be considered when PCB-layouts are designed:

- Clearance – the shortest possible distance between two points, and
- Creepage distance – the shortest path from one point to another point along an uninterrupted line on solid material

In high-voltage environments, arcing between different voltage levels has to be prevented. Arcing takes place over air-gaps – clearance distances – so the voltage level expected in the final system defines the distance between pads and traces as well as between active areas and heat sinks or other grounded parts. Even if the clearance between two points is chosen to be high enough, the insulation strength can be reduced by conductive particles over a longer period. This depends on the degree of pollution, which relates to the ambient conditions the device is used in.

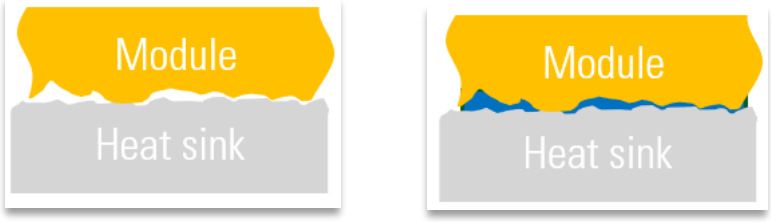
IEC60664-1 gives an insight about the relevant conditions that need to be considered to determine the creepage and clearance distances in a targeted design.

2.4. Use of Thermal Interface Materials

The use of Thermal Interface Materials (TIM) is mandatory to achieve a suitable contact between the device's base and the heat sink surface. It reduces the thermal resistance case-to-heatsink, R_{thch}. Thermal interface materials are available as thermal pad and thermal grease/compound. Unlike the discrete packages where the copper cooling pad is usually electrically active, SMPD packages feature a DCB structure which uses a layer of ceramic as electrical isolation. With up to 2500 V isolation voltage, the package provides the option to use electrically non-isolated thermal interface materials. It is not recommended to use an interface material with isolation such as silicone-pads used for discrete packaged devices. These materials inherently exhibit a higher thermal resistance compared to thermal grease/compound or conductive thermal pads.

The thermal interface materials should be applied evenly to the device base plate or the heat sink surface. Ideally, screen printing is used to achieve accurate and reproduceable results.

As no electrical isolation is required from the TIM layer, it is recommended to have a very thin layer of TIM so that the material just fills the gaps and voids between the device's copper pad and the heatsink, as seen in **Figure 5.**



(a) Without TIM, air gaps remain

(b) With TIM, the gaps are filled, contact area increases, and thermal resistance is reduced

Figure 5. Improving Thermal Transfer by using Thermal Interface Material (TIM)

If a solid thermal pad is considered, softer materials with high thermal conductivity are preferred to better fill the gaps. The thermal pad should be as thin as possible to provide the lowest possible thermal resistance. The mounting mechanism also needs to provide proper pressure on the thermal interface material to ensure a low value of thermal resistance.

2.5. Heat Sink Preparation

When the SMPD package is soldered to PCB, the copper side of the DCB substrate remains exposed for better thermal management. A heatsink needs to be mounted for heat dissipation, as shown in **Figure 6**. There are no mounting holes in the SMPD package; therefore, the heatsink should be mounted using screws or similar mechanical ways close to the package. Corresponding holes in the PCB need to be part of the layout.

To ensure a low value of thermal resistance, the contact surface of the heat sink must be flat, even, and clean. For the mounting area, the surface quality has to achieve or exceed the values given in **Figure 6**.

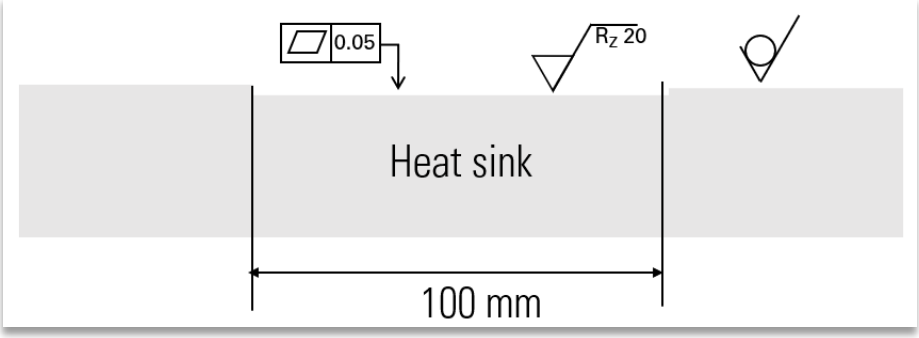


Figure 6. Heat Sink's Surface Requirements to Mount an SMPD

Prior to mounting, cleaning the surface with a suitable cleaning agent is advised.

3. Recommended Mounting Methods

Mounting an SMPD can conveniently be done in a multitude of ways using well-established methods. Screws, rivets, or clamps can be used as long as the pressure needed to obtain low thermal resistance is achieved.

3.1. Mounting a Single Device using a Clamp

A single device, as used in DC-DC-converters, can be attached to a heat sink using a suitable clamp. The design is drafted in **Figure 7**.

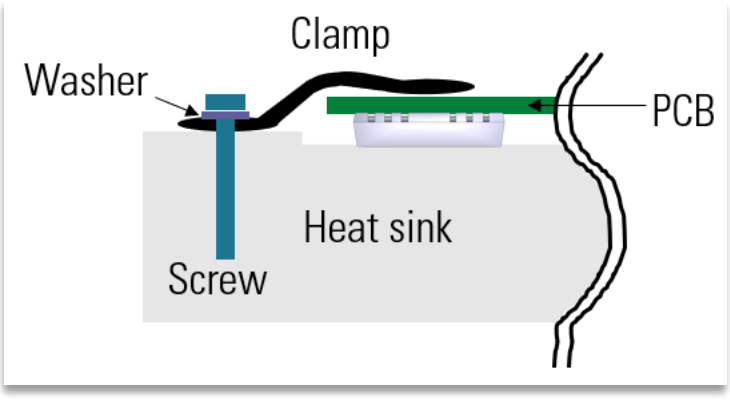


Figure 7. SMPD Mounted using a Clamp

Several manufacturers offer clamps in a wide variety of materials, shapes, and sizes that might be considered. The force applied to the module needs to safely exceed 50 Newtons. This minimum force is necessary to achieve a proper thermal connection, as the diagram in **Figure 8** reveals.

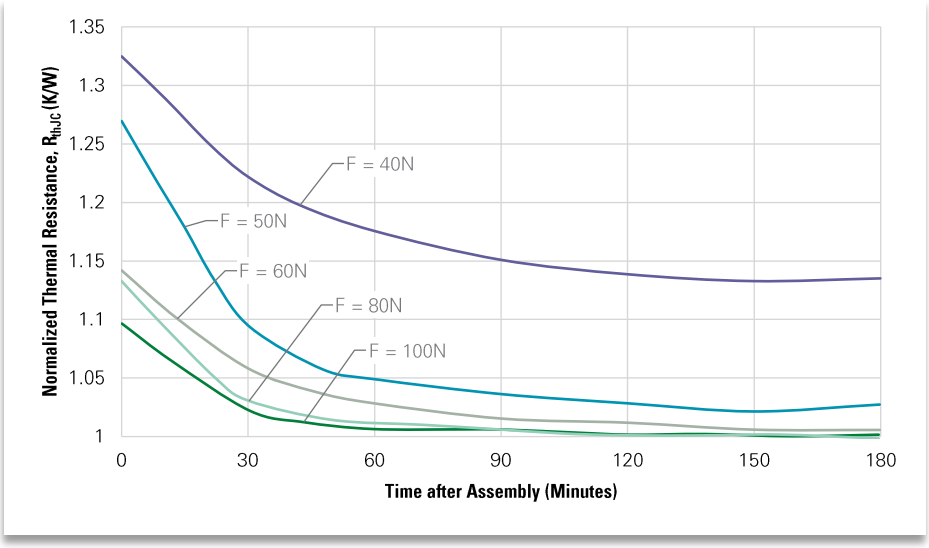


Figure 8. Correlation between Force Applied and Thermal Resistance, R_{thJC}

3.2. Mounting the SMPD using Screws

Generally, mounting the SMPD with screws, using the PCB to apply the necessary pressure is an option. When doing so, two important details need to be considered:

- an even distribution of pressure needs to be achieved to establish a suitable thermal contact
- spacers need to be in place that prevent bending the PCB too much while at the same time guarantee that the necessary pressure is applied.

Not implementing spacers can lead to unwanted bending of the PCB, as demonstrated in **Figure 9**. This needs to be prevented as the mechanical stress to the PCB and components mounted in the bent area can lead to instant defects or early failure in the field.

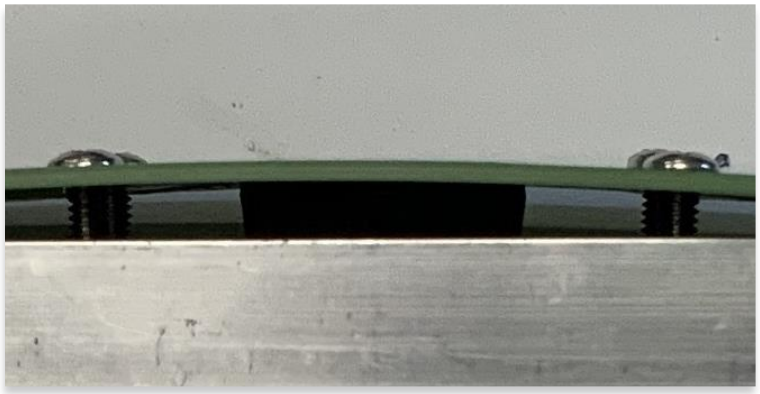


Figure 9. Bending of PCB due to Missing Spacers

In **Figure 10**, two examples are provided that are considered good practice.

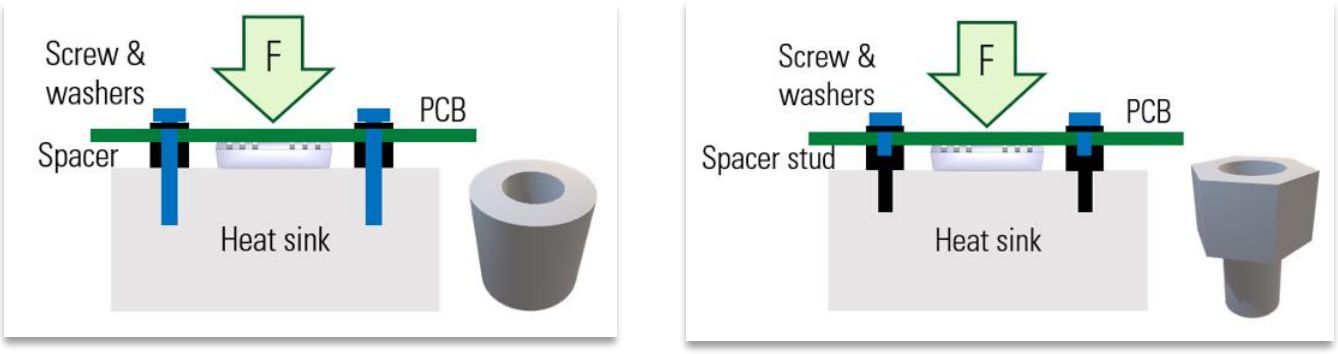


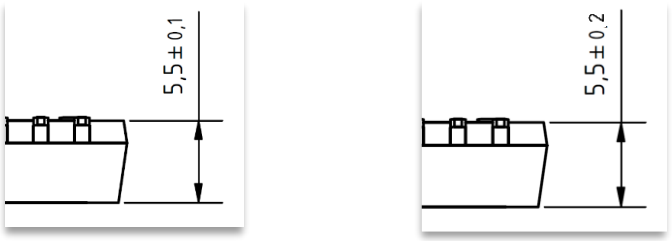
Figure 10. Mounting the SMPD using Cylindrical Spacers or Screw-type Spacer Studs

While mounting a single device with just two cylindrical spacers is a simple task, aligning spacers for a PCB that holds multiple devices can be challenging. In this case, spacer studs that are screwed into the heat sink and thus remain in place, pose a good solution. Such studs are available in male/female or male/male configuration and the selection depends upon the designer's preference.

In addition, the spacer studs can be made of non-conductive material. This keeps the heat sink isolated from the PCB. Thus, a metal screw or nut holding the PCB is not galvanically connected to the heat sink. This can be a helpful feature with regards to clearance and creepage distances during PCB-routing.

This sort of consideration becomes obsolete if all parts for the assembly are electrically non-conductive. Using plastic parts for mounting still requires that the mounting forces for each device are achieved.

A detailed look into the package and spacer tolerances is necessary to guarantee a force F in the direction shown in **Figure 11**. The drawing given in the datasheets includes the package height and the correlated tolerances. For SMPD-B, SMPD-X, and miniSMPD, the details are displayed in **Figure 11**.



(a) SMPD-B (b) SMPD-X and miniSMPD

Figure 11. Package Height and Tolerances

A suitable spacer must guarantee a height which is always slightly below that of the SMPD-package. As the spacer itself has a tolerance, care has to be taken that any possible combination of package and spacer remains in a valid range.

With a SMPD-B package's height of $5.5^{\pm 0.1}$mm, a spacer must remain below 5.4mm, including its own tolerances. A suitable part could be a cylinder with a nominal height of 5.4mm and a tolerance of -0.1mm. In a worst-case scenario, this could lead to a combination of a package with 5.6mm height and a spacer of 5.3mm, with a difference in height of 0.3mm. This difference grows to 0.5mm in case of the SMPD-X and miniSMPD due to the larger tolerances of these packages.

By moving the spacer away from the package, the bending angle of the PCB can be adjusted to remain within reasonable limits. This correlation is summarized in the diagram in **Figure 12**.

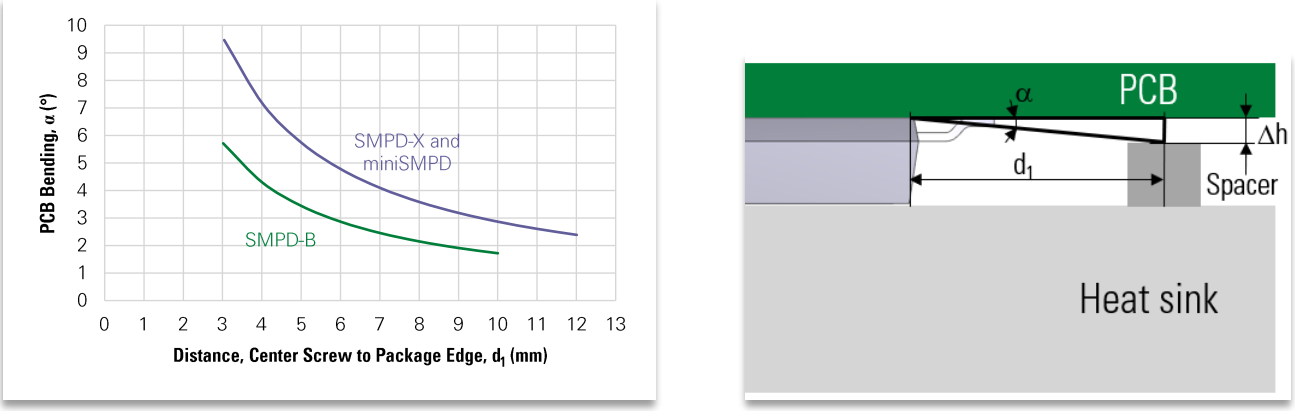


Figure 12. Impact of Spacer Distance to PCB Bending

The diagram is based on the worst-case assumption that Δh results from combining a package with a maximum thickness and a spacer of minimum length. To keep the mechanical stress low, both packages are well-served with a minimum distance of d_1=8mm between the module's edge and the center of the mounting screw. As a precaution, placing sensitive components like ceramic capacitors in the stressed area should be prevented.

Note: It is not considered best practice to compensate the tolerances by adding a compressible sheet or pad of thermal interface material. If it were thick enough to compensate a gap of 0.1mm or more, the thermal transfer, and therefore performance, of the component would be reduced.

Thermal pads that are not compressible need to be considered as an additional height and add a further tolerance to the setup that needs to be accounted for.

Multiple SMPDs in a variety of topologies can be used within an individual design. A typical topology of a converter in drives applications and the correlating power semiconductors can be seen in **Figure 13**.

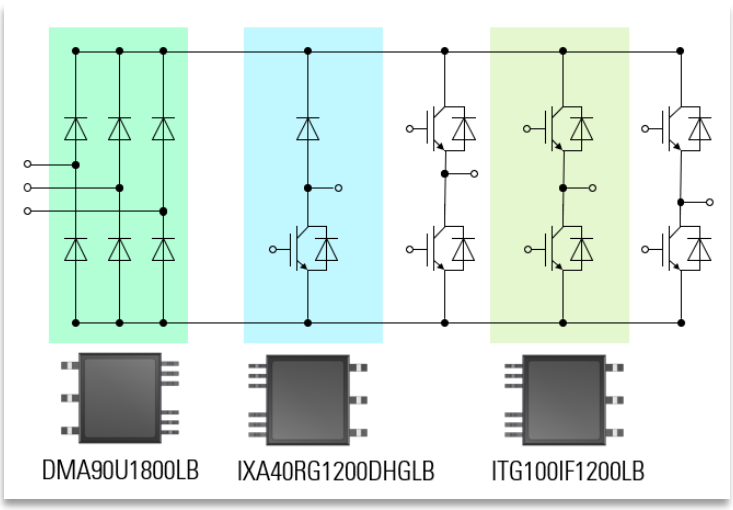


Figure 13. Power Section of an Inverter for Drives Application, Built by SMPD Devices

When mounting multiple devices, care has to be taken that the DCBs of the modules are as well aligned to the same plane as possible. Minor misalignments between the devices will be equalized due to the flexibility of the PCB.

The three power semiconductors that form the output stage in the example given in **Figure 13** are usually mounted close to each other, while the input rectifier and brake-chopper can be positioned in a location convenient for routing the PCB.

Parts aligned in a row can be fixed using screws along their center line, as shown in **Figure 14**. This can also be extended to a larger number of modules.

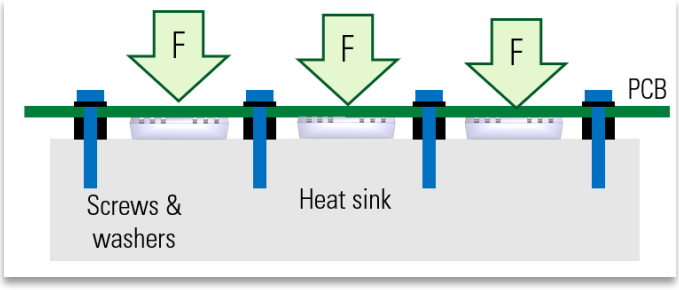


Figure 14. Mounting *n* Devices in a Row using *n+1* Screws

Using a counter bracket to apply pressure to several devices is a further option when mounting multiple devices aligned in one row, as seen in **Figure 15**.

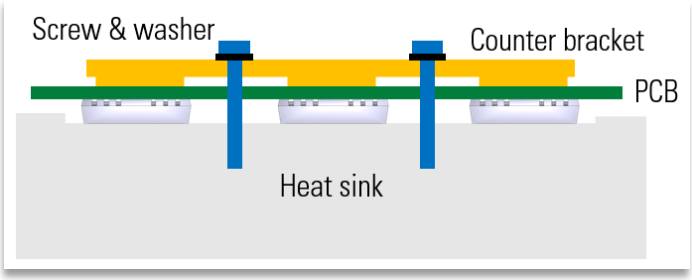


Figure 15. Multiple SMPDs Mounted using a Counter Bracket

A well-designed counter bracket applies a force only to the area covered by the module. The space between the modules remains free of pressure. Therefore, no bending of the PCB occurs, and spacers or supports are not needed.

The bracket is preferably made from non-conductive materials. Industrial thermoplastics like PBT, ASA, or ABS can be considered and first parts for evaluation can easily be created by 3D-printing. Milling brackets from solid material like paper-based plastics is another option. In mass production, customized injection-molded parts remain an option.

To keep the hole for the screws small, metric screws as small as M3 have proven to be sufficient. The use of washers and spring-lock washers is recommended to prevent loosening over time.

One suitable combination consists of:

- a metric screw M3 according to ISO 4672 / DIN 912 in a suitable length, reaching into the heat sink's thread by at least 3mm
- a washer according to ISO 7092 / DIN 433
- spring-lock washer as described in ISO 7090 / DIN 127.

For the screw, property class 6.8 or higher is recommended with a torque applied of 0.9Nm. If imperial screws are preferred, a screw 4-32 is closest to 3mm and a torque of 8lb-in is recommended.

3.3. Holistic Approach Built around the SMPD

In designs that are newly built, one further option is available. A housing, designed with suitable spring elements, can hold the PCB in place while at the same time have mechanical features that apply the desired pressure. Simultaneously, the encapsulation acts as the heat sink. **Figure 16** displays the idea in general.

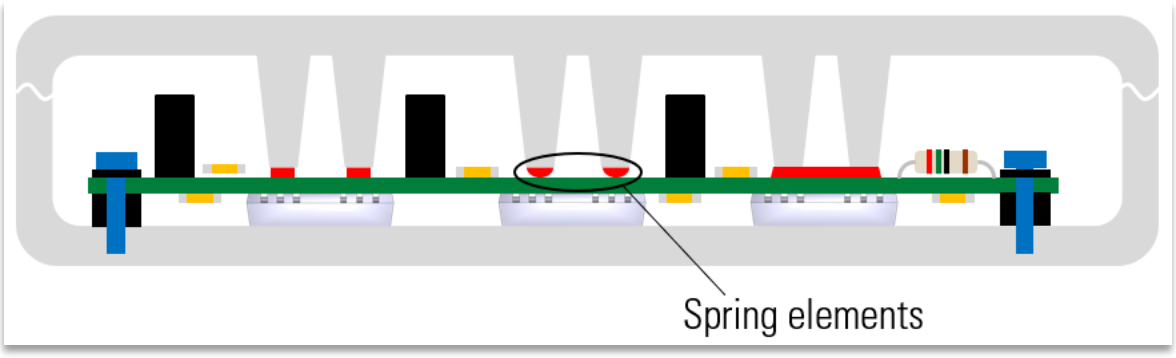


Figure 16. Multi-functional Encapsulation to Fix the PCB in Place and Apply Pressure where needed

The spring elements can be made of helical metal springs or they can be softer materials like rubber or suitable thermoplastics like TPU.

4. Thermal Performance Verification

In any application or setup, the thermal conditions are a major consideration for the semiconductor. It is important to verify that thermal interface material performs as predicted and that the semiconductor's junction temperature remains within the expected limits. To substantiate estimations based on simulations, a measurement within the given setup is needed.

As the chips within the SMPD are not accessible from outside, an indirect measurement is an appropriate way to get an insight about the thermal performance.

The procedure is about measuring the resulting sum of thermal resistances R_{thja} from the semiconductor's junction to the surrounding ambient, including thermal interface and the heat sink that is chosen for the setup. Once this value is known precisely, the chips' junction temperatures T_{vj} can be calculated from the following linear equation:

$$T_{vj} = T_{amb} + P_v \cdot \sum R_{th} = T_{amb} + P_v \cdot R_{thja}$$

In this equation, P_v represents the losses in the chip and T_{amb} is the ambient temperature.

4.1. Preparation and Calibration

First, the correlation of a die's forward voltage as a function of temperature, using a constant current, needs to be determined. The current needs to remain constant to reduce the number of variables, as the forward voltage depends on both, current and temperature.

As an example, the MCB20P1200LB featuring two MOSFETs in a half bridge configuration in an SMPD-B package is considered.

For the calibration, the device is mounted to a heat plate to precisely control the temperature. In steady state, the chip temperature and the heat plate's temperature reach the same value. Losses that heat up the chip are compensated by the heat plate's control, so that in steady state the two temperatures are the same again. Steady state is typically reached within a matter of minutes.

The MOSFETs feature body diodes as inherent part of the die. These are well-suited for the proposed procedure as their forward voltage for a given current linearly depends on the temperature. Safely turning off the MOSFET during the measurement is necessary to prevent current flowing through the MOSFET's channel as this will reduce the final result's accuracy. Applying a gate-source voltage of -5V is sufficient. **Figure 17**. includes the schematic used for calibration and the thermal dependance determined. For the measurement, the temperature was increased in steps of 10°K.

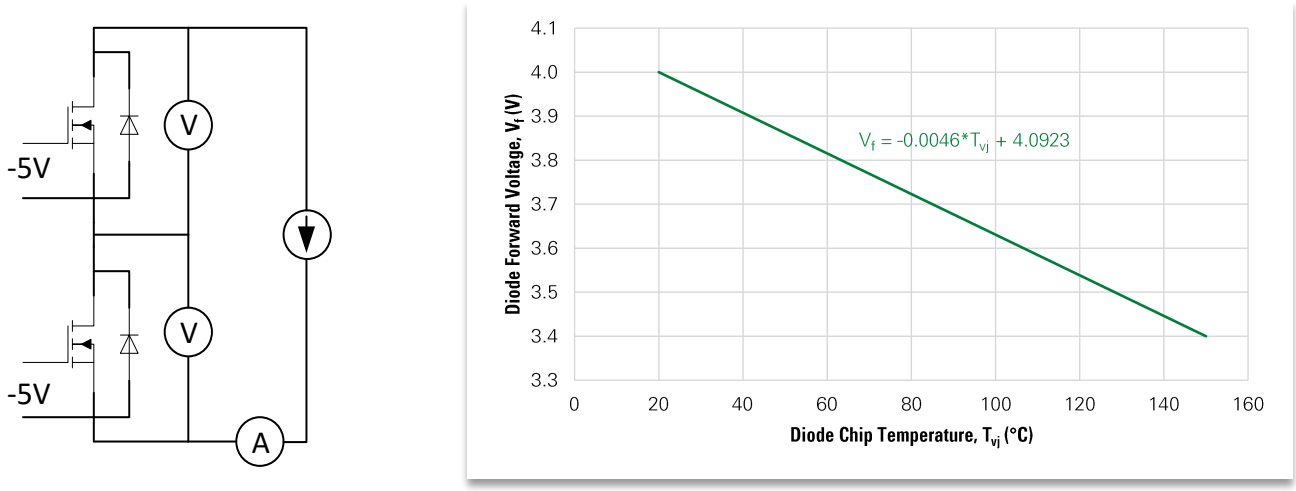


Figure 17. Schematic for the Test Setup and the Thermal Dependence Determined

The linear correlation $V_f = f(T_{vj}, I_D = 5A)$ can be rewritten into $T_{vj} = f(V_f, I_D = 5A)$.

4.2. Determining the Thermal Resistance in the Final Setup

This measurement can only be done within the final setup consisting of the mounted PCB, thermal interface material, and heat sink in place, mounted with the final technique. The process is now repeated at a known and measured ambient temperature T_{amb}. The same constant current as used for the calibration is injected into the power semiconductor and the voltage across the diode is observed until steady state is reached. This is achieved when the voltage across the diodes remains constant. Depending on the cooling conditions, this again can take several minutes.

In steady state, the losses result in $P_v = V_f \cdot I_D$. Given the linear correlation between thermal resistance, temperature swing and losses, the resulting thermal resistance R_{thja} can be calculated as:

$$P_v = \frac{\Delta T}{R_{thja}} = \frac{T_{vj} - T_{amb}}{R_{thja}} \Leftrightarrow R_{thja} = \frac{T_{vj} - T_{amb}}{P_v}$$

In applications that use the MOSFETs and the body diode, this procedure returns the value for one die that serves the function of the switch as well as the function of the freewheeling diode. This procedure can also be used on other chip technologies like IGBTs. In that case, conducting two measurements is advised as the thermal resistances of the diodes and the switches are independent.

Once the thermal resistance of the final design is known, calculations for operating points different from the calibration conditions can be done.

5. Conclusion

With the SMPD-package, Littelfuse has enlarged the ISOPLUS™ family. This portfolio of power semiconductor components allows a modular approach to set up a wide variety of power electronic applications.

Spreading the heat to larger areas enhances the thermal performance while at the same time releasing the designer from unwanted proximities, often seen in CBI-style power modules.

The isolated architecture and the combination of DCB and lead frame are key to building most compact designs in challenging applications like industrial drives or off-board EV-chargers.

The package can easily be mounted in a variety of ways, giving the designer further degrees of freedom in setting up their layouts.

IXYS

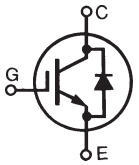
1200V XPT™ IGBT GenX3™ w/ Diode

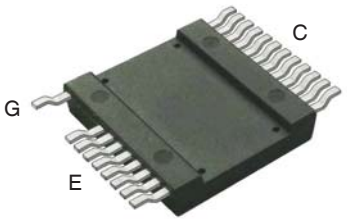
MMIX1Y82N120C3H1

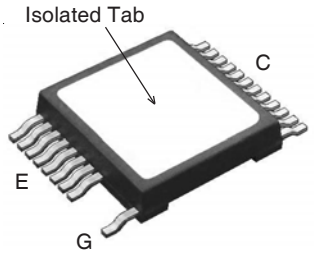
V_{CES} = 1200V
I_{C110} = 36A
$V_{CE(sat)}$ ≤ 3.4V
$t_{fi(typ)}$ = 93ns

(Electrically Isolated Tab)

High-Speed IGBT
for 20-50 kHz Switching







G = Gate E = Emitter
C = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capability)	78	A
I_{C110}	T_C = 110°C	36	A
I_{F110}	T_C = 110°C	34	A
I_{CM}	T_C = 25°C, 1ms	320	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 2Ω Clamped Inductive Load	I_{CM} = 164 @$V_{CE} \leq V_{CES}$	A
P_C	T_C = 25°C	320	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force	50..200/11..45	N/lb.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1200			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	μA
	Note 2, T_J = 125°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 82A, V_{GE} = 15V, Note 1		2.9	3.4	V
	T_J = 125°C		3.5		V

Features

- Optimized for Low Switching Losses
- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Square RBSOA
- Isolation Voltage 2500V~
- Anti-Parallel Ultra Fast Diode
- Positive Thermal Coefficient of Vce(sat)
- High Current Handling Capability
- International Standard Package

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- High Frequency Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	30	50		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		4060		pF
C_{oes}			285		pF
C_{res}			110		pF
$Q_{g(on)}$	I_C = 82A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		215		nC
Q_{ge}			26		nC
Q_{gc}			84		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**		29		ns
t_{ri}	I_C = 80A, V_{GE} = 15V		78		ns
E_{on}	V_{CE} = 0.5 • V_{CES}, R_G = 2Ω		4.95		mJ
$t_{d(off)}$	Note 3		192	280	ns
t_{fi}			93		ns
E_{off}			2.78	5.00	mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C**		29		ns
t_{ri}	I_C = 80A, V_{GE} = 15V		90		ns
E_{on}	V_{CE} = 0.5 • V_{CES}, R_G = 2Ω		7.45		mJ
$t_{d(off)}$	Note 3		200		ns
t_{fi}			95		ns
E_{off}			3.70		mJ
R_{thJC}				0.39	°C/W
R_{thCS}			0.05		°C/W
R_{thJA}			30		°C/W

Reverse Diode (FRED)

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 60A, V_{GE} = 0V, Note 1			2.7	V
	T_J = 125°C		1.9		V
I_{RM}	I_F = 60A, V_{GE} = 0V, T_J = 125°C		41		A
t_{rr}	$-di_F/dt$ = 700A/μs, V_R = 600V		420		ns
R_{thJC}				0.54	°C/W

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp I_{CES} measurement.
3. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

Fig. 1. Output Characteristics @ T_J = 25°C

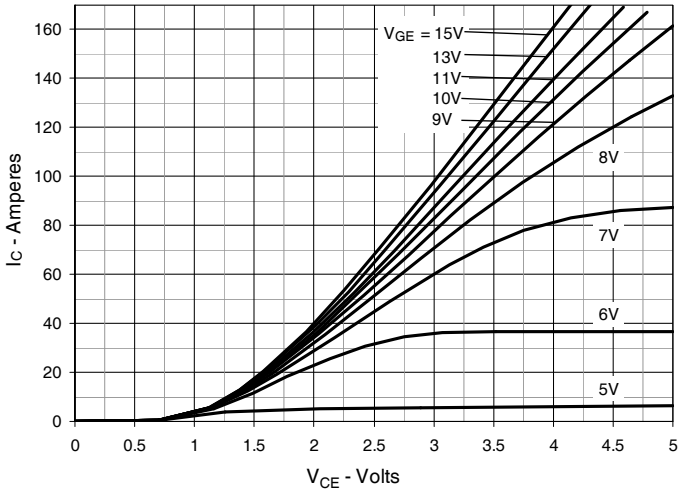


Fig. 2. Extended Output Characteristics @ T_J = 25°C

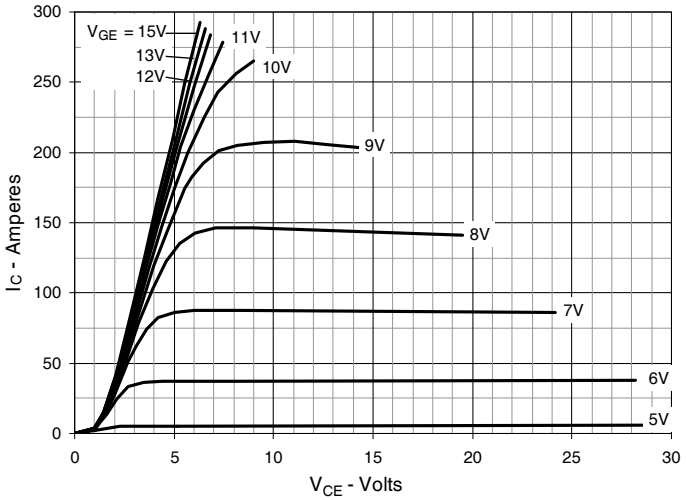


Fig. 3. Output Characteristics @ T_J = 125°C

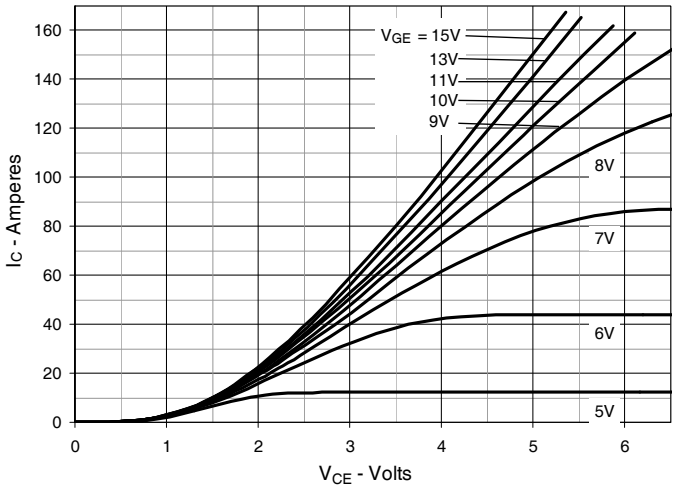


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

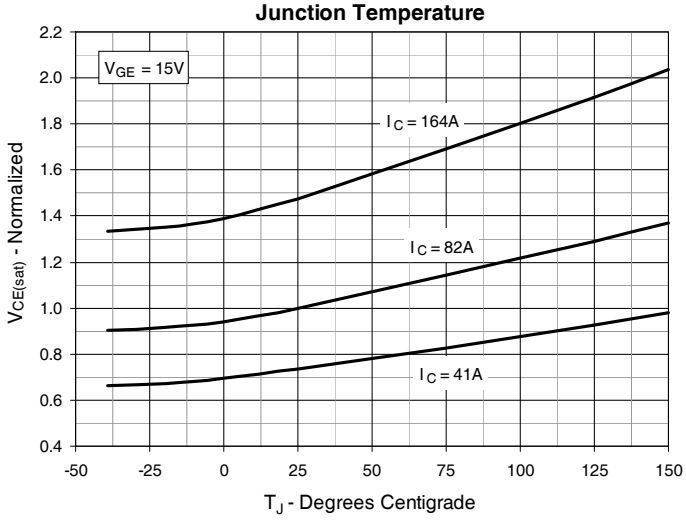


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

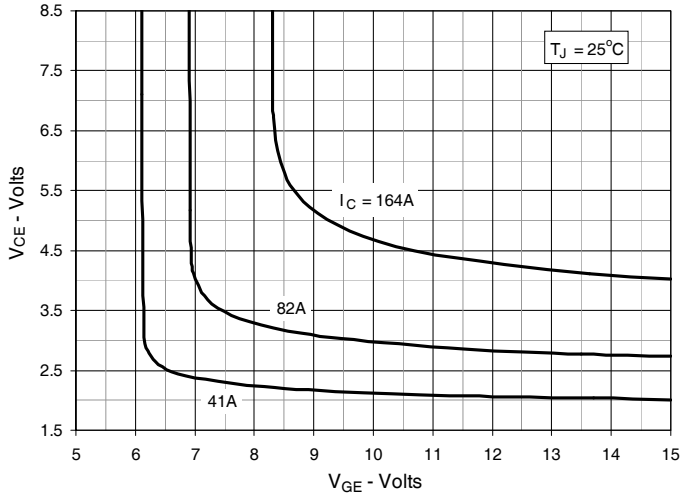


Fig. 6. Input Admittance

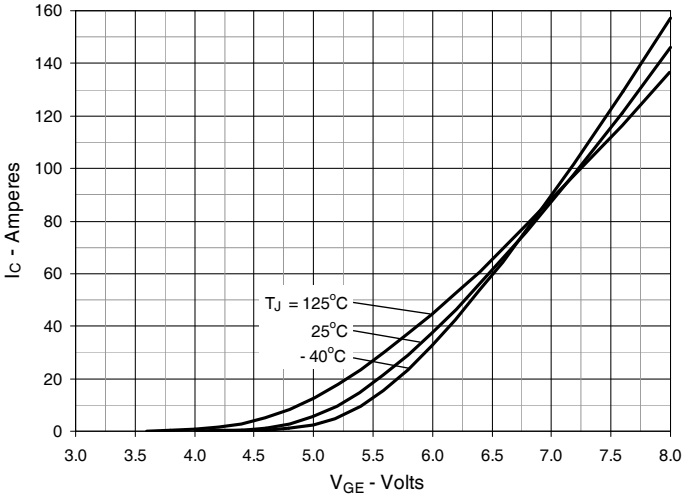


Fig. 7. Transconductance

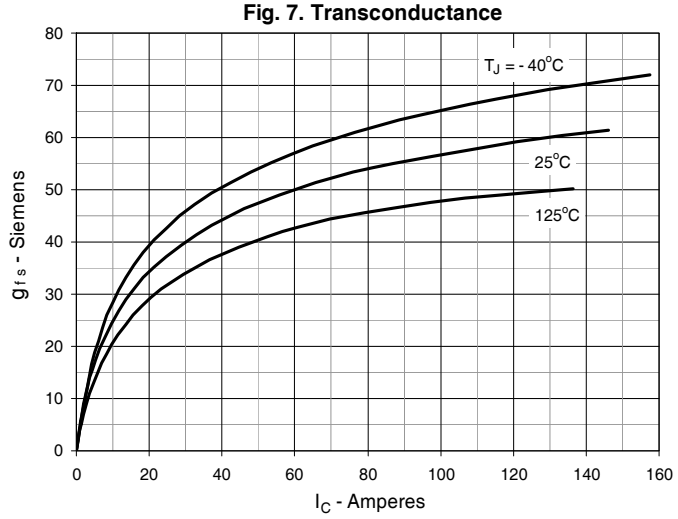


Fig. 8. Gate Charge

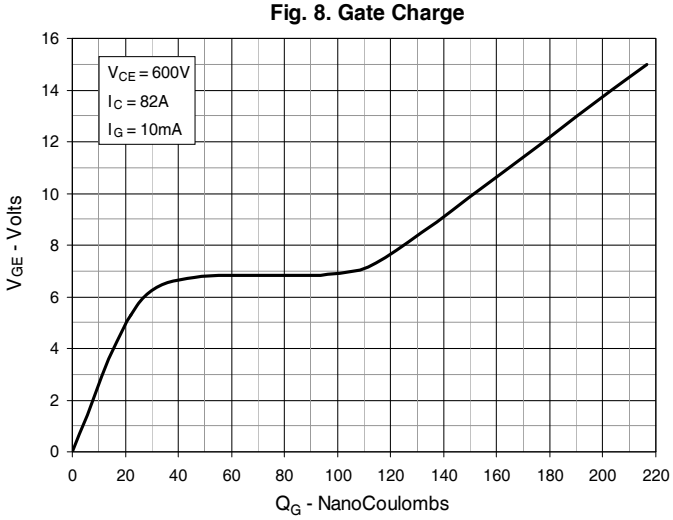


Fig. 9. Capacitance

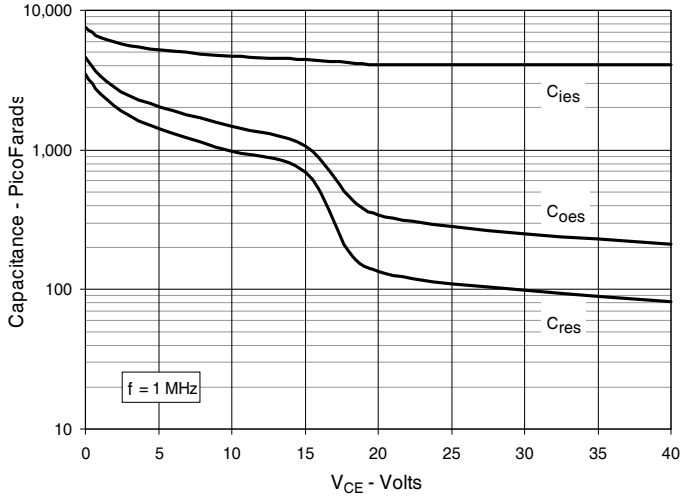


Fig. 10. Reverse-Bias Safe Operating Area

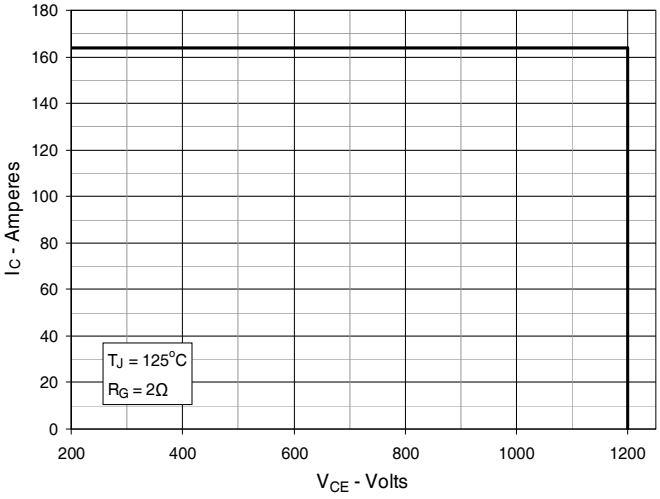


Fig. 11. Maximum Transient Thermal Impedance

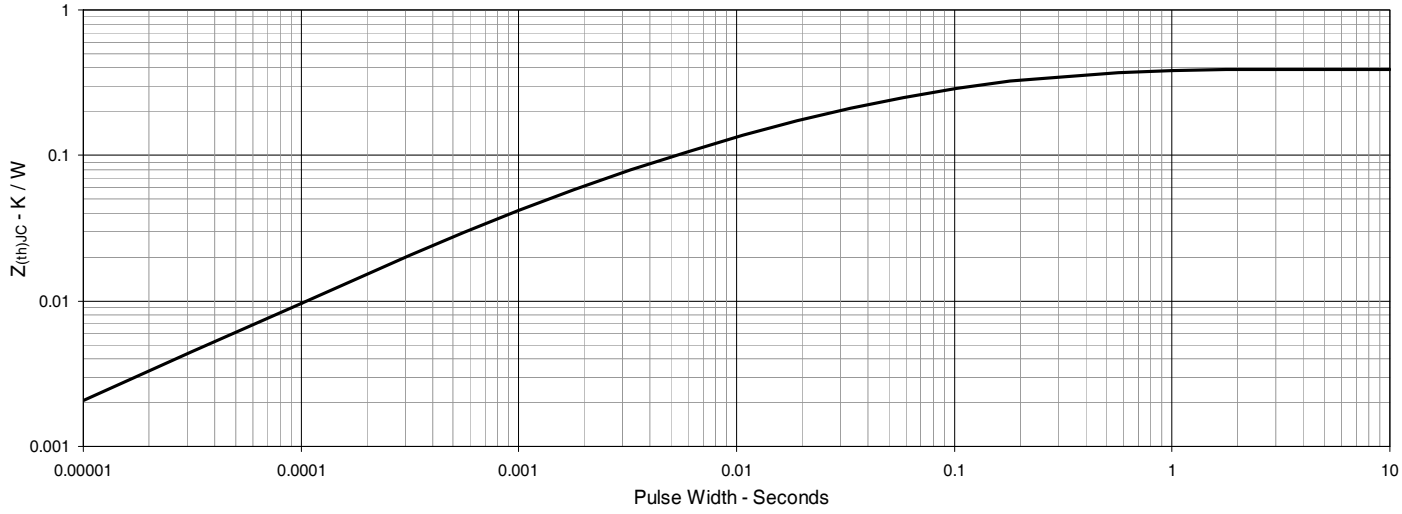


Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

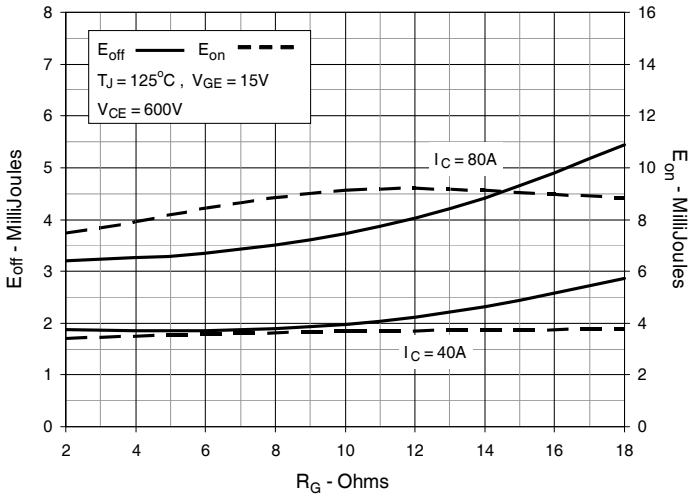


Fig. 13. Inductive Switching Energy Loss vs. Collector Current

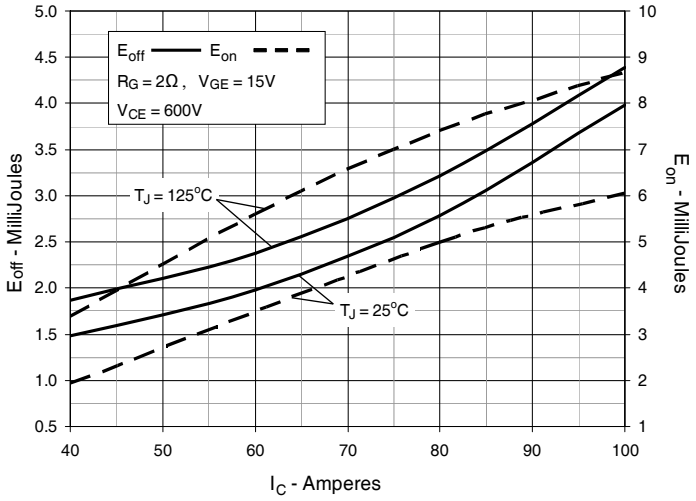


Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

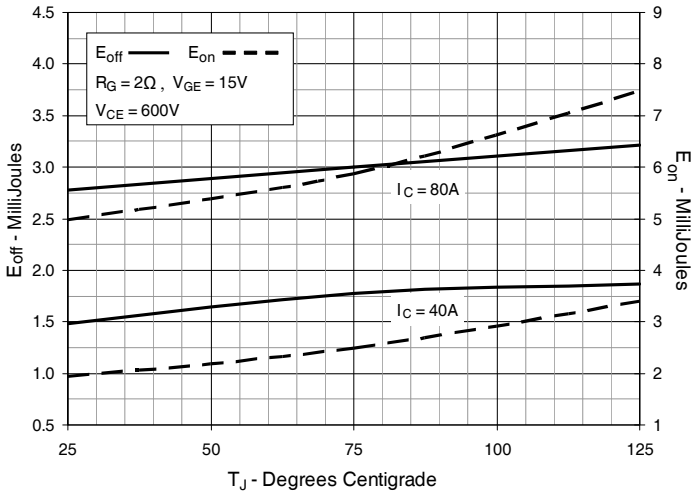


Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

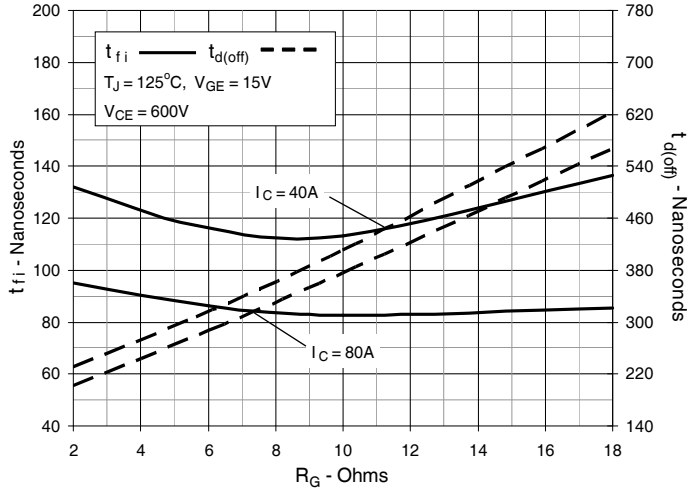


Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

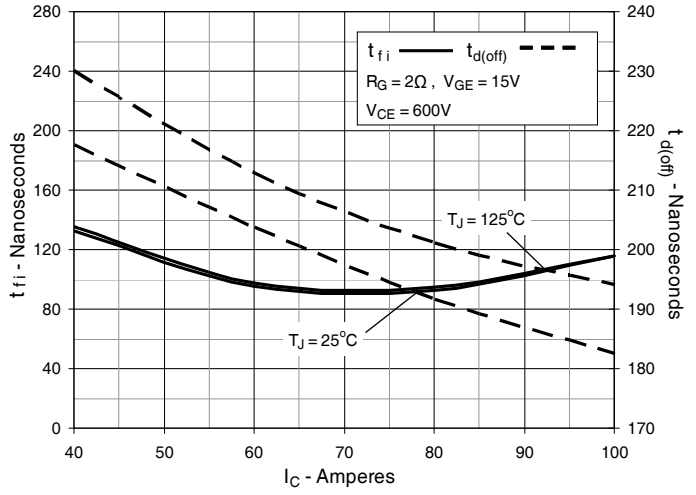


Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature

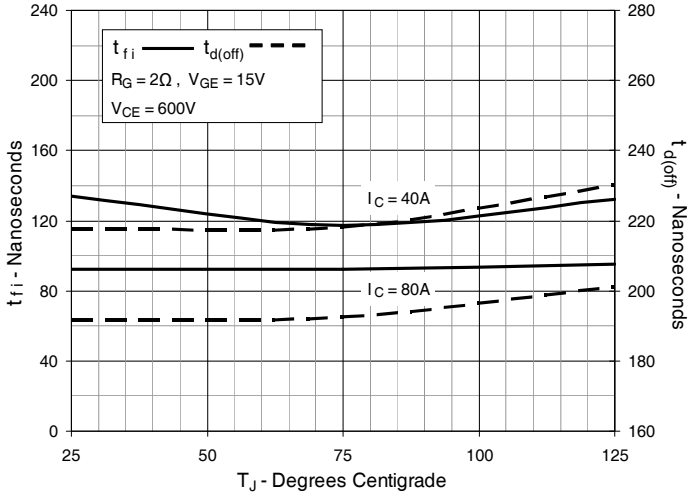


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

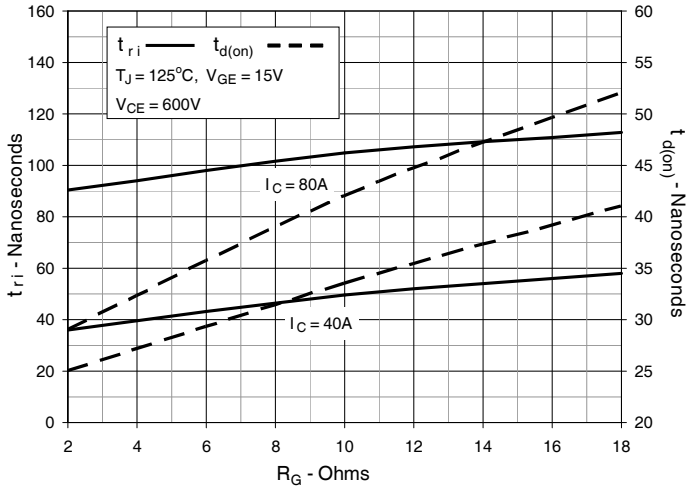


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

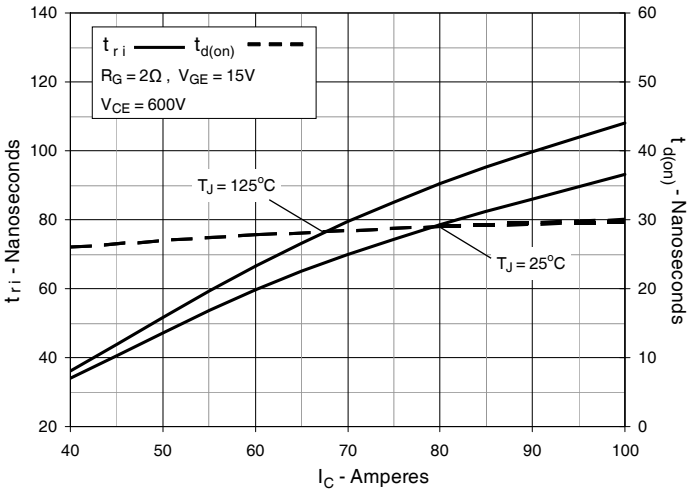


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature

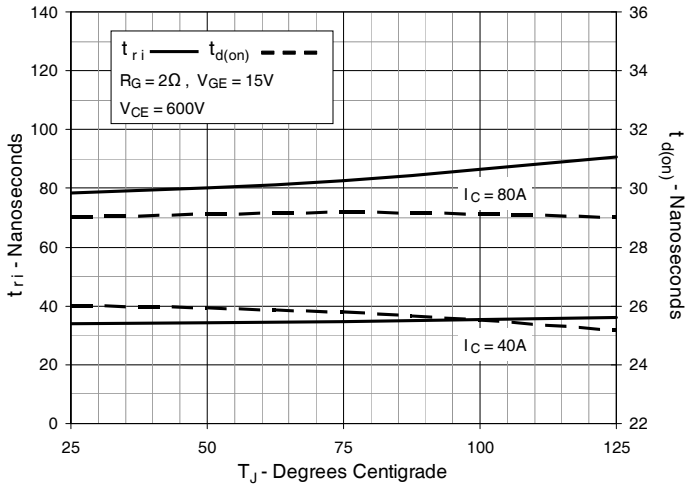


Fig. 21. Forward Characteristics

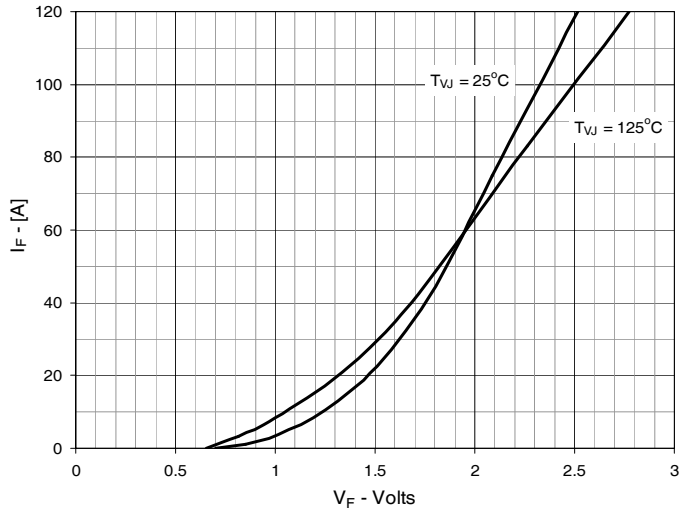


Fig. 22. Reverse Recovery Charge Q_{rr} vs. -di_F/dt

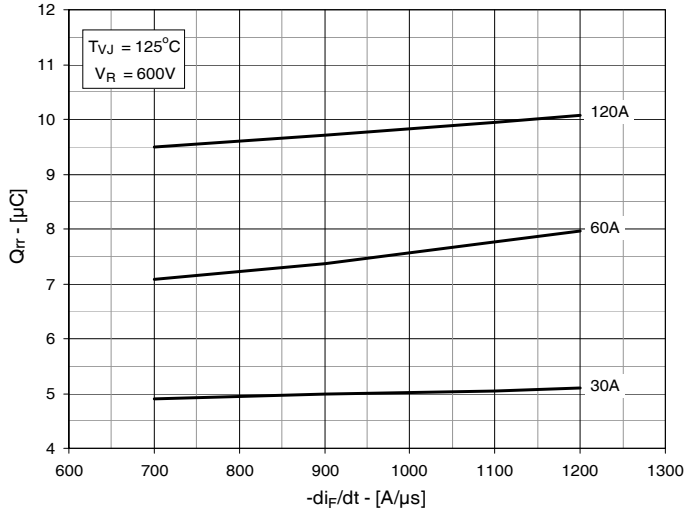


Fig. 23. PeakReverse Current I_{RM} vs. -di_F/dt

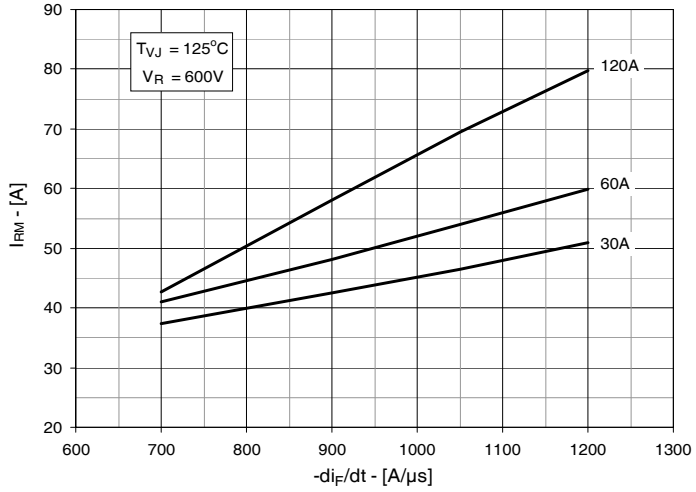


Fig. 24. Recovery Time t_{rr} vs. -di_F/dt

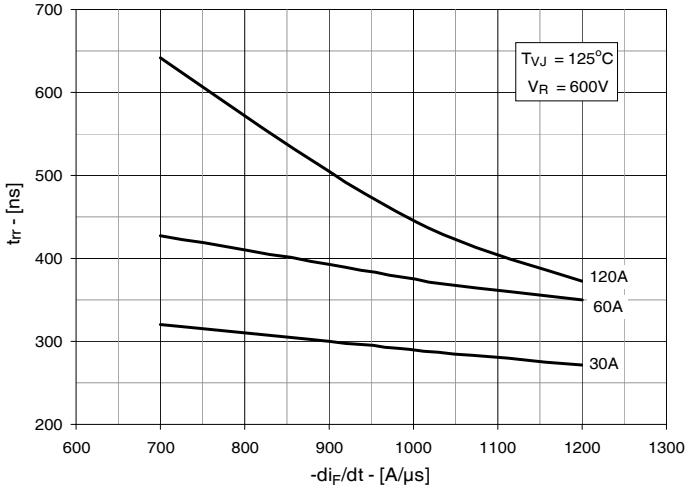


Fig. 25. Recovery Energy E_{rec} vs. -di_F/dt

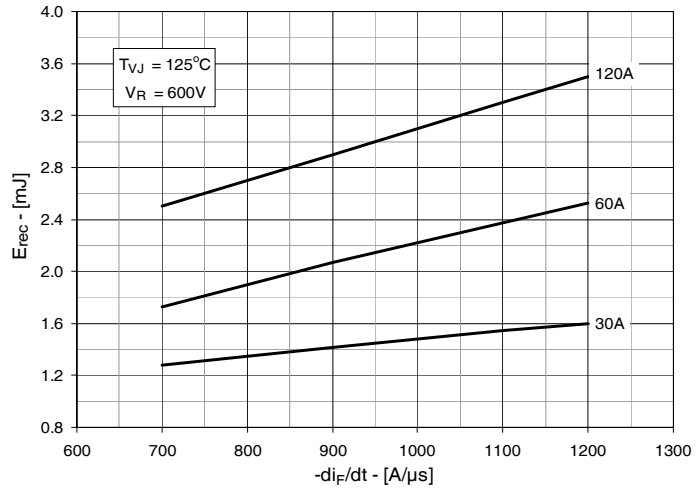
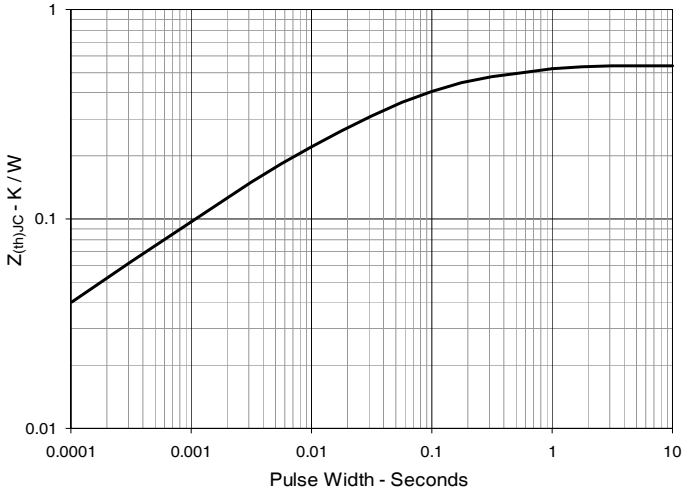
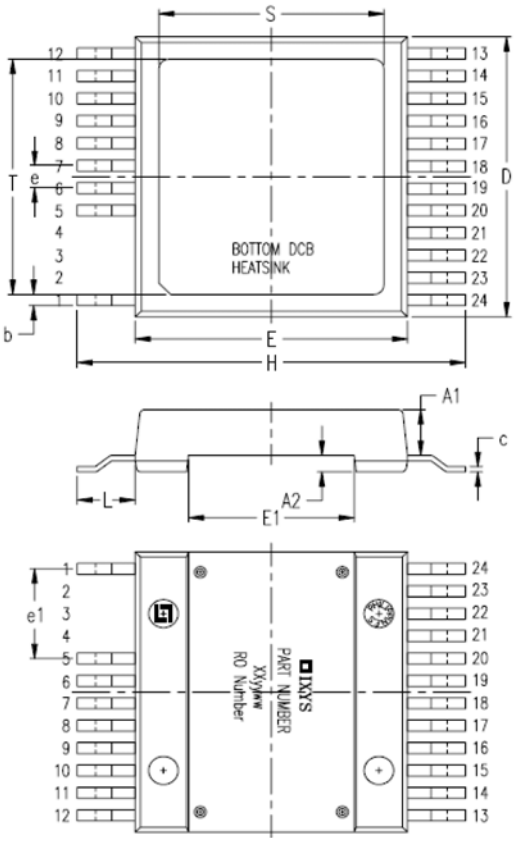


Fig. 26. Maximum Transient Thermal Impedance





SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

PIN: 1 = Gate
5-12 = Emitter
13-24 = Collector