Date:- 23rd Sept 2014

Data Sheet Issue:- 3

Phase Control Thyristor

Types N0416SC040 to N0416SC080

Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	400-800	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	400-800	V
V_{RRM}	Repetitive peak reverse voltage, (note 1)	400-800	V
V_{RSM}	Non-repetitive peak reverse voltage, (note 1)	500-900	V

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
$I_{T(AV)}$	Mean on-state current, T_{sink}=55°C, (note 2)	416	A
$I_{T(AV)}$	Mean on-state current. T_{sink}=85°C, (note 2)	274	A
$I_{T(RMS)}$	Nominal RMS on-state current, T_{sink}=25°C, (note 2)	840	A
$I_{T(d.c.)}$	D.C. on-state current, T_{sink}=25°C, (note 4)	685	A
I_{TSM}	Peak non-repetitive surge t_p=10ms, V_{RM}=0.6V_{RRM}, (note 5)	6000	A
I_{TSM2}	Peak non-repetitive surge t_p=10ms, $V_{RM}\leq$10V, (note 5)	6600	A
I^2t	I^2t capacity for fusing t_p=10ms, V_{RM}=0.6V_{RRM}, (note 5)	180×10^3	A^2s
I^2t	I^2t capacity for fusing t_p=10ms, $V_{RM}\leq$10V, (note 5)	218×10^3	A^2s
$(di/dt)_{cr}$	Maximum rate of rise of on-state current (repetitive), (Note 6)	500	A/µs
	Maximum rate of rise of on-state current (non-repetitive), (Note 6)	1000	A/µs
V_{FGM}	Peak forward gate voltage	18	V
V_{RGM}	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	2	W
P_{GM}	Peak forward gate power	100	W
V_{GD}	Non-trigger gate voltage, (Note 7)	0.25	V
T_{HS}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C

Notes:-
1) De-rating factor of 0.13% per °C is applicable for T_j below 25°C.
2) Double side cooled, single phase; 50Hz, 180° half-sinewave.
3) Single side cooled, single phase; 50Hz, 180° half-sinewave.
4) Double side cooled.
5) Half-sinewave, 125°C T_j initial.
6) V_D=67% V_{DRM}, I_{FG}=2A, $t_r\leq$0.5µs, T_{case}=125°C.
7) Rated V_{DRM}.

Characteristics

	PARAMETER	MIN.	TYP.	MAX.	TEST CONDITIONS (Note 1)	UNITS
V_{TM}	Maximum peak on-state voltage	-	-	1.22	I_{TM}=690A	V
V_{T0}	Threshold voltage	-	-	0.85		V
r_T	Slope resistance	-	-	0.535		mΩ
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	200	-	-	V_D=80% V_{DRM}	V/µs
I_{DRM}	Peak off-state current	-	-	20	Rated V_{DRM}	mA
I_{RRM}	Peak reverse current	-	-	20	Rated V_{RRM}	mA
V_{GT}	Gate trigger voltage	-	-	3.0	T_j=25°C	V
I_{GT}	Gate trigger current	-	-	150	T_j=25°C V_D=10V, I_T=3A	mA
I_H	Holding current	-	-	400	T_j=25°C	mA
R_{thJK}	Thermal resistance, junction to heatsink	-	-	0.12	Double side cooled	K/W
F	Mounting torque	24.5	-	27		kN
W_t	Weight	-	280	-		g

Notes:-
1) Unless otherwise indicated T_j=125°C.

Notes on Ratings and Characteristics

1.0 Voltage Grade Table

Voltage Grade	V_{DRM} V_{DSM} V_{RRM} V	V_{RSM} V	V_D V_R DC V
04	400	500	260
08	800	900	560

2.0 Extension of Voltage Grades

This report is applicable to other and higher voltage grades when supply has been agreed by Sales/Production.

3.0 Extension of Turn-off Time

This Report is applicable to other t_q/re-applied dv/dt combinations when supply has been agreed by Sales/Production.

4.0 Repetitive dv/dt

Higher dv/dt selections are available up to 1000V/µs on request.

5.0 De-rating Factor

A blocking voltage de-rating factor of 0.13%/°C is applicable to this device for T_j below 25°C.

6.0 Rate of rise of on-state current

The maximum un-primed rate of rise of on-state current must not exceed 1500A/µs at any time during turn-on on a non-repetitive basis. For repetitive performance, the on-state rate of rise of current must not exceed 1000A/µs at any time during turn-on. Note that these values of rate of rise of current apply to the total device current including that from any local snubber network.

7.0 Square wave ratings

These ratings are given for load component rate of rise of forward current of 100 and 500 A/µs.

8.0 Duty cycle lines

The 100% duty cycle is represented on all the ratings by a straight line. Other duties can be included as parallel to the first.

9.0 Maximum Operating Frequency

The maximum operating frequency is set by the on-state duty, the time required for the thyristor to turn off (t_q) and for the off-state voltage to reach full value (t_v), i.e.

$$f_{\max} = \frac{1}{t_{pulse} + t_q + t_v}$$

10.0 On-State Energy per Pulse Characteristics

These curves enable rapid estimation of device dissipation to be obtained for conditions not covered by the frequency ratings.

Let E_p be the Energy per pulse for a given current and pulse width, in joules
Let $R_{th(J-Hs)}$ be the steady-state d.c. thermal resistance (junction to sink)
and T_{SINK} be the heat sink temperature.

Then the average dissipation will be:

$$W_{AV} = E_P \cdot f \text{ and } T_{SINK(\max.)} = 125 - \left(W_{AV} \cdot R_{th(J-Hs)}\right)$$

11.0 Reverse Recovery Loss

11.1 Determination by Measurement

From waveforms of recovery current obtained from a high frequency shunt (see Note 1, Page 5) and reverse voltage present during recovery, an instantaneous reverse recovery loss waveform must be constructed. Let the area under this waveform be E joules per pulse. A new heat sink temperature can then be evaluated from:

$$T_{SINK(new)} = T_{SINK(original)} - E \cdot \left(k + f \cdot R_{th(J-Hs)}\right)$$

where k = 0.227 (°C/W)/s

E = Area under reverse loss waveform per pulse in joules (W.s.)
f = rated frequency Hz at the original heat sink temperature.
$R_{th(J-Hs)}$ = d.c. thermal resistance (°C/W).

The total dissipation is now given by:

$$W_{(TOT)} = W_{(original)} + E \cdot f$$

11.2 Determination without Measurement

In circumstances where it is not possible to measure voltage and current conditions, or for design purposes, the additional losses E in joules may be estimated as follows.

Let E be the value of energy per reverse cycle in joules (curves in Figure 9).
Let f be the operating frequency in Hz

$$T_{SINK(new)} = T_{SINK(original)} - \left(E \cdot R_{th} \cdot f\right)$$

Where $T_{SINK\ (new)}$ is the required maximum heat sink temperature and
$T_{SINK\ (original)}$ is the heat sink temperature given with the frequency ratings.

A suitable R-C snubber network is connected across the thyristor to restrict the transient reverse voltage to a peak value (V_{rm}) of 67% of the maximum grade. If a different grade is being used or V_{rm} is other than 67% of Grade, the reverse loss may be approximated by a pro rata adjustment of the maximum value obtained from the curves.

11.3 Reverse Recovery Loss by Measurement

This thyristor has a low reverse recovered charge and peak reverse recovery current. When measuring the charge care must be taken to ensure that:

(a) a.c. coupled devices such as current transformers are not affected by prior passage of high amplitude forward current.
(b) A suitable, polarised, clipping circuit must be connected to the input of the measuring oscilloscope to avoid overloading the internal amplifiers by the relatively high amplitude forward current signal
(c) Measurement of reverse recovery waveform should be carried out with an appropriate critically damped snubber, connected across diode anode to cathode. The formula used for the calculation of this snubber is shown below:

$$R^2 = 4 \cdot \frac{V_r}{C_S \cdot {}^{di}\!/_{dt}}$$

Where: V_r = Commutating source voltage
C_S = Snubber capacitance
R = Snubber resistance

12.0 Gate Drive

The recommended pulse gate drive is 30V, 15Ω with a short-circuit current rise time of not more than 0.5µs. This gate drive must be applied when using the full di/dt capability of the device.

The duration of pulse may need to be configured with respect to the application but should be no shorter than 20µs, otherwise an increase in pulse current could be needed to supply the resulting increase in charge to trigger.

Curves

Figure 1 - On-state characteristics of Limit device

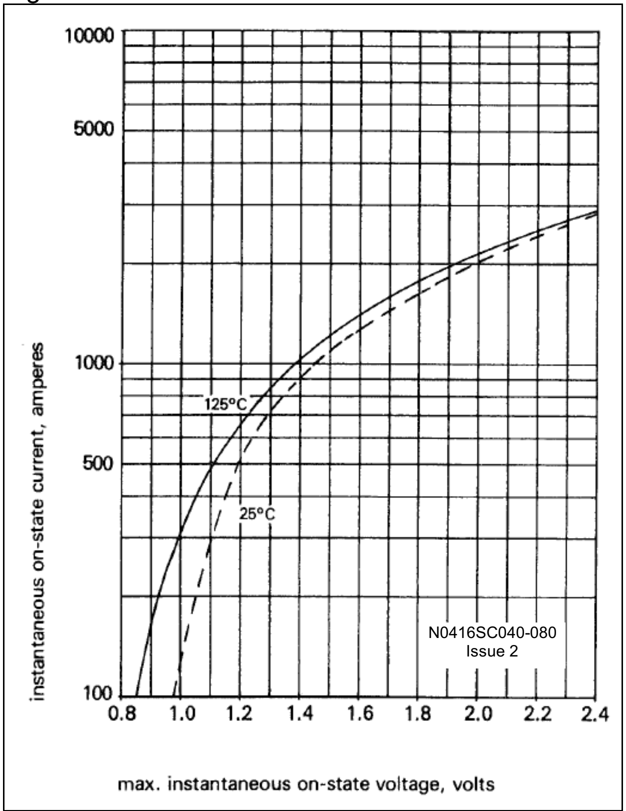

Figure 2 – Gate characteristics - Trigger limits

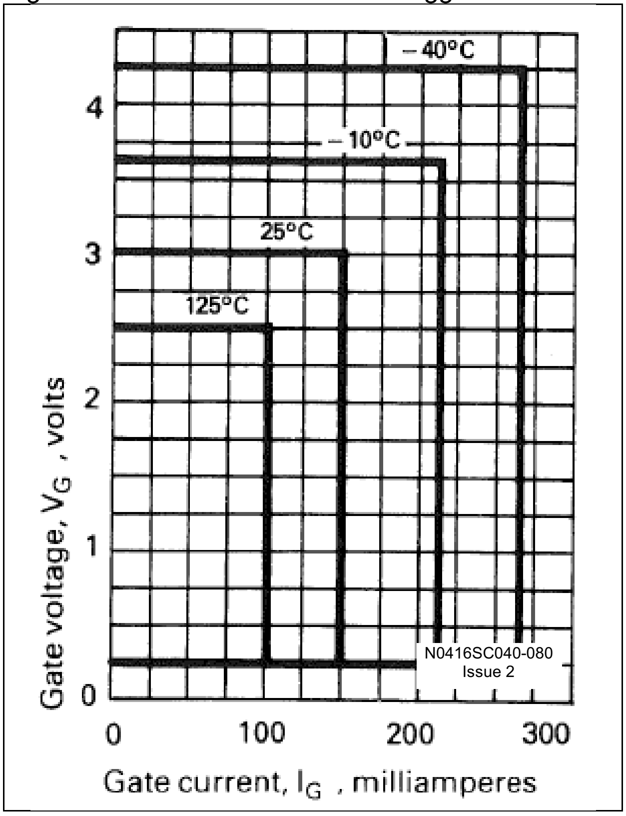

Figure 3 - Gate characteristics - Power curves

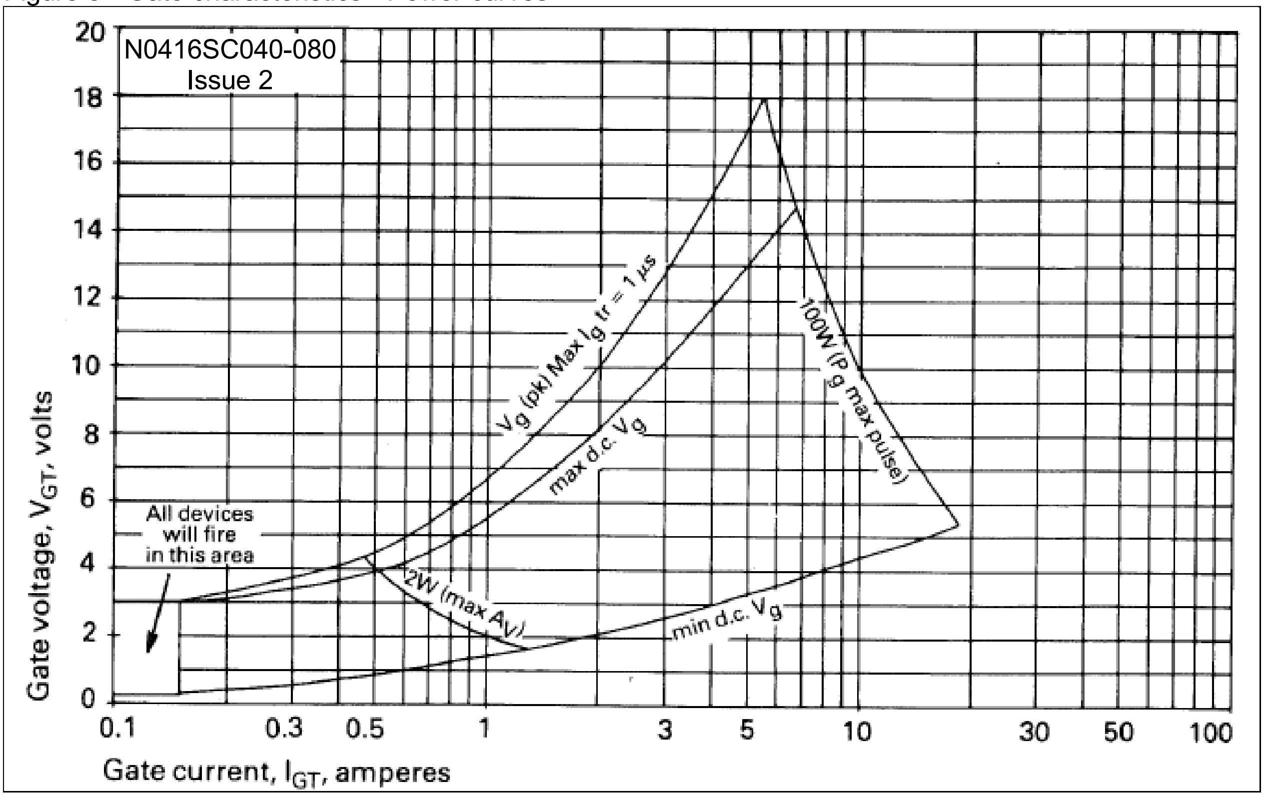

Figure 4 – Power dissipation and case temperature Vs. current – Square wave

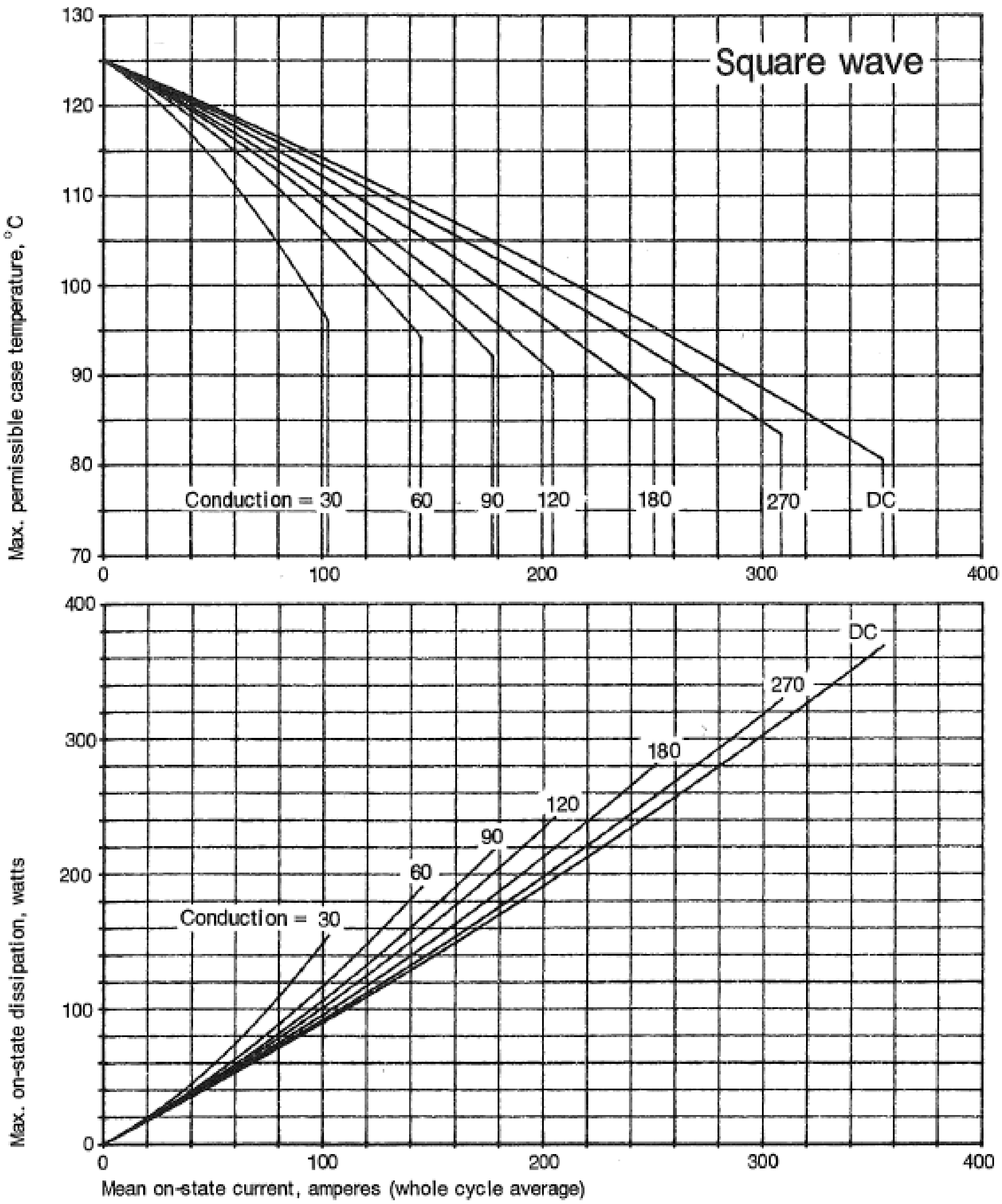

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Figure 5 – Power dissipation and case temperature Vs. current – Sine wave

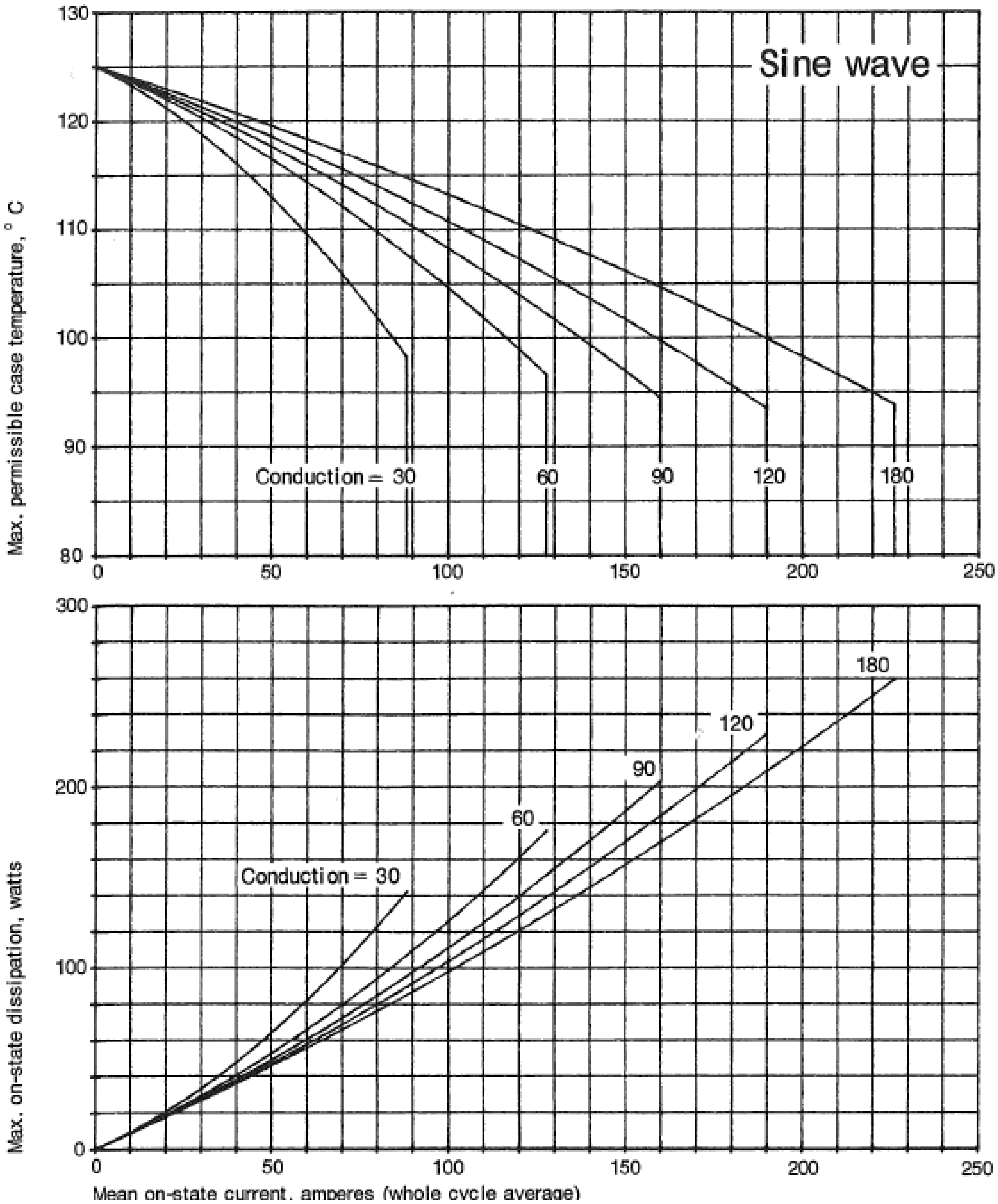

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Figure 6 – thermal resistance – Junction to case

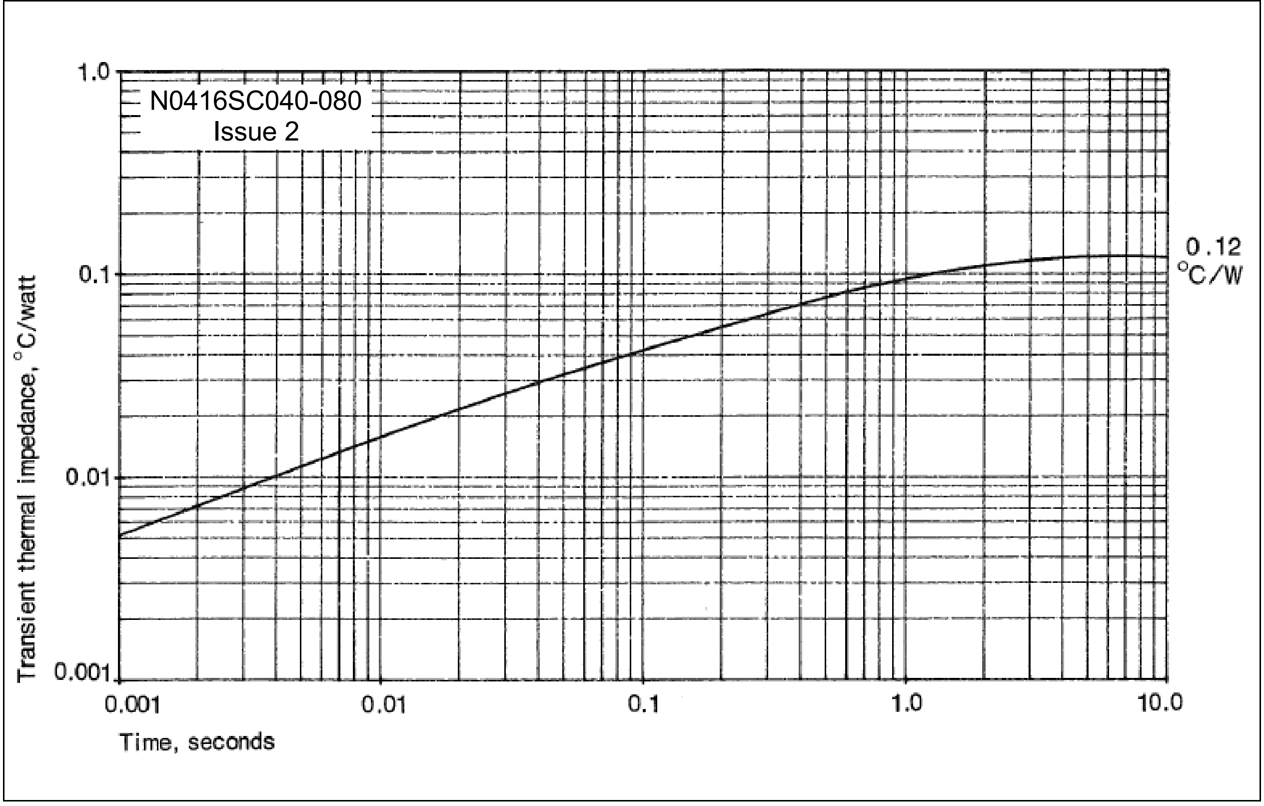
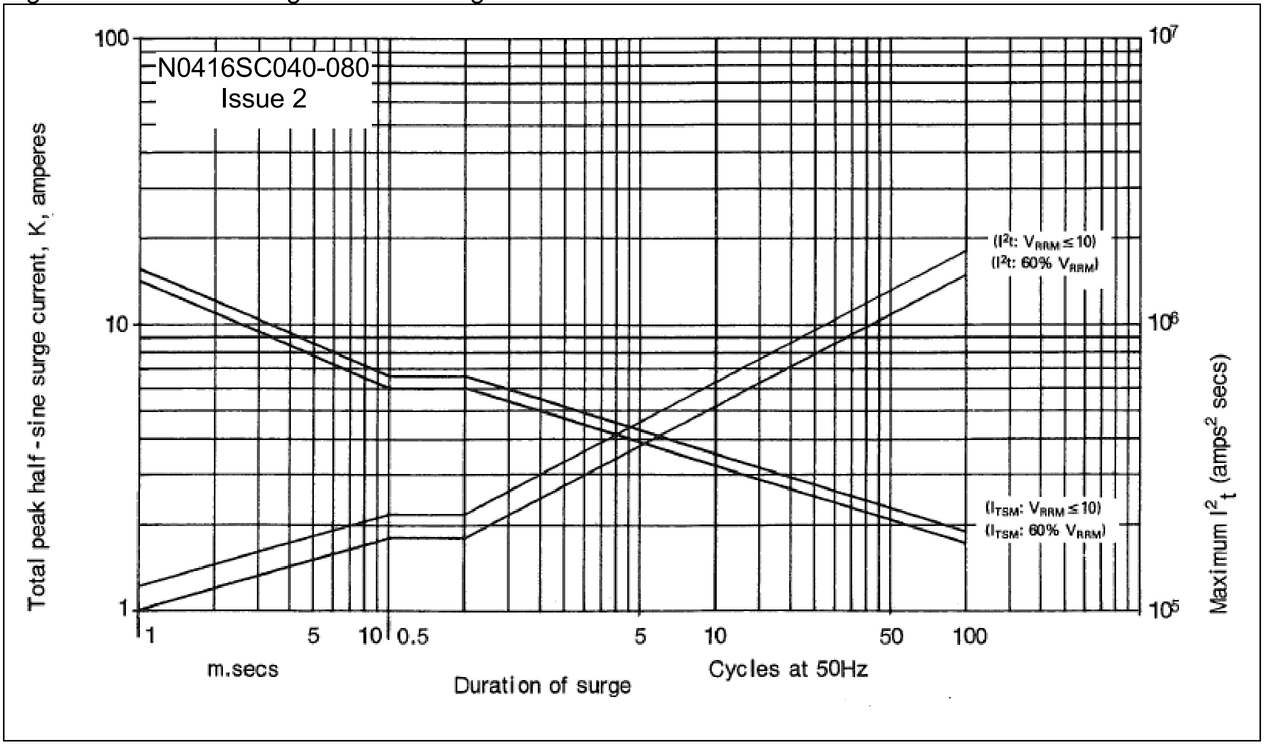
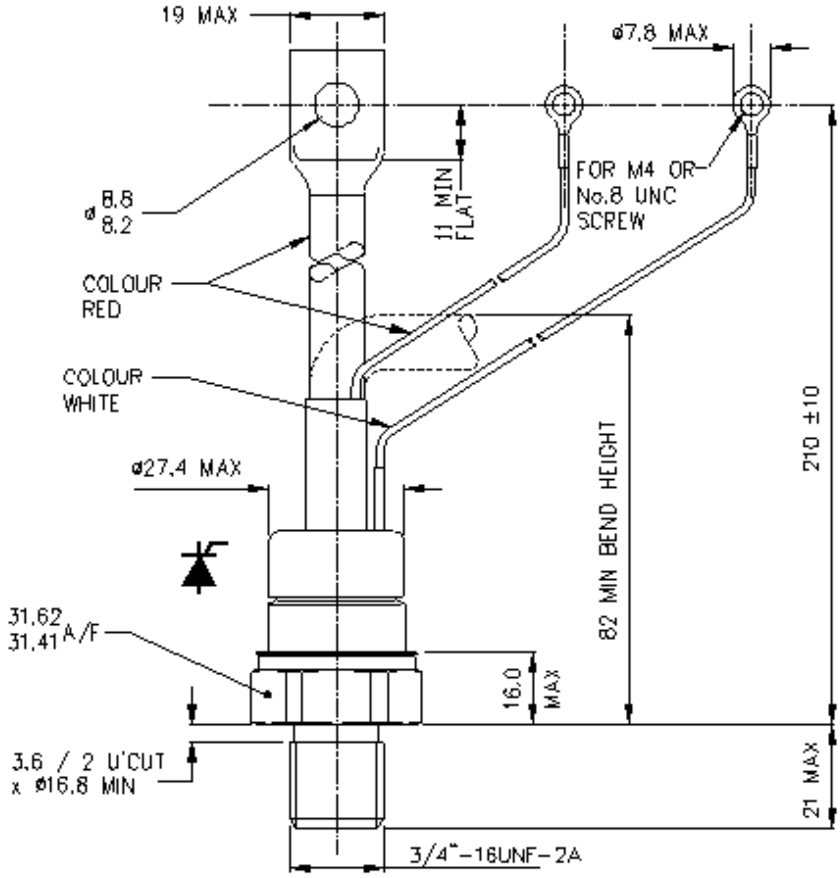


Figure 7 - Maximum surge and I^2t Ratings at initial T_J – 125°C



Outline Drawing & Ordering Information



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ORDERING INFORMATION (Please quote 10 digit code as below)

N0416	SC	♦♦	0
Fixed Type Code	Fixed Outline Code	Off-state Voltage Code V_{DRM}/100 04-08	Fixed Code

Typical order code: N0416SC040 – 400V V_{DRM} ¾" stud with lead

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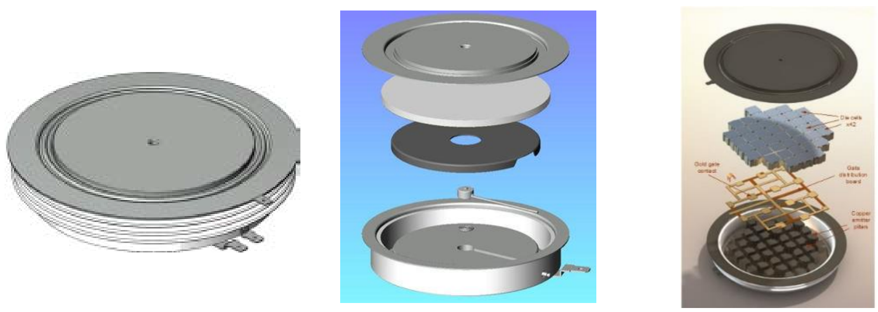
In the interest of product improvement, IXYS UK Westcode Ltd reserves the right to change specifications at any time without prior notice.

Devices with a suffix code (2-letter or letter/digit/letter combination) added to their generic code are not necessarily subject to the conditions and limits contained in this report.

Mounting and Handling Press-pack Semiconductor Devices

Objectives

This document outlines the minimum mounting conditions for Littelfuse high power devices along with instructions to achieve proper mounting. Press-pack devices are divided into two groups. GTOs, diodes, and thyristors share a common internal construction, while IGBTs are built using a different approach. **Figure 1** briefly highlights the differences.



(a) Disc-shaped device (b) Internal construction scheme for bipolar types (c) Internal construction scheme for IGBT types

Figure 1. Differences between the Press-pack Technologies

Disc devices containing thyristors, diodes, GTOs, or IGBTs are often stacked to support dedicated demands and set up the desired topology. This mounting technology requires precise alignment and careful handling of the power semiconductors as well as sophisticated mechanical construction. The most important factor in stacked assemblies is a homogeneous distribution of mounting forces.

Applications

- High-power motor drives, Medium-Voltage drives, Soft-starters
- Welding, Induction Melting, and Electro-chemical power supplies
- Static Synchronous Compensators (STATCOM) and HVDC-based power transmission
- Rail, Marine, and Mining transportation
- Renewable energies – Wind and Solar power

Target Audience

This document is intended for potential adopters of high-power semiconductors who want to determine the appropriate mounting and handling to ensure proper electrical and thermal performance as well as achieving a reliable mechanical situation.

Contact Information

For more information on this topic, contact the Littelfuse Power Semiconductor team of product and applications experts:

- North America – NA_PowerSemi_Tech@Littelfuse.com
- Central & South America – CSA_PowerSemi_Tech@Littelfuse.com
- Europe. Middle East, & Africa – EMEA_PowerSemi_Tech@Littelfuse.com
- Asia, Australia, & Pacific Islands – APAC_PowerSemi_Tech@Littelfuse.com

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1. Introduction

High-power semiconductors appear to be robust and durable parts at first sight. Despite this robust appearance and the high forces applied to the components during mounting, care must be taken to assemble the components in a suitable manner. Major factors for a successful design include the treatment of all contact surfaces involved, the thermal management, and a mechanical construction that leads to a homogeneous pressure distribution.

2. Disc Devices

As the name implies, disc devices are of circular shape. The housing consists of cylindrical ceramic; upper and lower covers are made from metal and act as electrical contacts to the semiconductor inside. Diodes in this package only feature the power terminals while thyristors, IGBTs, or GTOs have additional terminals for control. A schematical overview is given in **Figure 2**.

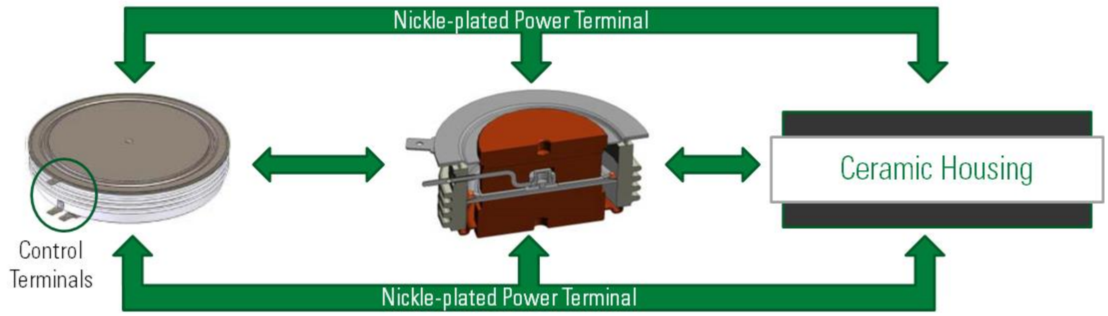


Figure 2. Schematical Overview of Disc Devices, Internal Construction, and Simplified Representation

In contrast to power modules with screw-type terminals, disc devices are contacted purely by pressure which is why they are also referred to as press-packs or capsule types.

2.1. Surface Requirements when Mounting Disc Devices

When using disc devices, the contact area fulfills two functions. It acts as an electrical contact to carry current and at the same time carries the thermal energy to allow proper cooling. As the contact area's partner can be both, heat sink and bus bar at the same time, it is important that these interfaces maintain a stable contact throughout the lifetime of the equipment to ensure reliable operation of the device. Both, the surface geometry, and the surface finish are important factors to be considered. For ease of understanding, heat sink or busbars are considered contact blocks throughout the remaining document. To ensure a low value of thermal resistance, the contact surface of the contact block must be flat, even, and clean. For the mounting area, the surface quality must achieve or exceed the values given in **Figure 3**.

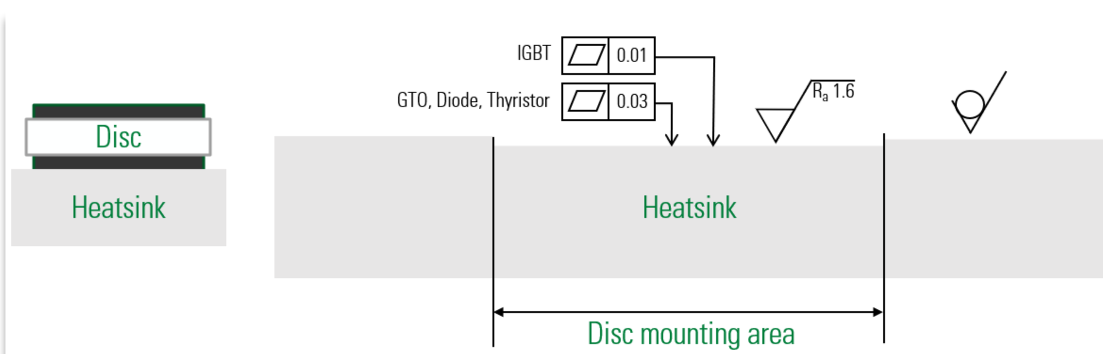


Figure 3. Contact Block Surface Requirements to Mount a Disc Device

In case the contact block is mounted between two discs, the contact surfaces on both sides must achieve parallelism as sketched in **Figure 4**.

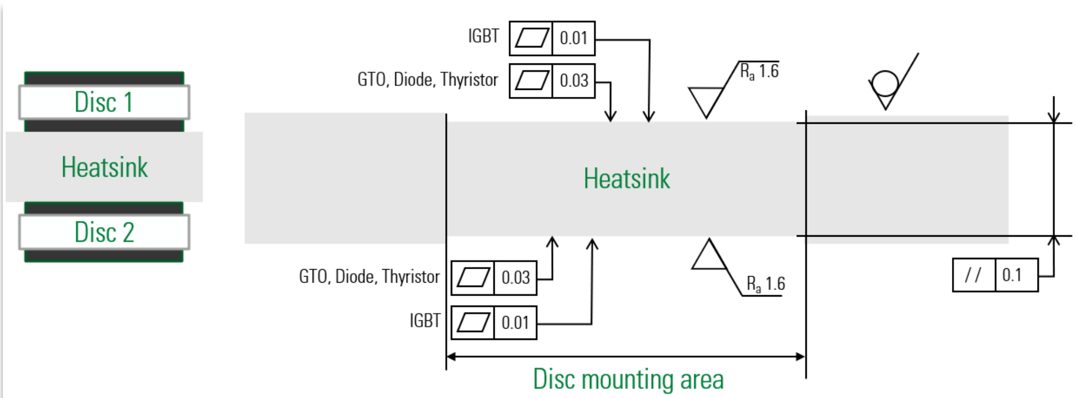


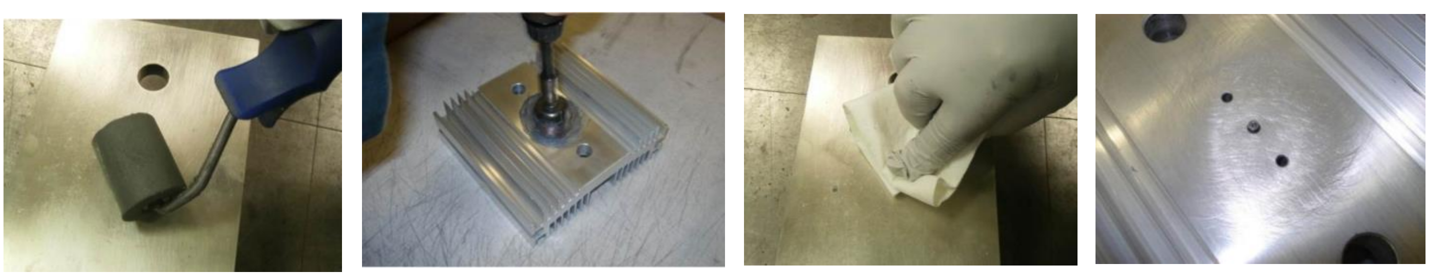
Figure 4. Contact Block Requirements When Discs are Mounted on Both Sides

Measuring the flatness of an IGBT's surface in unmounted condition may return values that exceed those specified when being clamped. This is expected because of the component's assembly technology and processes. In no way does this reflect or impact the device flatness once it is clamped to the nominal force.

It is also important to ensure that all components in a stack deform only elastically. A flatness exceeding the maximum specified may result if plastic deformation of the contact surfaces occurs under loading. One example where such effects can potentially be observed is a local collapse of heat sinks. Loss of reliability or lifetime can be a consequence of such an effect.

2.2. Surface Treatment

All contact surfaces should be clean and dry prior to assembly. If necessary, non-plated contact surfaces like these from extruded aluminum heat sinks should be lightly abraded to remove oxide films. A proper tool to do so is a rotary wire brush equipped with a suitable contact grease like Jet-Lube SCX13 to form a slurry. Note that the slurry produced by the abrasion should be left on the contact surface until the device is ready to be mounted. This helps to prevent oxidation of the surfaces. Alternatively, polishing the surfaces using 3M Scotch-Brite™ or a similar product can be considered. Right before conflating, the contact surfaces should be cleaned using ethanol or a similar solvent and a lint free cloth. The different steps of this procedure are depicted in **Figure 5**.



(a) Contact grease is applied to the surface sparingly | **(b) Abrasion of the heatsink using contact grease and rotating wire brush** | **(c) Cleaning the surface right before mounting the disc** | **(d) Mounting surface, lightly abraded**

Figure 5. Surface Preparation Sequence

Regarding the power semiconductor or heat sinks with plated surfaces, no further mechanical preparation is required. Cleaning with a suitable cleaning agent prior to mounting is advised to make sure that no particles remain on the surface.

In order to maintain a good electrical connection and avoid corrosion over time, Littelfuse recommends that all non-aluminum contact surfaces be nickel-plated. Chemical plating is preferable to electroplating in high reliability applications. Plating thickness should be 4-6 µm in accordance with that applied to the device or module.

Prior to mounting, a tiny amount of contact grease is applied to the power terminals of the press-pack homogeneously. In contrast to modules with isolated base plates, this grease must enhance the transfer of thermal energy but may not hinder electric current to flow. Therefore, materials like Jet-Lube SCX13 with metallic particles are used. With some experience, the application can be done with a rubber-roller, as depicted in **Figure 6**.

(a) Applying a very small amount of contact grease with a roller

(b) The result is a very thin, homogeneous layer

Figure 6. Applying Contact Grease by Roller and Inspection of the Result

Once the mounting force is applied, only the material necessary to fill microscopic gaps between the contact surfaces remains. Excess material is pressed out and forms a small bead around the semiconductor's perimeter. To get familiar with the process and gather experience, unmounting the disc can be done to inspect the result.

The mounting area should appear almost clean and a small bead with a line width of about 0.1 mm should remain, as seen in **Figure 7**.

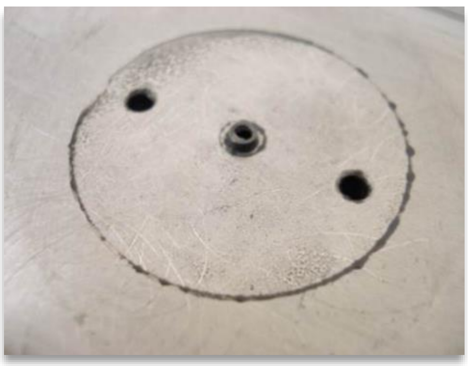


Figure 7. View After Unmounting the Device. A Bead Remains While Mounting Area Appears Almost Clean

Important: This inspection is just to get familiar with the process. Once the device was removed from the heat sink, thorough cleaning of the contact surfaces is mandatory and new contact grease needs to be applied. Putting the device back in place after unmounting is not recommended!

2.3. Applying the Assembly Force

It is mandatory, yet not trivial, to set up a mechanical fixture that applies the necessary mounting force and achieves a homogeneous distribution at the same time. Littelfuse offers a variety of proven clamp systems to support the construction of high-power semiconductor applications. Size and shape depend on the individual requirements of the application, the size of the component in use, and how many components need to be combined. Common ground for all the designs is the target of applying a proper force and spreading it to the semiconductors in a suitable manner.

The force must be applied perpendicular to the semiconductor's surface. In theory, an even distribution is achieved by applying the force to a single point aligned with the center line of the semiconductor and using suitable mechanical means to spread the force to the available contact area. A schematical overview is seen in **Figure 8**.

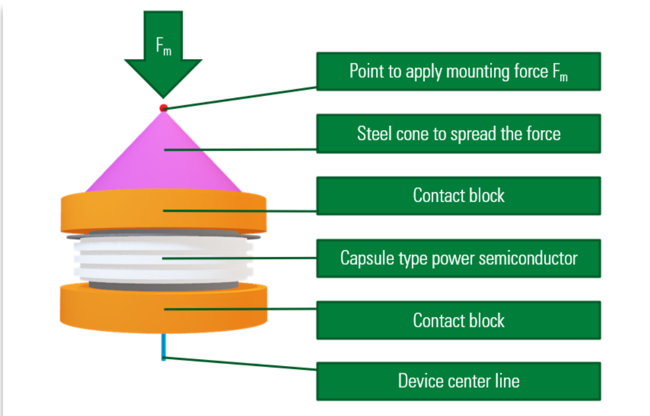
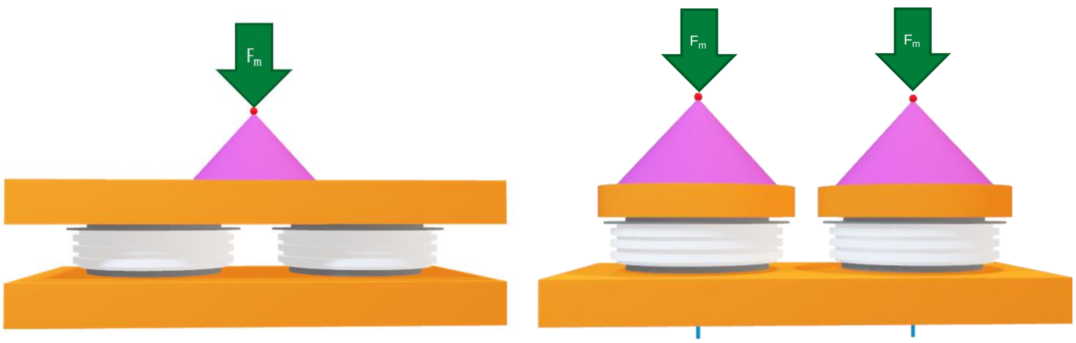


Figure 8. Spreading the Mounting Force to Uniform Distribution

To properly spread the applied force, the cone's diameter must match the semiconductor's diameter and the point angle must not exceed 90°.

2.3.1. Side-by-side Mounting

Depending on the topology to be built, either parallel or anti-parallel connection of power semiconductors may be necessary. Slight variations in the components' dimensions due to tolerances might lead to unnecessary mechanical stress if two devices are clamped using a single bracket. When combining devices with different height dimensions, spacers would be needed to achieve parallel arrangements which would make the design unnecessarily complex. **Figure 9(a)** holds an example where tilting angles due to different dimensions can lead to high mechanical stress to the disc's rims. **Figure 9(b)** displays an illustration with the preferred setup that inherently decouples the mounting forces and is also well-suited to combine devices with different geometries.



(a) Poor layout for side-by-side mounting
(b) Preferred layout for side-by-side mounting

Figure 9. Mounting Two Devices Side-by-side on a Common Carrier

2.3.2. Stacking Disc Devices

In high-power applications, it is very common to stack devices either to form the desired topology or to achieve higher blocking voltages. As an example, the image in **Figure 10** represents a diode arrangement, capable of blocking 90 kV. Due to specific application requirements, no heat sinks are needed in this design.

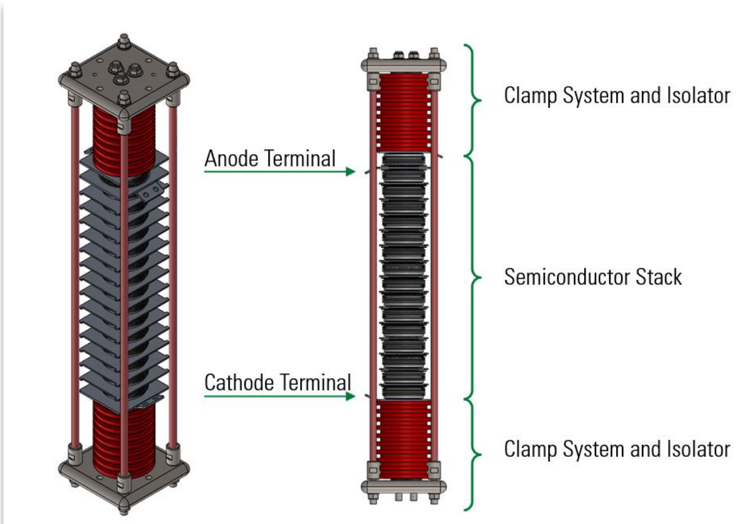


Figure 10. Stacked Diode Arrangement Using Littelfuse Clamping System

Stacks formed from more than just two devices required special attention during construction and assembly. Stacking several identical devices as in the given example is the most basic approach. When combining different devices, their mounting forces must be compatible. This prevents single devices from being overstressed or receiving an unsuitable low pressure. It is also favorable if the diameters of all press-packs involved are in a similar range. During assembly, the mounting direction of the discs is defined by the topology to be built. Attention needs to be paid to mount the discs with the correct orientation.

To facilitate the center alignment, press-packs feature centering holes on both the power terminals. In combination with a corresponding pin, this can be used to precisely align the devices to their central axes. Mechanical holders that align the discs during assembly can also be considered.

As the exploded view in **Figure 11** demonstrates, Littelfuse can supply kits, parts, and complete assemblies to speed up development of stacks.

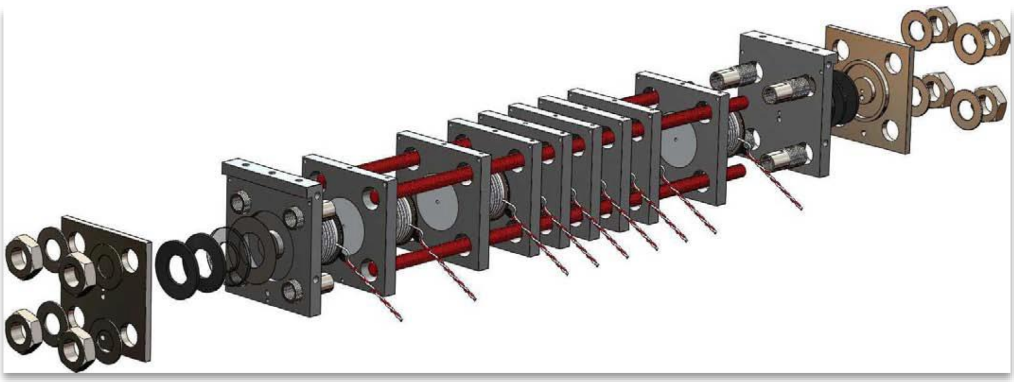


Figure 11. Clamps, Rods, Heatsinks, and other Mechanical Components for Stack-Assemblies

2.3.3. Design Verification

A homogeneous pressure distribution is a mandatory prerequisite when mounting disc devices as uneven distribution leads to accelerated aging of the components with a risk of premature failure. The pressure distribution is a consequence of properly designing and assembling the stack. As it cannot be measured or monitored in every stack, the mounting procedure and the stack's clamp system need to be defined in a way that ensures a suitable result by design.

A verification of the design needs to be done by monitoring the pressure in a fully assembled system. There are two potential methods of achieving a robust statement regarding pressure distribution.

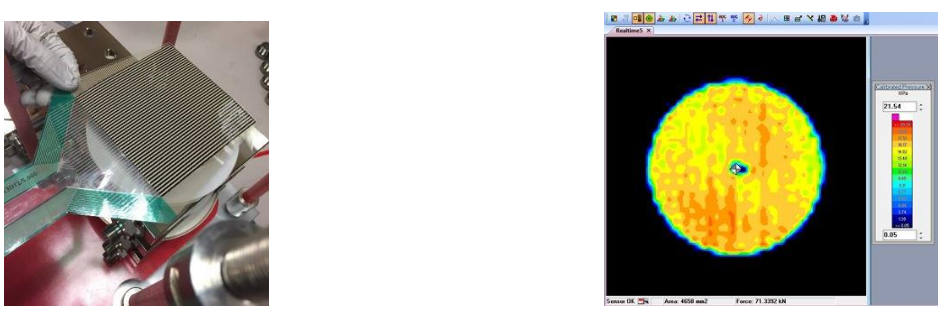
Littelfuse recommends the use of Fuji Prescale film or a similar film product to confirm the pressure uniformity. These films are available in several different pressure ranges and should be inserted between the semiconductor device and the corresponding contact block. Once pressure is applied to an area of the film, the material irreversibly changes color to indicate the local pressure.

The pressure distribution achieved with a given setup can be judged by disassembling the stack and inspecting the film. Uniform color change signals uniform pressure. A suitable pressure distribution and a non-uniform result are summarized in **Figure 12(a)** and **Figure 12(b)** respectively.

(a) Exemplary results showing uniform pressure distribution **(b) Poor results, revealing highly non-uniform pressure distribution**

Figure 12. Results from Inspecting Pressure Distribution Using Color-Changing Film

The second option is to use pressure sensitive electrical sensor arrays. These consist of a matrix of pressure-sensitive resistors that can be measured by dedicated equipment. The result is displayed as a color-map. In contrast to the irreversible color change of the film, these sensors allow monitoring in real-time and can be reused. A common sensor and a typical result from such a measurement are included in **Figure 13**.



(a) Sensor Matrix gets inserted between devices **(b) Dedicated software enables visualizing the captured data**

Figure 13. Piezo-electric, Tactile Pressure Sensor, and Captured Results

Both the sensor types need to be removed from the stack as they would prevent proper electric function. As this comes with releasing the pressure in the assembly, re-applying the force after removing the sensor is necessary. The result demonstrated by the measurement can substantiate that the chosen assembly technique reproducibly leads to the correct magnitude of force and to homogeneous pressure distribution.

2.4. Isolation Coordination

High-power applications typically come with high voltages, making isolation coordination an important issue in protecting hardware and people. Clearance and creepage distances for high voltages need to be considered. Correlating information can be derived from the relevant standards, particularly IEC 60664-1 and UL840.

2.5. Thermal Management Details

The power sections built by disc devices typically reach outstanding efficiency values. Given the amount of energy handled, the absolute value of losses that appear require proper considerations. In general, three types of use-cases can be identified:

- Pulse power applications where energy is handled in a time frame well below a single second. In these cases, the thermal capacity of the material involved may be large enough to absorb the thermal energy without exceeding the technological limits. If so, additional heat sinks turn out to be obsolete.
- Assemblies that need to dissipate a moderate amount of heat which can be done by forced air cooling using extruded aluminum heat sinks.
- Challenging applications with restrictive power-density requirements that can only dissipate the heat with advanced liquid cooling systems.

With press-packs, the cooling systems inevitably makes galvanic contact with electrically life parts. To prevent malfunction or even catastrophic failure, it is important to ensure galvanic connectivity is only present where device terminals share a common voltage node within the intended circuit. Particularly in liquid cooling, cold plates are mounted between the electronic devices. Electrically, each cold plate has a different voltage level while all of them are connected by sharing the same cooling liquid, as sketched in **Figure 14**.

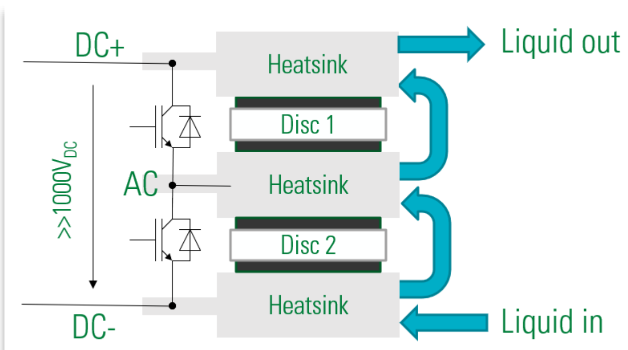


Figure 14. Basic Two-Level Phase Leg with Liquid Cooling

The use of a common cooling liquid requires that neither the cooling liquid itself nor the tubes in use may be electrically conductive. A suitable setup can be achieved using plastic tubes instead of metal parts and a mixture of 80% de-ionized water and 20% glycol ethylene as a cooling liquid. For the same reason, grounding the heat sinks is not an option!

3. Conclusion

Disc–, capsule– or press-pack-devices are key components in high-power electronics in a broad spectrum of applications and use cases. Despite their robust appearance, these components are challenging in terms of handling and mounting. Building and verifying a power section based on disc devices can best be done by applying proven mechanical concepts and components. Mastering the mechanical, thermal, and electrical challenges is a prerequisite to achieving long-lasting, reliable, and efficient designs. As there are plenty of standardized solutions for different applications that potentially can be customized to particular needs, a primary evaluation should consider whether acquiring a ready-made system solution could be the better option.

For additional information please visit www.Littelfuse.com/powersemi

Date:- 14th September, 2018

Issue: 1

An application note on wearout failure mechanisms

In general, the overall reliability of power semiconductor devices is represented by the “bathtub” curve shown in figure 1. The wearout phase of a device is linked to the general accumulation of physical damage under the operating load conditions in the application. The main changes in the properties of the device are linked to mechanical wear out due to the differences in the thermal expansion coefficients of the components in the housing. The surface of the die can show significant “scrubbing” due to expansion and contraction of the components. The scrubbing may lead to the formation of intermetallic compounds at these component interfaces as shown in figures 2-4. The build-up can then lead to changes in the on-state, V_T or forward voltage, V_F characteristic and in addition changes in the junction leakage current over long periods of time.

It is difficult to provide actual quantitative values to the X axis as this will depend very much on the conditions in the application. However, for many applications it is prudent to consider a refurbishment program after around thirty years’ service.

Generally, it is not good practice to remove a device from an assembly and then re-mount that device back into the same assembly using the same components. The device is unlikely to be re-located in exactly the same orientation in the clamp assembly, so the contact of the components is likely to be compromised due to the extended time in service.

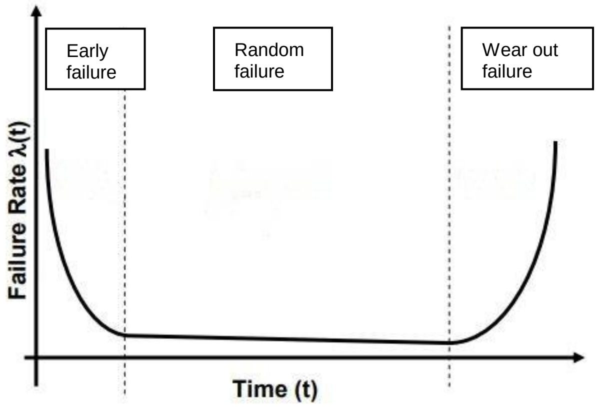


Figure 1: Typical “bathtub” curve

Figure 2: Initial evidence of thermal cycling scrubbing at the edge on the cathode contact area

Figure 3: Initial evidence of thermal cycling scrubbing on the anode molybdenum contact

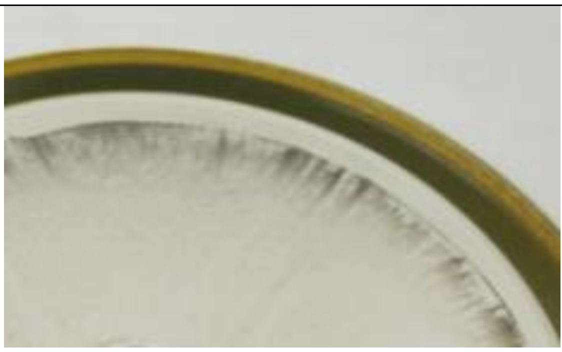


Figure 4: More extensive evidence of thermal cycling scrubbing at the edge on the cathode contact area

Date: 1st August 2017

Issue: 3

Application note for the use of a rectifier diode above $T_{j(max)}$ with a short term overload

Introduction

In many applications, semiconductor converters are subject to infrequent short-term overload periods. In order to make efficient use of the semiconductor device it is possible to consider a short term increase in junction temperature above $T_{j(max)}$ but at a reduced voltage.

Rectifier diode operation at an elevated temperature

Silicon rectifier diode characteristics are temperature dependant to some degree. For a modest increase in junction temperature many of these characteristics are of little consequence in line frequency converters.

Above the rated maximum junction temperature, $T_{j(max)}$ the reverse leakage current, I_{RRM} will approximately double for every 10°C rise above $T_{j(max)}$ as shown in figure 1. As the leakage current increases the power dissipation within the diode will increase and the potential for hot spots to form in the silicon could increase significantly. This mechanism could ultimately lead to component failure.

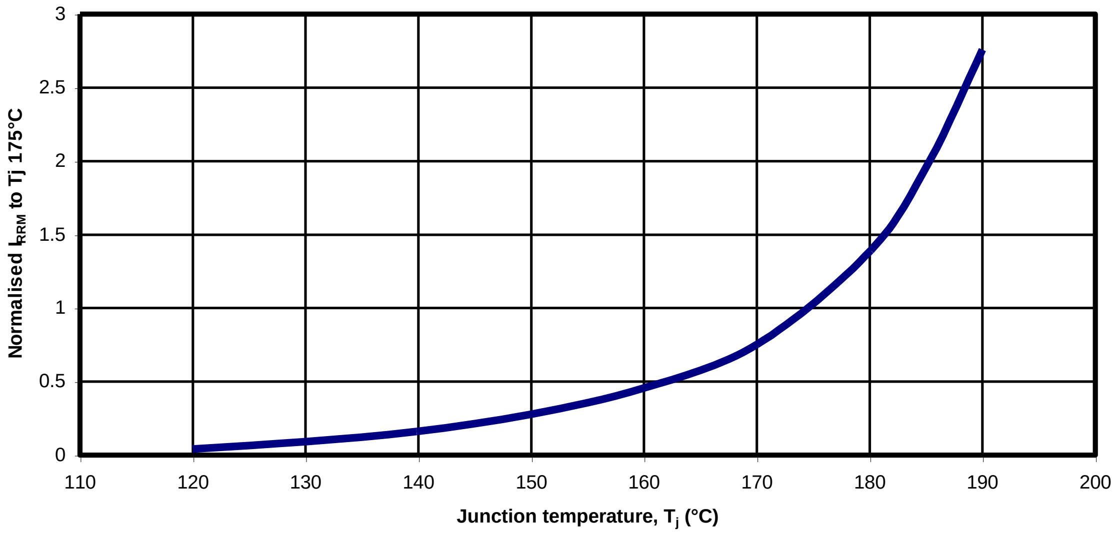


Figure 1: Normalised I_{RRM} vs Tj

In the majority of applications however there is a significant margin between the device rating and the applied working voltage. This is required to allow for transients induced by commutation and network disturbances.

It can be seen in figure 2 that the leakage current typically halves for a 20% drop in the applied voltage.

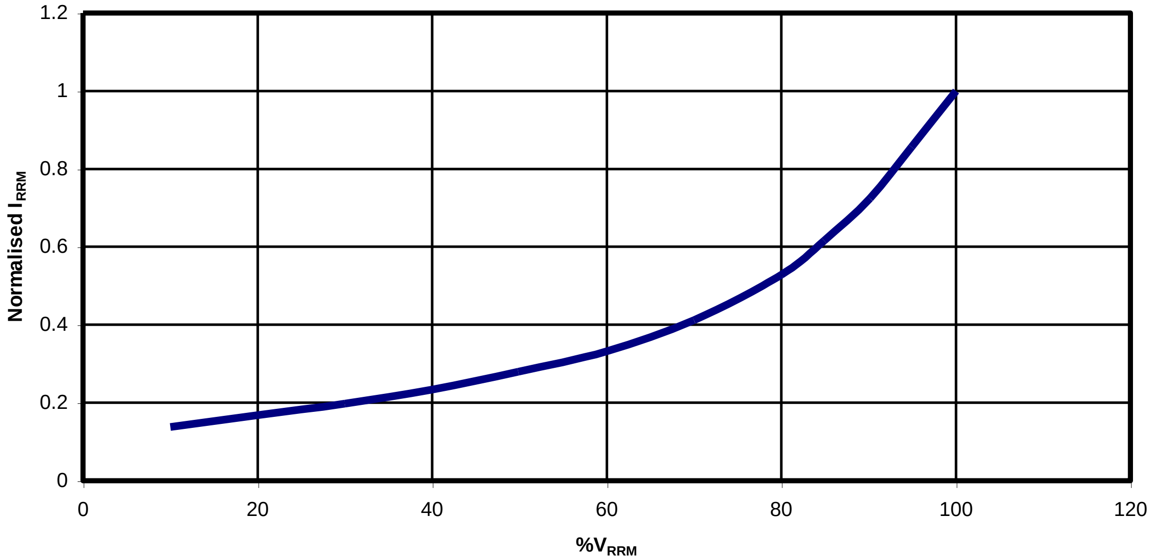


Figure 2: Normalised I_{RRM} vs % applied voltage

It is therefore reasonable to assume that in such applications it may be permissible to operate at an elevated junction temperature for a short period of time.

Designs in which the junction temperature of up to 15°C beyond the maximum rated value of T_j for transient operation with a maximum working peak voltage of 60% of the device rating have been successfully implemented. The transient overload period is limited by the thermal stability of the blocking junction and will vary according to cooling conditions and individual device geometry. Typically overloads up to 60 seconds are acceptable for all IXYS UK Westcode line frequency rectifiers.

It should be noted that during an overload period it may be appropriate to use the transient thermal impedance curve to calculate the increase in junction temperature. To demonstrate a graph of forward current and junction temperature vs time is shown in figure 3. The diode is conducting 5000A DC and the junction temperature is calculated at $T_{j(max)}$ using the steady state thermal resistance value. During this time a series of overload events takes place and the temperature increase is reflected using the transient thermal impedance curve. Information relating to the transient thermal impedances can be found in the data sheets.

For very short overload periods a much higher junction temperature is possible. Under typical limit surge conditions the device junction temperature may exceed 350°C. Please refer to the individual device data sheets for more information relating to surge events.

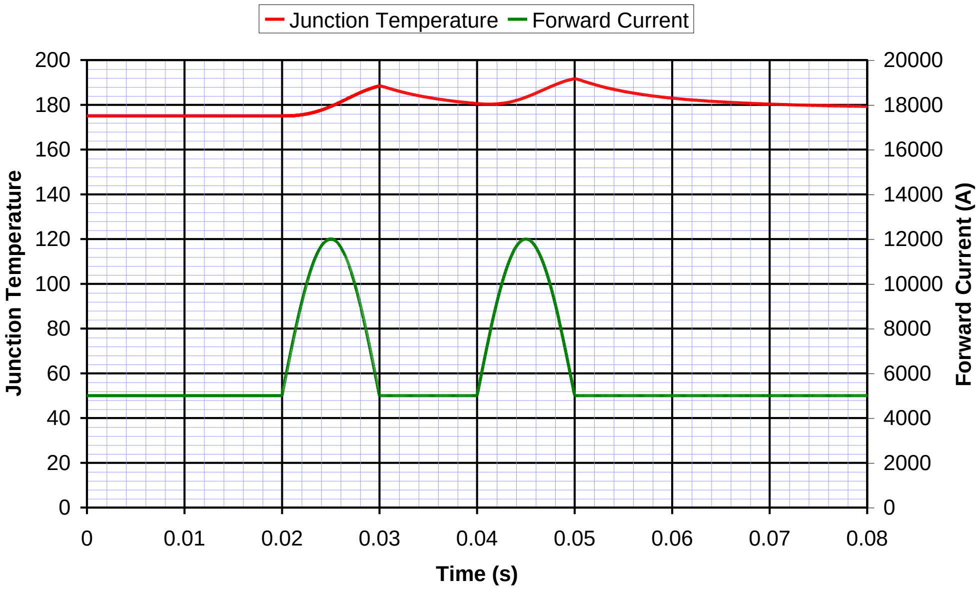


Figure 3: Forward current, junction temperature vs time under overload conditions

Precautions

Other device characteristics will be affected by increasing the T_j beyond that specified in the datasheet, in particular:

1. Increased recovered charge of typically 10% of Q_{rr} per 15°C. This increase must be factored into any snubber design.
2. A shift in the on state characteristics, specifically a small reduction in V_{T0} and a small increase in R_T. This shift could be as much as 5% per 15°C.

Other characteristics such a forward recovery voltage, V_{FR} could be affected but these parameters are less likely to be significant in typical rectifier applications.

One final point to consider is that of thermal cycling load. Operation of a diode with a large temperature deviation (ΔT) is likely to accelerate the mechanical wear out of the internal components and could lead to a reduction in the useful life of the diode. Again it is unlikely that this will present as an issue, but it may warrant investigation.

Summary

The application of rectifier diodes with a junction temperature of 15°C beyond the maximum rated value for transient operation of with an upper limit working peak voltage of 60% of rating has been successfully achieved. The transient overload period is limited by the thermal stability of the blocking junction and will vary according to cooling conditions and individual device geometry. Typically overloads up to 60 seconds are acceptable for all IXYS UK Westcode line frequency rectifiers.

The effects of the increased temperature on the various parameters have been briefly outlined.

It should be noted that the customer must be satisfied as to the suitability of this approach in the specific application.

Disclaimer

The guidance given herein is provided for information only and IXYS UK Westcode in no way implies any warranty for devices operated outside of the maximum ratings as specified in the datasheet.

Any application of devices beyond maximum ratings should be thoroughly qualified and validated on an individual basis.

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Date: 1st October 2015

Issue: 2

An application note for stocking and handling requirements of press pack devices and pressure contacted modules

Stocking and handling requirements

IXYS UK Westcode recommends that devices and assemblies be stocked in their original packaging if possible. The devices and assemblies should be stored within the temperature range specified in the data sheet. Storage in conditions of very high humidity of greater than 95%RH for long periods should be avoided. The primary pack boxes should not be stacked more than five boxes high.

Press pack devices, assemblies and pressure contacted modules can be stored indefinitely as long as the storage conditions are within the limits specified in the datasheet. Pressure contact devices do not deteriorate with time.

Care should be taken in handing the devices and assemblies; in particular damage to the following should be avoided:

- Scratches and dents to the external anode and cathode contact faces of the device may result in reduced thermal and electrical performance.
- Mechanical damage to the device flanges, which may result in loss of hermetic sealing and a possible reduction in the useful life of the device.
- Cracking or chipping of the alumina ceramic which may result in loss of hermetic sealing or a reduction in tracking performance between the anode and cathode.
- Distortion to the end plates, bus bars and coolers of an assembly, which may result in water leaks, poor thermal performance or the inability to mount the stack to the assembly fixtures.
- Scratches or fingerprints on the assembly components that could damage the surface passivation and result and increase in localised oxidation or corrosion.
- Damage to assemblies resulting from multiple stacking.

It is recommended that latex, vinyl or nitrile gloves be worn when handing devices or assemblies.

Assemblies utilising oil filled capacitors should be orientated to prevent oil leaking from the capacitor.

The recommended manual handling procedures should be adopted when handling a number of devices or an assembly to avoid potential personal injuries. For an assembly, a crane or other suitable handing equipment is recommended.

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Date: 28th November 2013

Issue: 1

An application note for soldering leads to thyristors, GTO’s and IGBT’s

Figure 1 *All device types - Set up* Ensure that the temperature controller for the soldering iron is set high enough to melt the solder.	
Figure 2 *Cathode tag and gate pin solder process* Use a pair of pliers to attach the cathode tag to the cathode terminal. Note that this solder process also applies to GTO’s.	
Figure 3 *Cathode tag and gate pin solder process* Use a pair of pliers to attach the gate terminal to the gate pin. The pin will click into position when it is correctly seated.	

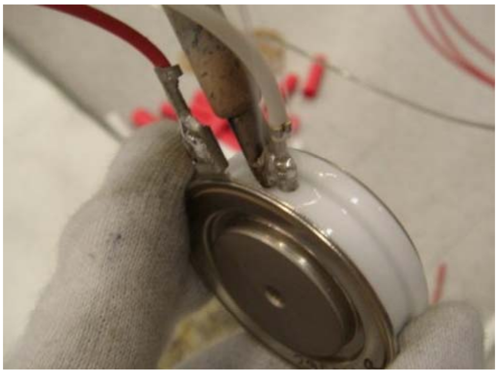
Figure 4 *Cathode tag and gate pin solder process* Wipe the soldering iron tip with a sponge moistened with water and apply a small amount of solder to the tip of the soldering iron. This will assist the wetting process.	
Figure 5 *Cathode tag and gate pin solder process* Place the soldering iron in contact with the cathode tag as shown and allow the solder to wet the joint. Pull the device away from the soldering iron and allow to joint to cool.	
Figure 6 *Cathode tag and gate pin solder process* Place the gate terminal and pin into contact with the soldering iron and apply solder to the joint. Ensure that the solder wets the joint. Pull the device away from the soldering iron and allow to joint to cool.	
Figure 7 *Solder inspection - Cathode tag* Some evidence of flux can be seen on the weld flange area but the solder must not have flow beyond the weld area.	

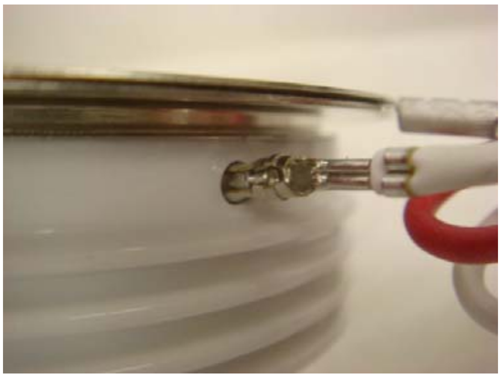
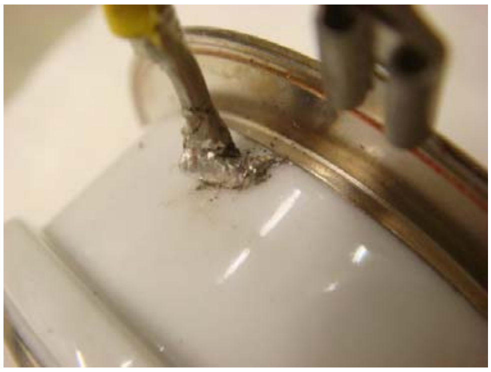
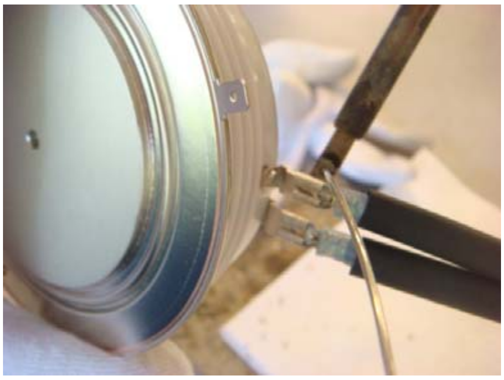
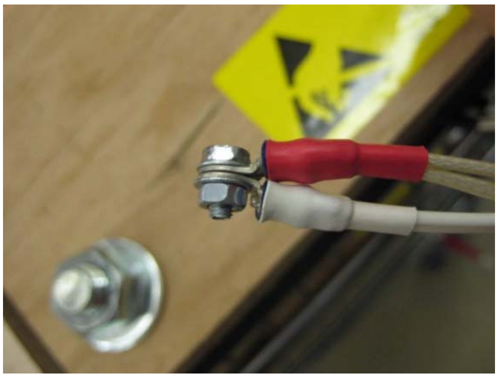
Figure 8 *Solder inspection - Gate pin* Inspect the cathode tag soldered joint. Ensure that the solder has fully wet the joint.	
Figure 9 *Solder inspection - Gate pin* Check that the solder has flowed correctly onto the gate pin. The picture shows EXCESSIVE SOLDER shorting the gate to the cathode. This solder must be removed, cleaned and re-soldered.	
Figure 10 *Shrink sleeving* Place the sleeving (if required) over the soldered leads and push up to the gate and cathode tag terminals.	 
Figure 11 *Shrink sleeving* Shrink the sleeving using a hot air gun. Inspect the sleeving to ensure it has shrunk evenly around the terminals and that no exposed copper wire is showing between the end of the terminal and the lead insulation.	

Figure 12 *Cleaning process* Spray a small amount of flux removing solvent onto a tissue and remove the flux from the top face of the cathode return flange. Note that if clear sleeving is used the flux removal should be carried out before the sleeving process is complete.	
Figure 13 *Cleaning process* Gently remove the flux from the underside of the cathode flange.	
Figure 14 *Cleaning process* Apply a small amount of flux removing solvent to a short bristled brush.	
Figure 15 *Cleaning process* Remove the flux underneath the cathode tag using the brush.	

Figure 16 *Cleaning process* Remove the excess flux close to the gate pin using the tweezers.	
Figure 17 *Cleaning process* Clean the anode poleface with a tissue soaked in flux removing solvent.	
Figure 18 *Cleaning process* Clean the cathode poleface with a tissue soaked in flux removing solvent.	
Figure 19 *IGBT solder instructions* Take ESD precautions when soldering IGBT devices.	

Figure 20 *IGBT solder instructions* Tighten the ESD wrist strap onto the appropriate wrist.	
Figure 21 *IGBT solder instructions* Place the heatshrink onto the lead terminations as shown.	
Figure 22 *IGBT solder instructions* Remove the shorting clip from the emitter and gate connectors.	
Figure 23 *IGBT solder instructions* Gently push on the connectors to the termination.	

Figure 24 *IGBT solder instructions* Solder using the same process as shown for thyristors. Follow the thyristor instructions for the heatshrink process.	
Figure 25 Ensure that the gate lead terminals are shorted before removing the ESD protection shown in figures 19 and 20.	

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