Compendium on Large Area Thyristors

Objectives

This document outlines the general functionality and characteristics of high-power thyristor devices in disc-shaped press-packs. **Figure 1** depicts the typical appearance of such a disc device and the large-scale silicon die that forms the power semiconductor.

Figure 1. High Power Thyristor Devices

Disc devices, also referred to as capsule-types, are preferred components when it comes to handling high voltages and high currents.

Applications

- High-power motor drives, Medium-Voltage drives, Soft-starters
- Welding, Induction Melting, and electro-chemical power supplies
- STATCOMs and HVDC-based power transmission
- Transportation in Rail, Marine and Mining
- Renewable energies, Wind and Solar Power

Target Audience

This document is intended for all engineers that need to get familiar with high-power thyristors, their features, and capabilities.

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1. Introduction

Thyristors, invented in the late 1950s, are semiconductors that can be turned on by applying a control current in a period of positive voltage across the device and turn off once the load current reverses. Thyristors are therefore widely used in applications that control alternating currents.

The technology itself is well established and despite the development of high-power IGBTs and silicon carbide (SiC) MOSFETS will remain in the market for dedicated applications. Therefore, this document summarizes the basics of this technology as a reference for power-electronic engineers.

2. Device Theory and Design Device Description

The thyristor, also called silicon-controlled rectifier (SCR), is a three terminal, four-layer, regenerative device. Sketched in **Figure 2** is the symbol, the physical representation in the four alternating P-N-layers, and the electrical representation as interconnected pair of transistors.

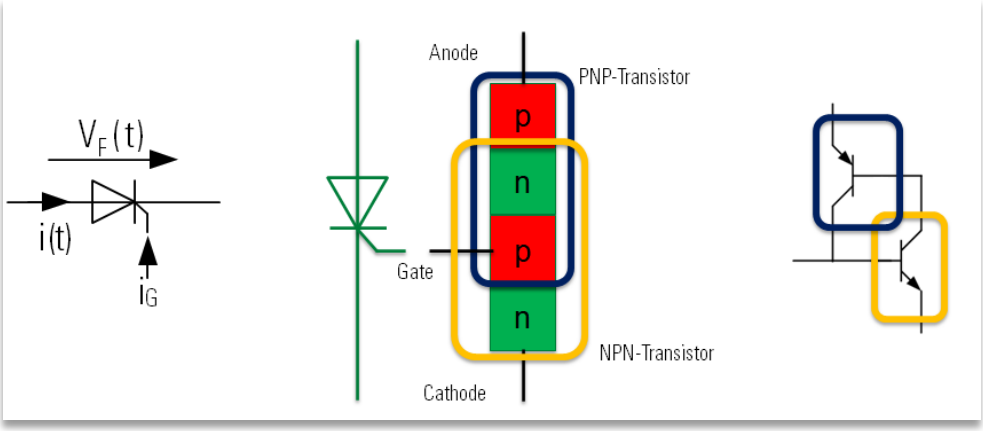

Figure 2. Thyristor in Three Different Representations

The thyristor has essentially three modes of operation:

- Forward blocking with a voltage V_F at the anode is positive with respect to the cathode
- Reverse blocking with a voltage V_F at the anode is negative with respect to the cathode
- Forward conduction with current flow from anode to cathode

It is important to note that sustained reverse conduction is not possible.

These conditions are often called static conditions, the transitions between the various modes of operation are usually termed dynamic operation.

In order to switch the thyristor from the forward blocking mode into the forward conduction mode, a relatively low gate-current pulse I_G is required. This gating or trigger pulse must flow from the gate terminal to the cathode terminal. A typical gate pulse would be 1A from a 20V source, and a few tens of microseconds in length. Within a few microseconds of the initial application of the gate current, the thyristor will begin to switch on. Once the anode current has risen to a level beyond the *latching current* value, the gate pulse may be removed, and the thyristor will remain in conduction due to a regenerative action. The device will remain in conduction indefinitely, providing that the anode current is maintained above a minimum current, known as the *holding current*. It should be noted that, although conduction will begin within a few microseconds of the gate pulse, this conduction will first be localized around the thyristor's internal gate structure. It may take up to two milliseconds for conduction to spread across the full area of the device and the on-state volt drop to settle within published parameters. This time is referred to as the *spreading time*.

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As mentioned, a thyristor will remain in conduction mode until the anode current falls below the holding level. This assumes a very slow rate of decay of current. More typically, the current falls very rapidly through zero and starts to reverse. In this instance, depending primarily on the current change rate di/dt, the thyristor will remain on for a short period after current zero crossing, before starting to block reverse voltage. The *stored charge*, corresponding to this reverse current, is important in terms of device losses and snubber design. In addition, under these conditions, a minimum time must elapse before the thyristor is able to block forward voltage; this is known as *circuit commutated turn off time*. Maximum voltage and current ratings and their derivatives with respect to time, dv/dt and di/dt, impose further constraints on thyristor operation.

2.1. Structure

High voltage thyristors are manufactured from a mono-crystalline slice of very high purity silicon. The silicon slices are given an initial n- doping by a neutron transmutation process, which yields very high uniformity for the bulk of the device. The thyristor structure is then manufactured vertically through the slice, using a combination of diffusion and photolithography processes resulting in the structure given in **Figure 3**.

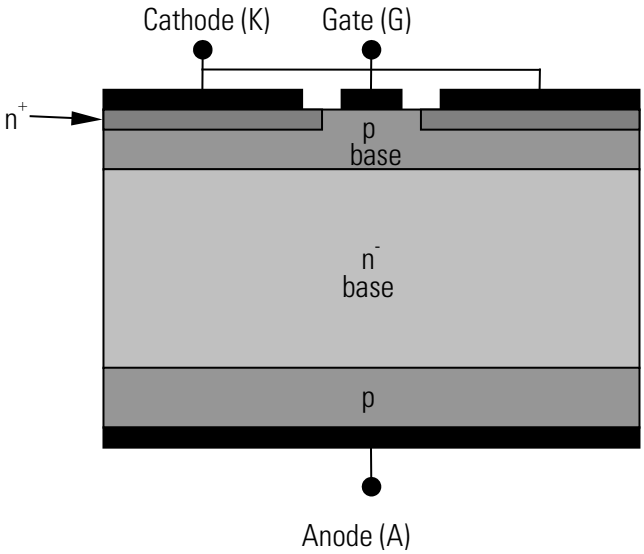

Figure 3. Practical Device Structure, Cross-Section

The principal factors governing high voltage thyristor designs are silicon thickness, primarily the n-base, and p-base doping concentration.

The n-base thickness along with its doping concentration determines the voltage blocking capability of the device. The thicker the n-base, the higher the voltage rating but the losses will be higher and dynamic response generally slower. The p-base doping affects the trigger sensitivity of the device but as such also influences the dv/dt capability and turn off time.

When designing thyristors, Littelfuse optimizes these trade-offs according to the intended field of operation and application to be served.

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2.2. Carrier Lifetime Control

One important factor in optimizing thyristors is the so-called carrier lifetime, which is the average time required for an electron and hole to recombine with each other. After the manufacturing process, the carrier lifetime is quite high. This means that during conduction many carriers are available and as such the device's conduction losses are low. However, a high carrier lifetime also means that the device is slow to turn off. High values of stored charge consequently increase the turn-off losses. In light of this, it is desirable to control the carrier lifetime of a given device. Carrier lifetime control can be performed by several means such as electron irradiation, heavy metal diffusion, and ion implantation, of which the most common method employed on large area devices is electron irradiation. Electron irradiation, with subsequent annealing, provides a means of accurately controlling carrier lifetime to provide the optimal trade-offs for a given application. Carrier lifetime can be tailored to specific needs if required. For indicative purposes, **Figure 4** summarizes the typical trade-off relationship obtainable.

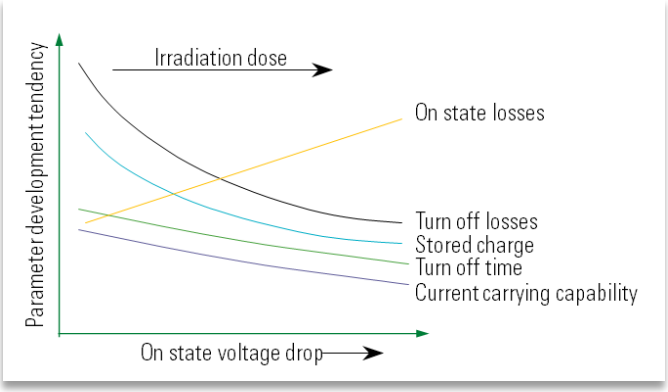
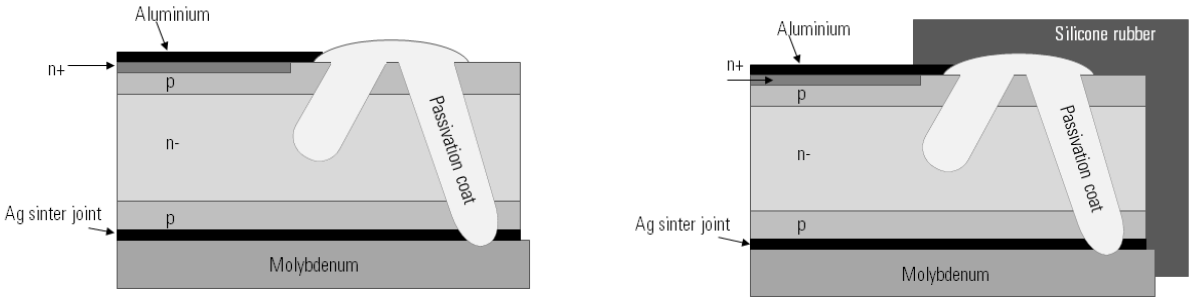


Figure 4. Impact of Irradiation Dose to the Device's Parameters

2.3. Junction Edge Termination

The bulk of the diffused silicon slice is designed to accommodate the required electric field within the n-base region. However, at the edge of the silicon slice, there is a high surface field concentration, which would lead to premature voltage breakdown. Several techniques are available to designers to control the electric fields at the edge of the junction, the most common of which is junction edge profiling. Referring to **Figure 5**, grooves are cut through the main blocking junctions; the geometry of these is designed to ensure that the maximum electric field at the surface of the device is no more than that in the bulk. After cutting, the grooves are etched, to restore the crystalline qualities of the silicon before a special passivation coat is applied directly to the junction's edge. This passivation coat is designed to withstand the high electrical stress and equally important, the accumulation of surface charge. Finally, a silicone rubber ring is molded around the device to provide further control of electric field and protect against mechanical damage. The junction edge termination technology used by Littelfuse has been thoroughly evaluated for long-term reliability at high voltages. Extensive type tests have been conducted as demanded per IEC / JIS specifications.



(a) Edge Termination up to 2.8 kV **(b) Edge Termination 3.6 kV and up**

Figure 5. Detailed view to the Junction Terminations

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2.4. Gate- and Cathode Structures

Triggering a large area thyristor of the design given in **Figure 5** would require a quite substantial gate pulse. To improve this situation, all large area thyristors incorporate an amplifying gate structure as detailed in **Figure 6.**

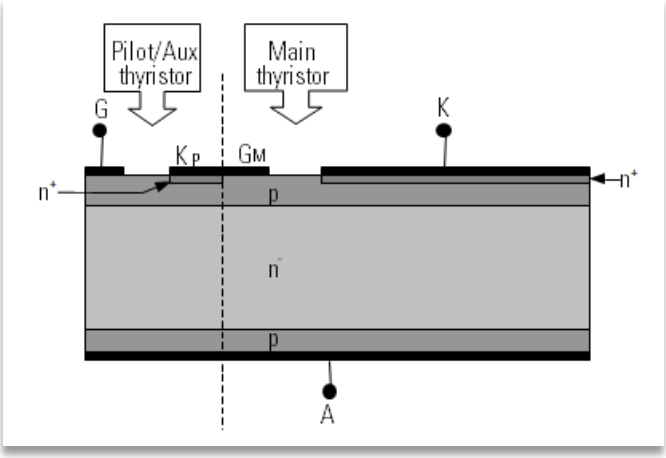
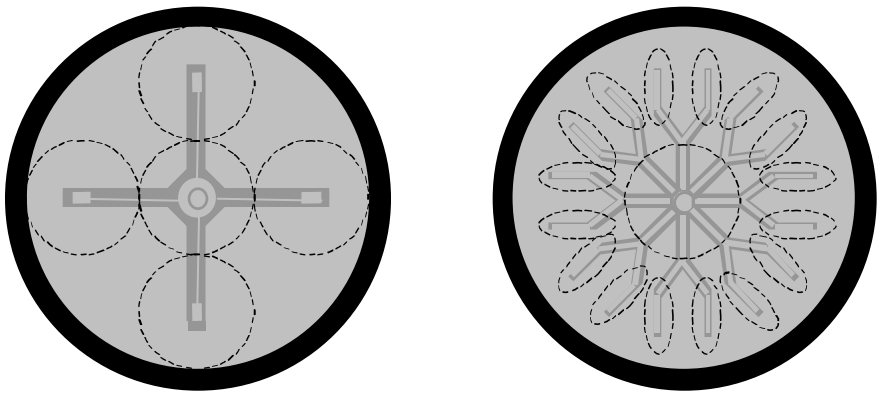


Figure 6. Amplifying Gate Structure with Pilot- and Main-Thyristor

The implementation of this is similar to the Darlington transistor concept. A smaller device is used to trigger the main device, the smaller device is often referred to as the pilot- or auxiliary thyristor.

It can be seen from **Figure 6**, that the pilot thyristor's cathode is contacted to the main thyristor's gate. When the pilot thyristor is triggered, current flows from the common anode into the main cathode gate region, thus triggering the main cathode. In terms of the user, the device simply has three terminals and may be treated as a conventional thyristor. Another advantage of this design is that different device types have a similar gate requirement, hence standardization of gate driver units is possible.

The current flowing in the pilot thyristor may be distributed to a greater or lesser extent to turn on the main cathode area. **Figure 7** holds a comparison of two different types of thyristor designs.



(a) Phase Control Thyristor (b) Fast Switching Thyristor

Figure 7. Auxiliary Cathode Pattern for different Requirements, dotted lines denote spreading fronts

The amplifying gate pattern can be seen clearly as a series of arms radiating from the gate contact in the center of the device. A phase control thyristor (PCT) only has 4 to 6 gate arms and each is designed to be primarily active at its extremity. This technique is referred to as dissemination. In contrast, the fast switching thyristor (FST) has up to 24 gate arms and each one, being uniform in width, is designed to be active along most of its edge length.

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When the thyristor is triggered, current initially flows through the pilot thyristor. Then, when a certain current is reached, the main thyristor will start to conduct and current will drop in the pilot thyristor. This commutation of current into the main thyristor occurs, initially, around the acting edges of the amplifying gate. The current subsequently spreads across the whole wafer as indicated by the dotted lines. The rate of transfer and spreading is highly influenced by, among other factors, current change rate di/dt. Obviously, different applications require different design considerations. For example, the phase control thyristor design ensures at least four, equidistant, discrete areas of the main cathode conduct plus the center area. An even simpler gate geometry, potentially reduced to just three arms, could not guarantee proper turn-on at the lower di/dt seen in phase control applications.

Another area affecting amplifying gate design and indeed, the main cathode design, is shorting. If the gate structure were manufactured as shown in **Figure 7**, the resulting thyristor would be highly sensitive to voltage changes dv/dt forward direction and spurious gate signals. To counteract this, small shorts in the form of resistive connections are included in the design of the gate structure. These connections serve to channel capacitive displacement currents safely during transients, without compromising the overall performance.

There is a similar effect with the main cathode. Here, gate shorts stabilize the pilot thyristor, but the main cathode could be triggered directly by capacitive currents. To prevent this, small shorts through the cathode's n+ layer are included in the design. The design of these cathode shorts is of critical importance as they can potentially hinder spreading and hence reduce di/dt performance. However, the use of sophisticated computer models and many years of experience enable the design of devices with optimized dv/dt and di/dt performance for a given application.

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2.5. Packaging

The mechanical design of power thyristor housings can have a surprising influence on their electrical performance and long-term reliability. To achieve efficient cooling of the silicon slice, and hence ensure maximum power handling capability, it is important to bring the silicon slice as close as possible to the heat sink. However, it is also important to maintain the electrical insulation required for high voltages.

To achieve this, all Littelfuse large area thyristors are encapsulated in press-pack type housings, which conform to international industry standards. All components used in the construction of the device are screened to ensure that exacting standards of quality and component tolerance are met. In contrast to the so-called alloy-free technology used until recently, current products are built using a low-temperature sintered construction and diffusion soldering processes. The silicon die is directly bonded to a molybdenum disc which leads to higher surge-current capabilities as well as improved thermal performance. As the complete silicon slice now is in, supported by a metal disc, thermal performance improves, and a more reliable edge-termination is achieved. Maintaining the same height of the device using thicker copper electrodes also increases thermal capacities while the thinner molybdenum plate in use reduces the thermal resistance. The two technologies are contrasted for comparison in **Figure 8**.

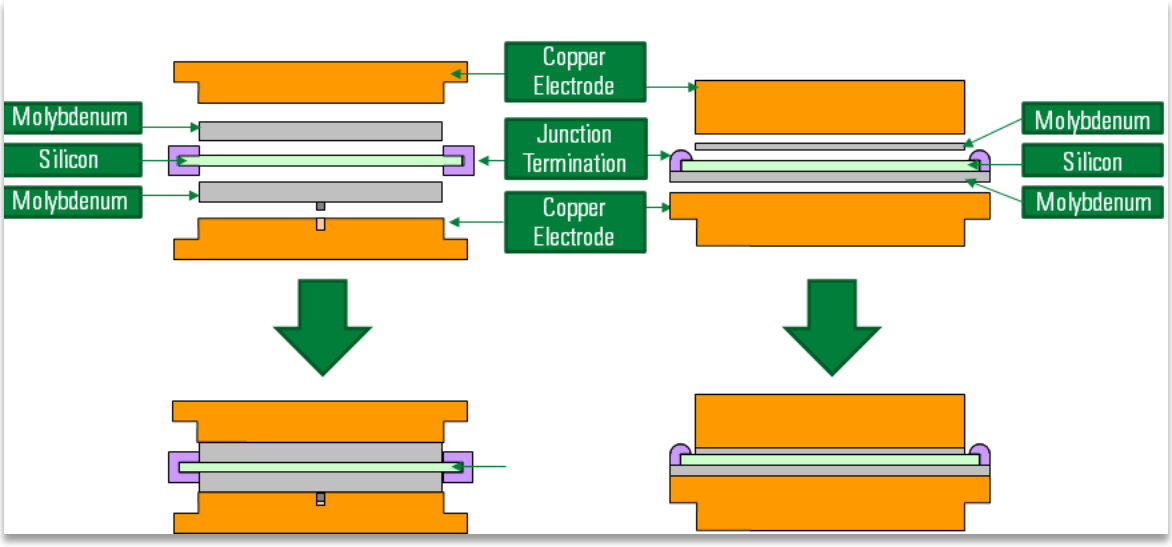

Figure 8. Comparison of two different Assembly Technologies

The reliability improvement offered by sintered technology is most apparent in applications where repeated thermal cycling of the device occurs, such as induction melting, energy transfer in high-voltage DC-transmission, and traction applications. All devices are evaluated for thermal cycling performance at the design stage. Tests performed show that these devices are easily capable of surviving more than 100,000 thermal cycles at a junction temperature swing of over 90°C, as outlined by the relevant international standards.

Mounting of the device requires a force of 1 to 1.5 kN/cm² to be applied evenly along the axis of the pole faces. The exact value of mounting force depends upon individual thermal resistance and thermal cycling requirements. Littelfuse also offers a range of complementary clamping arrangements to suit individual requirements, ranging from single devices to complete subassemblies.

Mounting disc devices in general is described in the Littelfuse *Mounting and Handling Press-pack Semiconductor Devices Application Note*.

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3. A Guide to Thyristor Ratings and Characteristics

The aim of this section is to guide the designer through the meaning and interpretation of thyristor ratings. Each parameter will be looked at in turn, in the order in which it appears in the data sheet. Not all parameters are given in all data sheets, the data sheets only contain parameters which are relevant in typical applications for a given device. In the case of non-standard parameters or tests being required, this can be achieved by customized measurements, denoted by the use of a dedicated suffix code. This is typically done where parallel or series matching of devices is required or where there is a need for testing at non-standard conditions; for example, forward voltage drop at a different test current or testing at conditions that reflect the application.

Data sheets offer two main categories of information:

- Maximum ratings, giving information on the absolute maximum capabilities of a given device. Exceeding these values may cause permanent damage or catastrophic failure.
- Characteristics which provide information on how a given device will behave in the application. Where maximum or minimum limits are given, Littelfuse guarantees that a device will behave within these boundaries under normal operating conditions.

Unless stated otherwise, all values are applicable over the temperature range -40°C to 125°C.

3.1. Off state voltage ratings – V_{DRM}, V_{RRM}, V_{DSM}, V_{RSM}, V_{DC}

Off state voltages or blocking ratings fall into three main categories:

- repetitive peak parameters V_{DRM} / V_{RRM},
- non-repetitive peak values V_{DSM} / V_{RSM}, and
- continuous working voltages – V_D or V_{DC} / V_R.

These values are illustrated in **Figure 9**, which gives an overview in a typical waveform.

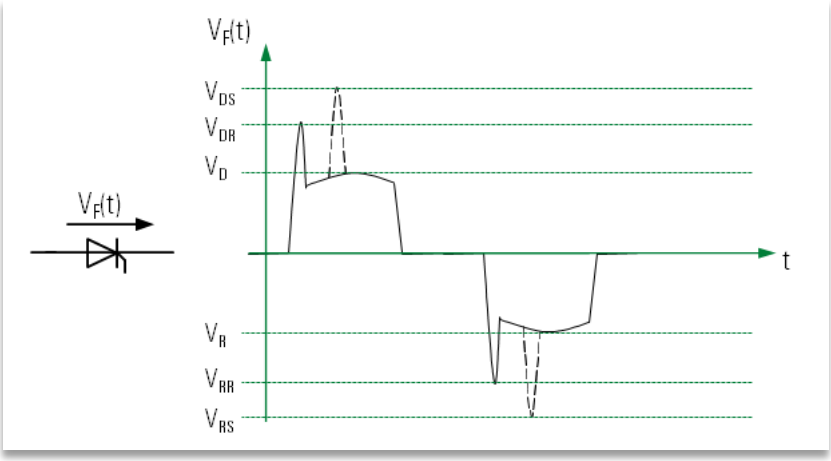

Figure 9. Typical Voltage Waveforms

Continuous ratings, V_D and V_R, are the maximum continuous or direct voltage values that may safely be applied to the thyristor. For phase control applications, this value would equate to the crest voltage of the supply under worst case conditions. For inverter applications, this value represents the highest dc link voltage that can be expected.

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Repetitive ratings, V_{DRM} and V_{RRM}, refer to the absolute highest instantaneous value of any repetitive transient voltage applied to the thyristor. V_{RR} is usually generated by commutation of the thyristor itself and is a function of the circuit. V_{DR} is often impressed upon the thyristor by another device in the circuit commutating and again depends on the circuit design. Unless otherwise stated, these values are valid for sinusoidal pulses with a base width up to 10ms. Again, when designing for this parameter, it is important to take the worst-case scenario into consideration.

The surge ratings, V_{DSM} and V_{RSM}, refer to the absolute instantaneous values of any non-repetitive transient voltage applied to the thyristor. These voltages are usually caused by an external effect, such as a supply disturbance. It is assumed that its effect has completely disappeared before the next transient arrives. Unless otherwise stated, these values are valid for sinusoidal pulses with a base width up to 10ms.

A further blocking voltage parameter is the breakover voltage, V_{BO}, which refers to the forward voltage at which the thyristor will be self-triggered into forward conduction due to excessive leakage current. This value is seldom quoted for high power thyristors, as the marginal triggering condition may result in device destruction.

In the reverse direction, most thyristors exhibit some reverse avalanche capability, $V_{R(AV)}$. However, this capability should only be used with extreme caution.

It should be noted that all blocking ratings assume the gate terminal to be floating open circuit or shorted to the cathode. Any current induced into the gate leads by electromagnetic interference may affect these values.

It should also be noted that the blocking ratings are given for a temperature of 25°C. Below 25°C, a de-rating factor of 0.13% per Kelvin should be applied to published values.

3.2. On state current ratings – $I_{T(AV)}$, $I_{T(RMS)}$, I_{DC}

The average and root-mean-square (RMS) current ratings are given in the data sheet as a guide to the 180° sinusoidal current handling capability of a given device. The values are calculated based on a fixed case temperature T_{Case}, the maximum junction temperature $T_{j(max)}$ and known thermal resistance $R_{th(jc)}$ from the device's junction to its case. These parameters are used to calculate the maximum power dissipation $P_{AV(max)}$ allowed, to achieve the maximum junction temperature.

The on-state characteristic $V_F=f(I_T)$ can be approximated by the linear function comprised of the XXXX-voltage V_0, the thyristor's differential resistance R_T and forward current. It is then possible to calculate the average current permissible to achieve this power level. By multiplying the average value by the form factor $\pi/2$, the RMS value may also be obtained.

Equations 1 to **3** describe the mathematical correlation.

$$P_{AV(max)}=\frac{T_{j(max)}-T_{CASE}}{R_{th(jc)}} \quad (1)$$

$$I_{T(AV)}=2\cdot\frac{\sqrt{Vo^2+R_T\cdot\pi^2\cdot P_{AV(MAX)}}-V_0}{R_T\cdot\pi^2} \quad (2)$$

$$I_{T(RMS)}=I_{T(AV)}\cdot\frac{\pi}{2} \quad (3)$$

Various values of average, RMS, and dc-current are given in the data sheet for various case temperatures and cooling arrangements. It should be noted that these ratings are given, as by most manufacturers, for indicative purposes only. They are generally used only to compare the performance of similar devices under the same conditions. They do not include any turn on or commutation losses as encountered in practical circuits and as such do not necessarily imply real operational ratings.

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3.3. Surge current ratings – I_{TSM}, I^2t

Two principal surge or overload current ratings exist, I_{TSM} and I^2t. I_{TSM} is the maximum peak value of a non-repetitive, half sinusoidal, surge current of specified base width. This usually refers to 8.3 or 10ms corresponding to 60 or 50Hz respectively. The rating assumes that the device has already been operating at maximum power and hence the junction temperature is at its rated maximum value. During the surge pulse, the device's junction is heated to well beyond its rated maximum temperature. The junction can safely withstand average temperatures of up to 350°C for short periods without any irreversible damage. However, at this highly elevated temperature the device is no longer able to block its rated voltage. To enable designers to use these ratings more effectively, two cases are given in a data sheet. The first value, I_{TSM1} results in a condition whereby the device is able to block up to 60% of its rated reverse voltage immediately after the surge event. This indicates the maximum fault condition which the device can 'ride through' and maintain operation.

The second value, I_{TSM2}, defines a condition immediately after which the device can no longer block any appreciable voltage. This rating is aimed at applications whereby some means of clearing the fault is used, such as a crowbar, fuse link or circuit breaker.

I^2t is the surge current load limit integral given in **Equation 4**.

$$I^2t = \int_0^{t_P} I_T^2(t) \cdot dt = \frac{I_{TSM}^2 \cdot t_P}{2} \qquad \textbf{4}$$

The explanatory text relating to I_{TSM}, is equally applicable to I^2t. The reason for including I^2t ratings is to aid in the selection of a suitable semiconductor fuse. The I^2t value of the fuse must be lower than that of the semiconductor device the fuse is meant to protect. Care must be taken to ensure that any additional energy stored, not limited by the fuse, is considered in calculations.

It should be noted that although a single surge does not cause any permanent damage to the silicon slice, it should not occur too frequently. As per IEC specifications, all devices are expected to withstand at least 100 surge events. It should also be noted that the device may momentarily loose gate control after a surge event.

For further information on surge capabilities of a given device, the data sheet contains a graph of I_{TSM} and I^2t versus pulse width / number of cycles.

3.4. Critical rate of rise of on-state current – $di/dt_{(crit)}$

Due to the physics of the turn on process, the device begins to conduct in a relatively small region around the amplifying gate structure, before spreading to the remainder of the cathode area. If the current increases too rapidly, excessive current density and hence power dissipation in this region may cause the device to fail. For this reason, where appropriate, maximum di/dt ratings are included in the data sheets.

Two ratings are given, one for repetitive and the other for non-repetitive operation. The ability of the device to withstand high di/dt is also influenced by gating conditions. Of particular importance are gate current rise time t_r and peak gate current I_{FG}. A fast-rising gate pulse ≥4A/µs with appropriately high amplitude will ensure that the auxiliary thyristor triggers rapidly with minimal transition losses and supplies a well-defined turn on signal to the distribution arms. If a weak gate pulse is used there is a danger that the auxiliary cathode will take longer in its transition to the on state, with increased losses and generation of local hot spots. The main cathode will, in turn, receive a less well-defined gate signal and have higher losses. Weak gate pulses lead to the risk that either an area of the main cathode will be destroyed, or that the load current will not transfer sufficiently fast from the pilot thyristor, resulting in its destruction.

It should be noted that the di/dt rating is for load component current rise only. When determining a di/dt rating, the discharge from any local snubber network is considered. As such the user can ignore this, assuming the snubber consists of a resistor larger than 47Ω and a capacitor below 0.47µF.

The ratings given for di/dt are generally conservative values, applicable in typical applications. For intermittent operation, pulse applications, or applications using saturable reactors, individual values need to be determined.

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3.5. Gate ratings, characteristics & application – $P_{G(AV)}$, P_{GM}, V_{GD}, I_{GD}, V_{RGM}, V_{GT}, I_{GT}

Included in the data sheet is a diagram similar to the one in **Figure 10**, showing the production limits of the gate characteristics.

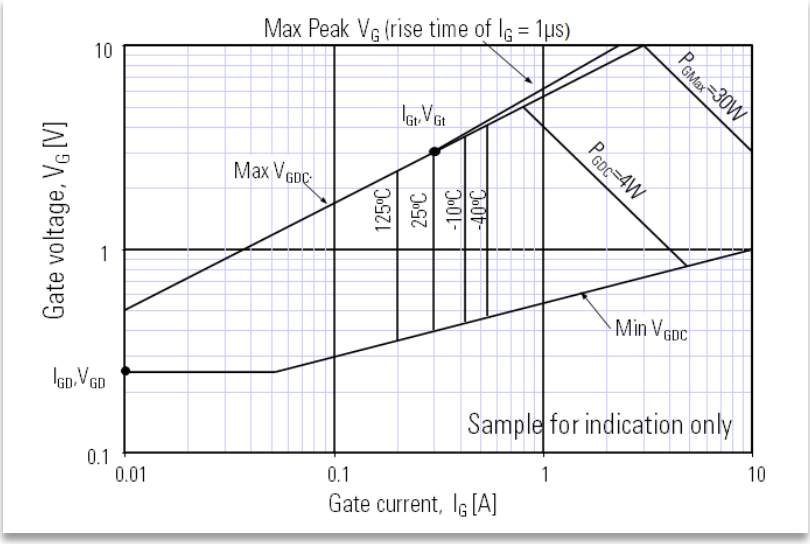

Figure 10. Typical Gate Characteristic

This diagram shows the gate voltage with respect to gate current. A device will have a gate characteristic anywhere between the upper and lower boundary lines. The ratings for $P_{G(AV)}$ and $P_{G(dc)}$ denote the maximum average and continuous power dissipation permissible in the gate region. A boundary line towards the right of the diagram indicates this condition.

The instantaneous power dissipation may be much higher than the average value. However, the peak value of this, P_{GM}, should not exceed the given value at any time. Here too, a boundary line towards the right of the diagram indicates this condition.

The voltage V_{GD} and the current I_{GD} are defined as the maximum gate voltage and current permissible to avoid spurious triggering of the device. A point on the bottom left corner of the gate characteristic indicates these values. The values given are for worst case conditions in a typical application with 67% of V_{DRM} across the device while the maximum junction temperature is applied. Invariably, large area devices are operated in an electrically noisy environment. It is of critical importance that any induced gate signals are suppressed below the gate non-trigger values, as this type of marginal triggering may be destructive to the device. Where appropriate, the use of a gate snubber or filter network is recommended, similar to the one drawn in **Figure 11**.

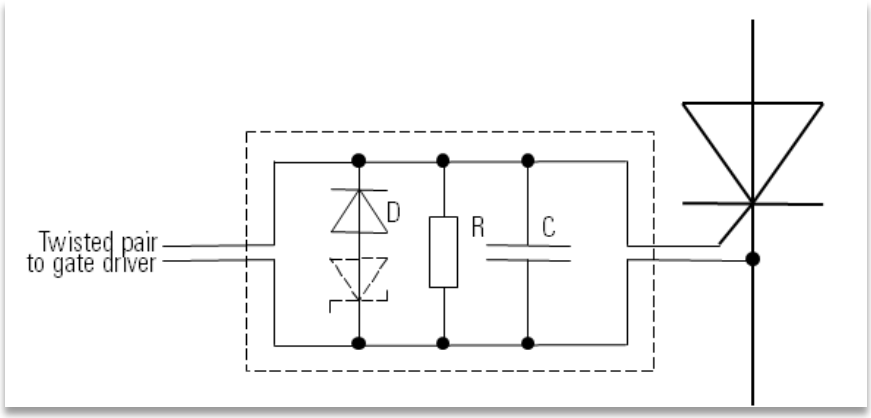

Figure 11. Gate Snubber Network

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Typical values are R=100Ω, C=10pF and D=1N4007. For maximum benefit, the circuit should be mounted close to the thyristor. The inclusion of a Zener diode also helps to protect against excessive reverse gate voltage, V_{RG}.

The value V_{RGM} specifies the maximum instantaneous reverse gate voltage. This value is chosen to limit reverse gate power dissipation to an acceptable level and is considered when defining $P_{G(AV)}$.

Gate trigger voltage V_{GT} and current I_{GT} are the minimum values of voltage and current required to safely trigger the device. Gate trigger voltage and current are highly influenced by temperature. Both, gate trigger voltage and current decrease with increasing temperature. For this reason, several vertical lines are included on the gate characteristic diagram in **Figure 12**, each one representing a minimum trigger condition at a given temperature. Additionally, gate trigger voltage and current decrease with increasing anode voltage. With this in mind, all trigger values are valid down to an anode voltage of 10V.

It is important to keep in mind that a thyristor is a bi-polar device and as such is current driven. Gate trigger voltage is merely a function of gate current and the characteristic impedance of the gate structure. The value of gate trigger current is a minimum and not a recommended operating condition. For optimal performance it is recommended that a gate-current change rate of ≥4A/µs is reached and a high amplitude between 5 and 10 times I_{GT} is applied to the device's gate. The period of this pulse must allow the anode current to rise significantly above the latching level. Where appropriate a dc-coupled gate signal is recommended, this comprising of the initial pulse already described plus a 1.5 times I_{GT} continuous bias, a so-called backporch. A suitable gate-current waveform can be seen in **Figure 12**.

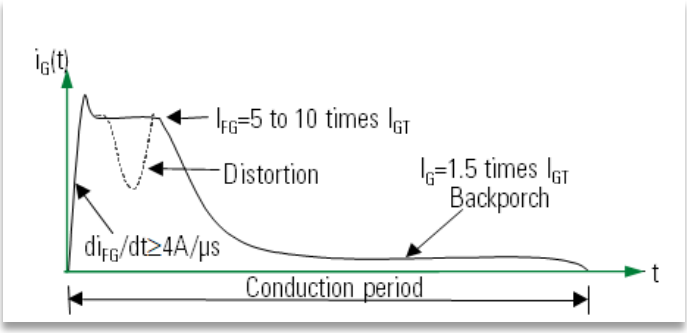

Figure 12. Gate-Current Waveform

This type of gate pulse is particularly advantageous in applications where the anode current can fluctuate close to or below the holding current level. Another application to which this type of gate pulse is suited, is where the thyristor must pick up the current flowing from another device or phase and gate synchronization is difficult. If DC-coupling of the gate signal is not possible, similar benefits can be achieved by the use a train of pulses covering the desired conduction period.

Under load conditions, it is usual to see some distortion of the gate signal as denoted by the dashed line in **Figure 12**. This is caused by feedback from the amplifying gate structure and tends to worsen at higher anode di/dt. Whilst distortion as depicted poses no real problem, if the gate current falls close to the trigger level or indeed goes negative, there is the potential for device failure due to inhomogeneous triggering. Studies have shown severe gate distortion to have a noteworthy effect on long term device reliability. To ensure that distortion is minimized, it is important that the gate current source is of sufficient voltage. The common range for thyristor gate-supplies is 20V to 50V depending upon di/dt requirements and device voltage rating.

It should be noted that applying a forward gate current during reverse blocking should be avoided at all costs. This is because, due to a weak transistor action, the reverse leakage can increase substantially under these conditions. This leakage current flows in a region local to the pilot thyristor causing excessive power dissipation and ultimately, device failure.

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3.6. Temperature Ratings

There are two general temperature ratings

- the maximum junction operating temperature $T_{j(max)}$
- the maximum storage temperature, T_{stg}.

The maximum junction temperature is primarily limited by the ability of the device to block its rated voltage. As the junction temperature increases above its maximum value, the forward and reverse leakage current increase dramatically and blocking instabilities are inevitable. When designing equipment, it is important to ensure that the junction temperature never exceeds its rated value for even a few milliseconds as it may take several seconds to recover. For design purposes, a safety margin is advisable with respect to maximum junction temperature.

The maximum storage temperature is the maximum continuous isothermal temperature, which will not cause any irreversible damage to the device.

3.7. On state characteristics – V_T, I_T, V_0, R_T

The on-state characteristic gives information on the instantaneous voltage drop V_T across the device at a given instantaneous current I_T. The values given are for a worst-case device throughout the production spread, hence typical values may be lower. The values given are for a steady state condition and assume that the whole of the device is in conduction. During the initial turn-on phase, current may be restricted to a region around the amplifying gate and the resulting voltage V_T may be higher than the value given in a datasheet. The time required for the on-state characteristic to settle to its steady state value depends largely on the turn-on conditions and the device's structure. Typical values range from a few tens of microseconds for fast switching types, up to a millisecond or more for phase control types. The additional voltage and hence power loss due to this turn on process is discussed later in terms of turn on energy.

A typical and a maximum value of V_T are given in a data sheet at nominal current. Additionally, a diagram is given to display the characteristic over the nominal operating current range. An example of this is given in **Figure 13**, including the influence of temperature on forward voltage V_T.

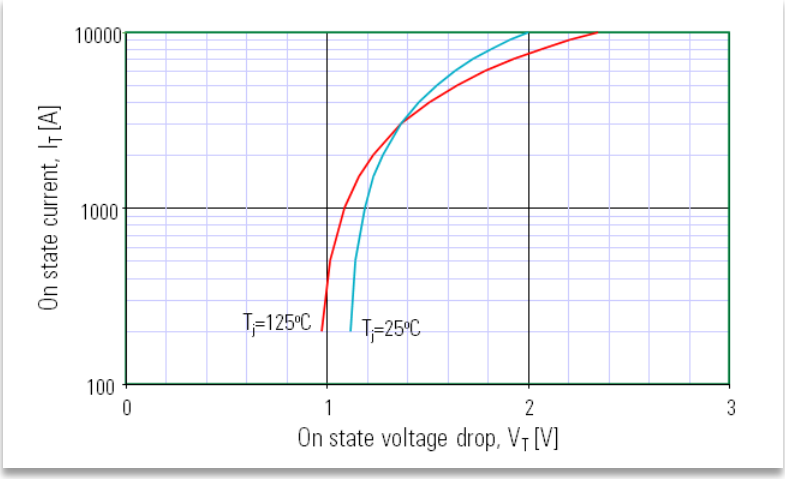

Figure 13. On-state Characteristic

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For the purposes of calculating steady state power loss and current ratings, a straight line approximation of the on-state characteristic is given. This takes the form of the threshold voltage V_0, and the equivalent differential resistance R_T. An approximate value for the on-state volt drop may be found using **Equation 5**.

$$V_T = I_T \cdot R_T + V_0 \quad \textbf{5}$$

For most devices, an additional on-state model is quoted in the datasheet. This gives improved accuracy over the linear model and is particularly suitable for inclusion into computer models. **Equation 6** details the form of the model, known as the ABCD model.

$$V_T = A + B \cdot \ln(I_T) + C \cdot (I_T) + D \cdot \sqrt{I_T} \quad \textbf{6}$$

The constants are derived by using sophisticated curve fitting and are given for hot and cold characteristics, where appropriate. The resulting values from this model agree with the true device characteristics over a wide, application-relevant current range.

3.8. Critical rate of rise of off state voltage - dv/dt(crit)

When a voltage ramp is applied to a thyristor in the off state, a displacement current will flow due to the capacitance of the blocking junction. The higher the dv/dt, the higher the resulting current. If this current is of sufficient magnitude, the thyristor will turn on, but conduction is likely to be localized in a small region of the cathode. The resulting local current density and hence power dissipation may destroy the device. To improve the ability of a device to withstand high dv/dt, resistive shorts are constructed through the cathode emitter to bleed dv/dt associated currents away safely.

The critical dv/dt-rating is conventionally given for a linear voltage ramp, rising to 67% of V_{DRM}. If an exponential voltage ramp is seen in the application, the effective dv/dt may well be approximated by a straight line from 10% through 67% of the waveform. The correlations are visualized in **Figure 14.**

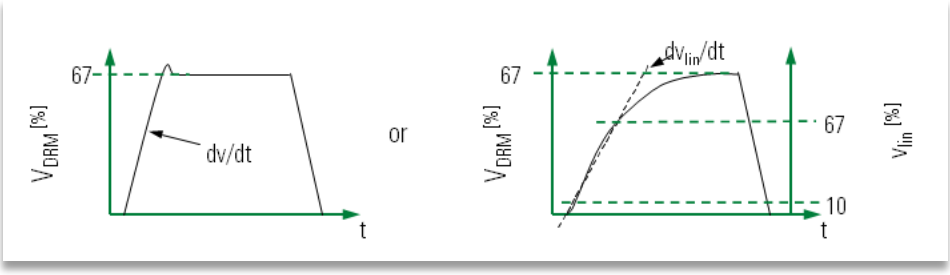

Figure 14. Approximations for dv/dt(crit)

3.9. Off state leakage currents – I_{DRM} and I_{RRM}

The forward leakage current I_{DRM} and the reverse leakage current I_{RRM} given in a data sheet are the peak values of current that may flow when the device is blocking its rated voltage V_{DRM} and V_{RRM} respectively. Referring to the waveform given in **Figure 15**, it can be seen that at the voltage-peak, dV/dt, is inherently zero. In this instant, there is no capacitive component of current.

3.10. Holding current and latching current – I_H and I_L

The holding current I_H relates to the value of on state current required to maintain the regenerative action within a device. It is measured by triggering the device into conduction and then reducing the anode current at negligible di/dt until the device turns off and begins to block forward voltage. It should be noted that if the anode current falls at a significant di/dt, the holding current might be higher.

The maximum holding current is defined as the value of on-state current that will guarantee that any thyristor within the production spread will remain in conduction. Conversely, the minimum holding current, where given, is defined as the value of on-state current which will guarantee that any thyristor within the production spread will turn off.

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In order to initiate a regenerative condition within a device, it is necessary to achieve a value of on-state current that is slightly higher than the holding current, known as the latching current I_L. The correlation between holding and latching current are pictured in **Figure 15.**

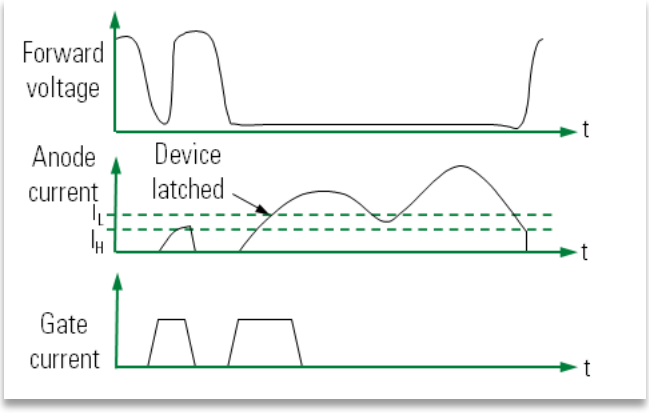

Figure 15. Correlation between Holding Current and Latching Current

3.11. Turn on parameters – t_{gd}, t_r, t_{gt}, t_{spread}, E_{on}

Figure 16 illustrates current and voltage developments during a thyristor's turn-on to explain the timing correlations.

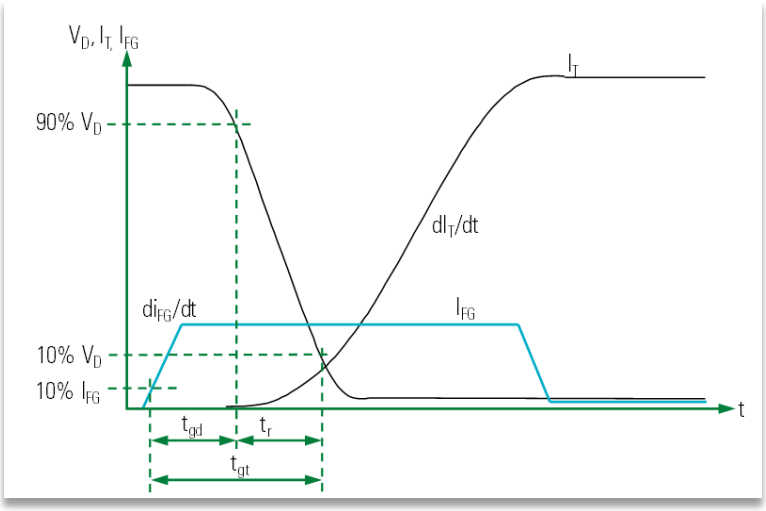

Figure 16. Timing Correlation during Turn-on

The delay time t_{gd} is defined as the delay between the gate current reaching 10% of its targeted value to the point where the forward voltage dropped to 90%. As mentioned previously, a fast-rising gate pulse is important to ensure that the delay time and hence the variation between devices is minimized. This is of particular importance in applications requiring series connection of devices and to a lesser extent parallel connection of devices. In series connection, if one device starts to turn on early, the remaining devices must support an additional voltage and subsequent turn on loss. In parallel connection, if one device switches early, the remaining devices may not be able not turn on correctly, due to low anode voltage. The rise time tr is defined as the time between the point where the forward voltage dropped from 90% close to its on-state value, typically 10%.

Within the circuit di/dt must be limited to avoid device damage. To evaluate this, the negative slope of the voltage drop is measured as one parameter – despite the negative slope, historical convention is to call it rise time. The gate-controlled turn-on time t_{gt} is the sum of delay time and rise time.

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When the device turns on, current starts to flow around the amplifying gate and spreads towards the edge of the silicon. The time taken for this process is known as the spreading time t_{spread}. During spreading, the on-state voltage drop is higher than the steady state value. This is due to an increased current density and leads to an associated increased localized power dissipation. It should be kept in mind that this increased power dissipation is not uniformly distributed across the device area. The integral over the power $P_V(t)=V_D(t)\cdot I_T(t)$ represents the turn on energy E_{ON} which can be seen in the hatched area in **Figure 17**.

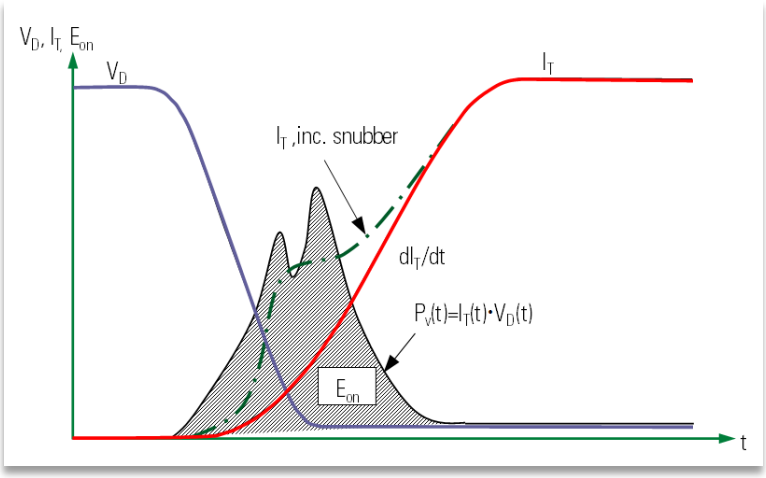

Figure 17. Turn-on Energy

As this occurs once in every switching cycle, switching losses may become a significant proportion of the total device losses in high frequency applications. **Equation 7** details the turn on energy and its associated power loss.

$$E_{ON}=\int_{t|10\%I_{FG}}^{t_{spread}}(V_{T(spread)}-V_{T(steady)})\cdot I_T\,dt \quad \text{and} \quad P_{ON}=E_{ON}\cdot f \qquad \textbf{7}$$

It should be noted that turn on times and turn on energy are highly influenced by gate drive conditions, load-current change-rate di/dt and snubber conditions. For this reason, it is advised to measure the losses in a given design to verify simulation results and achieve the thermal conditions needed.

3.12. Turn off parameters – I_{rr}, t_{rr}, Q_{rr}, Q_{ra}, K-factor, t_q and E_{rr}

During conduction, the bulk of the silicon is flooded with charge carriers. If the device is switched off, or commutated, at a rate that is significant when compared to the carrier lifetime, the device cannot immediately block a voltage applied in either direction.

In a typical application, the device is reverse biased in order to turn it off, this being accomplished by either the AC-supply or forced commutation circuits. When this happens, a current flows in the reverse direction until the remaining charge in the device is either removed or recombines. Only then, the device is able to block the reverse voltage. The peak value of this current is known as the reverse recovery current I_{rr}. The duration this current flows is the reverse recovery time t_{rr}. The integral of this current with respect to time is known as the reverse recovery charge Q_{rr}.

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Figure 18 summarizes the basic reverse recovery parameters.

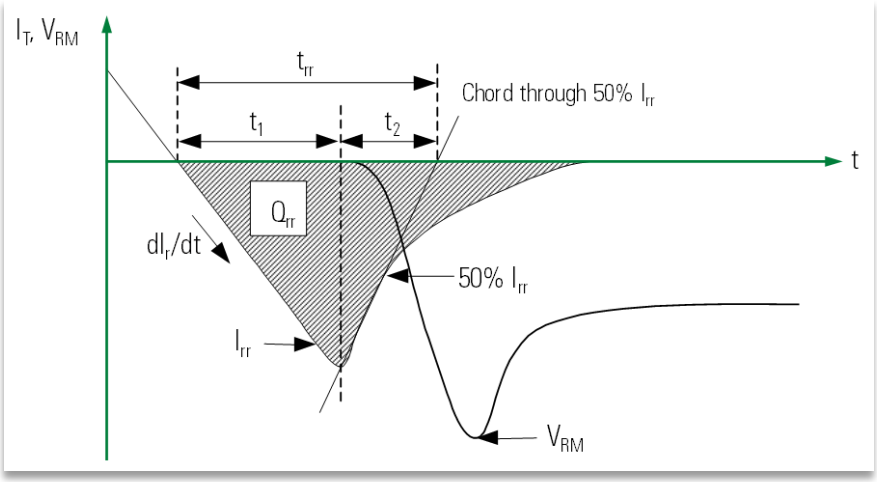

Figure 18. Reverse Recovery Characteristics

The reverse recovery charge is often approximated by calculation. This is done by assuming a triangular characteristic of reverse recovery current constructed using a chord through 50% I_{rr}. This is referred to as Q_{ra} to differentiate it from the real value. In many applications, the shape of the reverse recovery current is of critical importance. At the peak of the reverse recovery current, the device starts to block reverse voltage and the recovery current can fall very rapidly. This reacts with any in-circuit inductance to produce a voltage spike VRM. The faster the current falls, the higher the resulting voltage gets. A device in which the current falls very rapidly, referred to a snappy device, is therefore undesirable.

In order to quantify this, the ratio of di/dt during recovery to reverse di/dt is calculated as the K-factor. Referring to **Figure 18**, K equals t_1 divided by t_2. In practice, an RC snubber circuit is used to limit the effects of reverse recovery.

When commutated, a period of time is required before the device is able to block a reapplied forward voltage V_{DR}. This time is referred to as the circuit commutated turn off time t_q. The delay between commutation and reapplication of voltage is known as the hold off time, t_{hold}. In case $t_{hold}<t_q$ the device will turn back on. In many cases, this turn on will be in a localized area and may result in device destruction. **Figure 19** depicts the main parameters involved in this process.

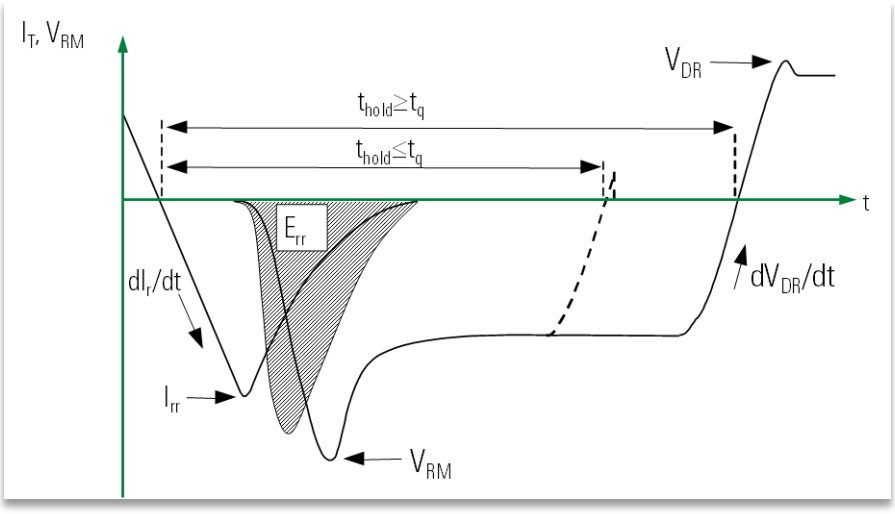

Figure 19. Circuit Commutated Turn-off Time

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The circuit commutation time t_q given in the datasheet is influenced by three parameters that need to be considered to estimate the value later achieved in the individual application. **Figure 20** gives an insight into how the junction temperature influences t_q.

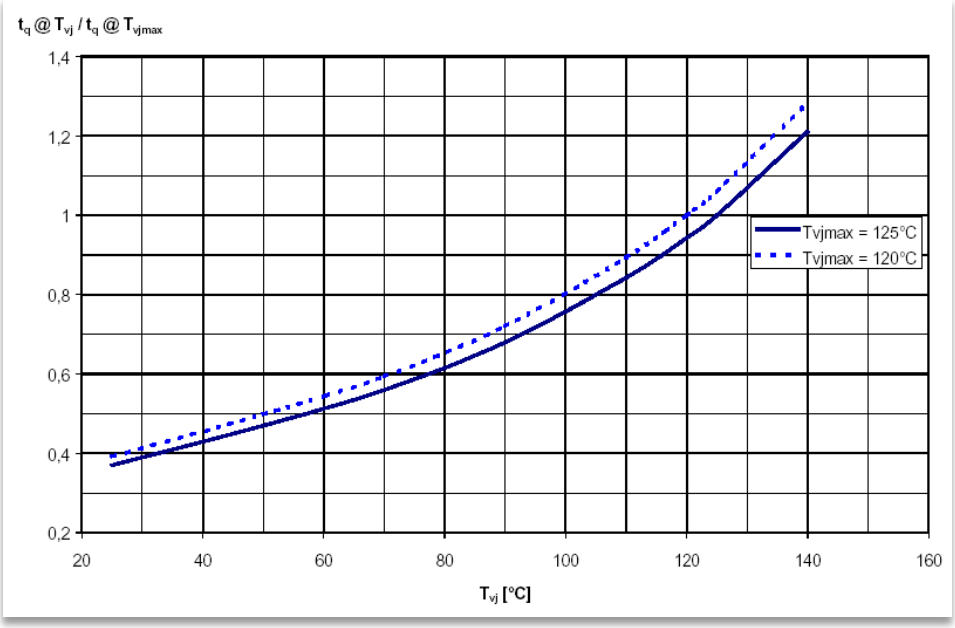

Figure 20. Dependency of t_q on Junction Temperature T_{vj}, normalized to 125°C

The influence on t_q resulting from the voltage change rate is given in **Figure 21**.

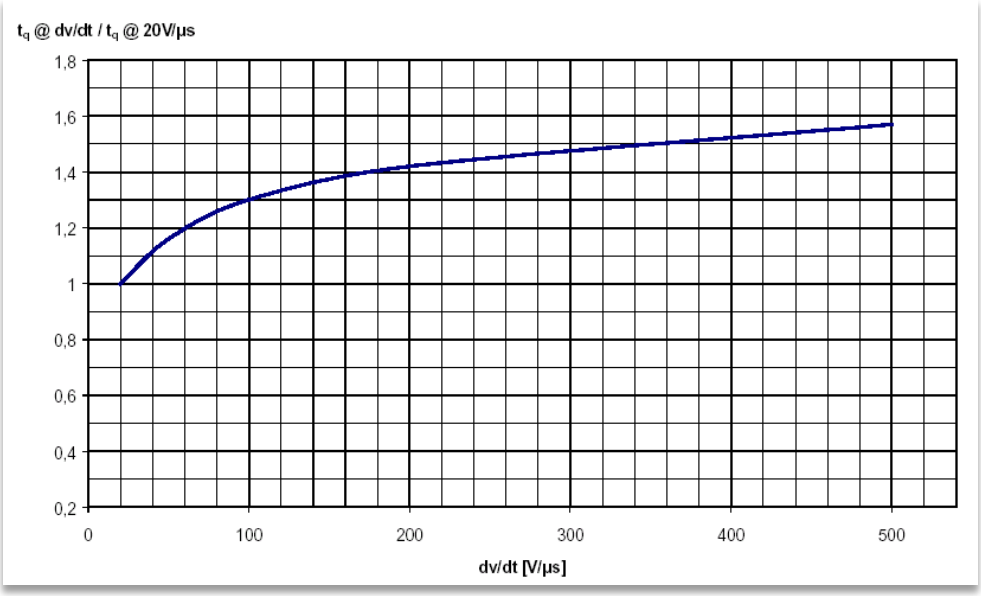

Figure 21. Dependency of t_q on Voltage Change Rate dv/dt, normalized to 20V/µs

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Finally, the current change rate di/dt also has an influence on the t_q-value as can be seen in **Figure 22**.

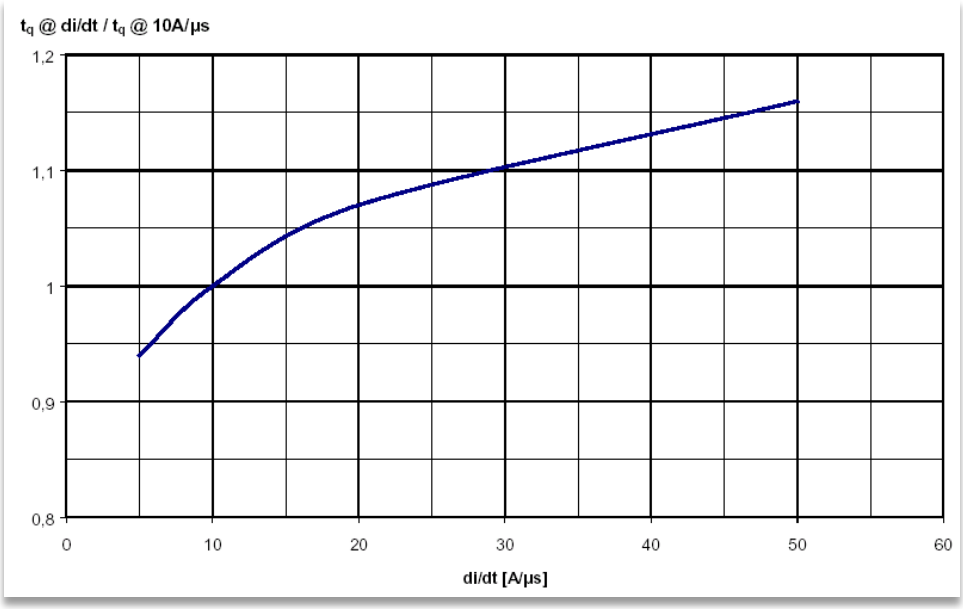

Figure 22. Dependency of t_q on Current Change Rate di/dt, normalized to 10A/µs

These normalized curves act as a fundament to estimate the time t_q for an individual application or setup by correlating the different factors to the values given in a specific data sheet.

It can be seen from **Figure 18** and **Figure 19** that during recovery, there is a period when the device is carrying a significant reverse current while supporting evenly significant reverse voltage. This leads to an instance of high power dissipation within the device. In large area devices, the peak value of this may be up to a few megawatts. The integral of this power is known as the reverse recovery energy E_{rr}. As this energy occurs once in every switching cycle, in high frequency applications, it may become a significant proportion of the total device losses. **Equation 8** details the turn off energy and its associated power loss.

$$E_{rr} = \int_0^{I_{rr} \to 0} I_r \cdot V_R \; dt \quad \text{and} \quad P_{rr} = E_{rr} \cdot f \qquad \textbf{8}$$

Reverse recovery is affected by numerous device and circuit parameters. These include temperature, commutation rate, on-state current, reverse voltage, and snubber design. Additionally, the circuit commutated turn-off time t_q is affected by the voltage change rate dV_{DR}/dt and to a lesser extent the magnitude of V_{DR}. Curves are included in data sheets, where appropriate, to allow the user to predict how a device will behave in the circuit under the specified conditions. In addition to these curves, the coefficients of a polynomial expression are included for computer modelling and simulation of the device's behavior. The mathematical form of recovery model is given in **Equation 9**.

$$y = \sum_{p=0}^{p=n-1} k_p (di_r/dt)^p \qquad \textbf{9}$$

In **Equation 9**, n represents the number of terms in the series, p the individual number, y is the recovery parameter an k_p a coefficient given in the data sheet.

Due to the large number of variables affecting reverse recovery characteristics, it is not practical to include, in a data sheet, information covering every eventuality; indeed, it may be preferable to make measurements in circuit to determine recovery losses.

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3.13. Thermal Parameters - R_{th} and $Z_{(th)t}$

Values of the steady state thermal resistance R_{th} are given for anode-, cathode- and double-side cooling where appropriate. These values assume the device is mounted within the specified range of force and that the force is evenly distributed. The values include mounting effects and assume that the mounting surfaces are of a quality similar to that of the device.

Detail on mounting large-area disc devices can be found in the Littelfuse *Mounting and Handling Press-pack Semiconductor Devices* Application Note.

The masses of the silicon and associated components within the housing have a significant thermal capacity. This results in the device having transient thermal impedance $Z_{(th)t}$. The $Z_{(th)t}$-value for periods of time measured in seconds is lower than the R_{th}-value for the steady state. A data sheet includes a graph showing the relationship between transient thermal impedance and time. **Figure 23** gives a typical example of this.

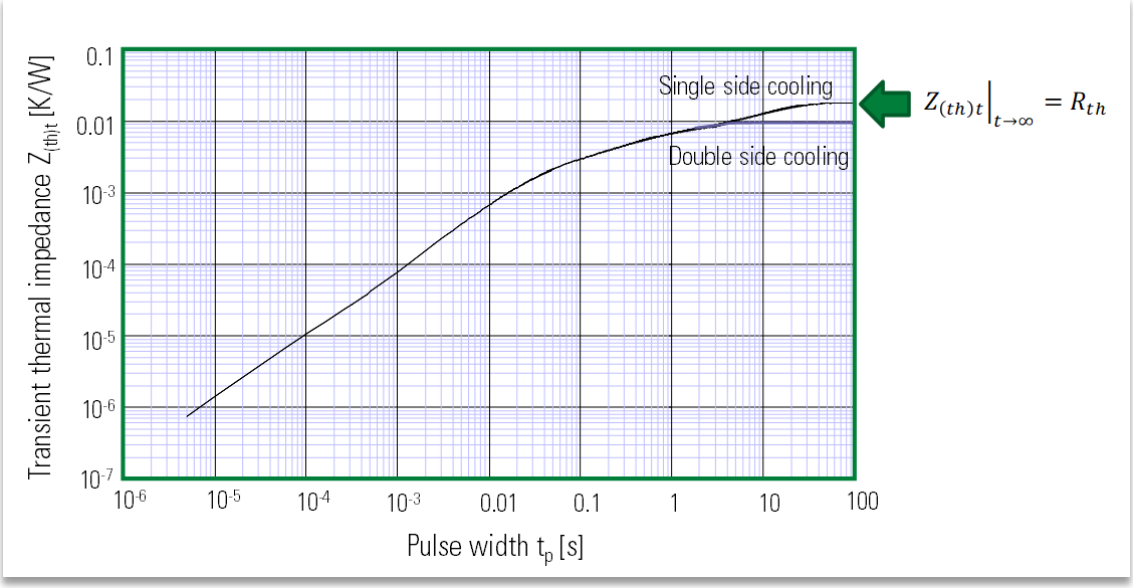

Figure 23. Transient Thermal Impedance $Z_{(th)t}$

In addition to this graph, a representative function is included for the purposes of device simulation and modelling. This function is given by the polygonal expression in **Equation 10**.

$$r_t = \sum_{p=1}^{p=n} r_p \left[\left(1 - e^{\frac{-t}{\tau_p}}\right) \right] \qquad \textbf{10}$$

The equation result is a thermal resistance $\boldsymbol{r}$ at a time t. The constants $\boldsymbol{\tau_p}$ and $\boldsymbol{r_p}$ are given in the device data sheet.

The transient thermal impedance may be used for applications where the power dissipation varies with time.

In applications like rectifiers operating at 50Hz, the effective thermal impedance is higher than the steady state value of the thermal resistance. Where appropriate, values of thermal impedance for common applications are given.

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3.14. Mechanical characteristics – F, W_t

The range of recommended mounting force F is that which guarantees correct operation of the device within the specifications outlined in the data sheet. Higher mounting forces may offer some improvement in conduction losses and power dissipation. However, this may be at the expense of thermal load cycling performance. Littelfuse also offers a range of complimentary clamping arrangements to suit individual requirements, ranging from single devices to complete subassemblies.

The weight or mass W_t of the complete device along with the mounting force F is given in the datasheet similar to the example in **Figure 24**.

F	Mounting force	5	-	9		kN
W_t	Weight	-	90	-		g

Figure 24. Excerpt of the datasheet showing Mounting Force and Device Weight

An outline drawing is also included as seen in **Figure 25**.

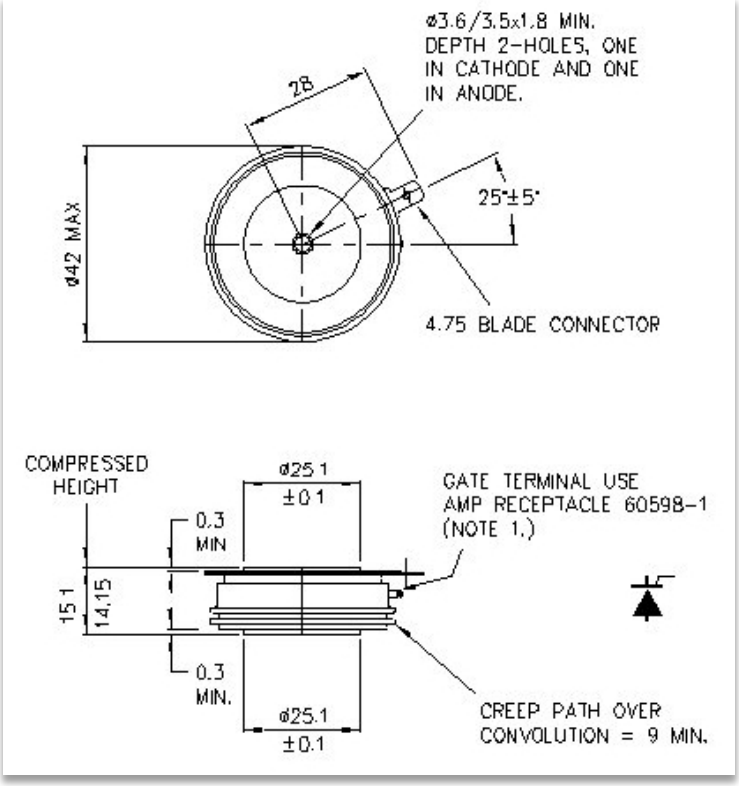

Figure 25. Typical Outline Drawing of a Capsule-type Thyristor

For additional information please visit www.Littelfuse.com/powersemi

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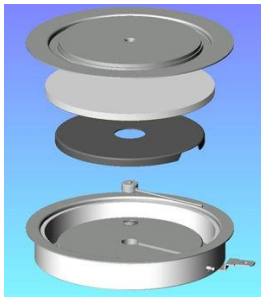
Mounting and Handling Press-pack Semiconductor Devices

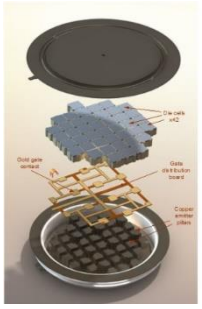
Objectives

This document outlines the minimum mounting conditions for Littelfuse high power devices along with instructions to achieve proper mounting. Press-pack devices are divided into two groups. GTOs, diodes, and thyristors share a common internal construction, while IGBTs are built using a different approach. **Figure 1** briefly highlights the differences.

(a) Disc-shaped device



(b) Internal construction scheme for bipolar types



(c) Internal construction scheme for IGBT types

Figure 1. Differences between the Press-pack Technologies

Disc devices containing thyristors, diodes, GTOs, or IGBTs are often stacked to support dedicated demands and set up the desired topology. This mounting technology requires precise alignment and careful handling of the power semiconductors as well as sophisticated mechanical construction. The most important factor in stacked assemblies is a homogeneous distribution of mounting forces.

Applications

- High-power motor drives, Medium-Voltage drives, Soft-starters
- Welding, Induction Melting, and Electro-chemical power supplies
- Static Synchronous Compensators (STATCOM) and HVDC-based power transmission
- Rail, Marine, and Mining transportation
- Renewable energies – Wind and Solar power

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Target Audience

This document is intended for potential adopters of high-power semiconductors who want to determine the appropriate mounting and handling to ensure proper electrical and thermal performance as well as achieving a reliable mechanical situation.

Contact Information

For more information on this topic, contact the Littelfuse Power Semiconductor team of product and applications experts:

- North America – NA_PowerSemi_Tech@Littelfuse.com
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- Europe. Middle East, & Africa – EMEA_PowerSemi_Tech@Littelfuse.com
- Asia, Australia, & Pacific Islands – APAC_PowerSemi_Tech@Littelfuse.com

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1. Introduction

High-power semiconductors appear to be robust and durable parts at first sight. Despite this robust appearance and the high forces applied to the components during mounting, care must be taken to assemble the components in a suitable manner. Major factors for a successful design include the treatment of all contact surfaces involved, the thermal management, and a mechanical construction that leads to a homogeneous pressure distribution.

2. Disc Devices

As the name implies, disc devices are of circular shape. The housing consists of cylindrical ceramic; upper and lower covers are made from metal and act as electrical contacts to the semiconductor inside. Diodes in this package only feature the power terminals while thyristors, IGBTs, or GTOs have additional terminals for control. A schematical overview is given in **Figure 2**.

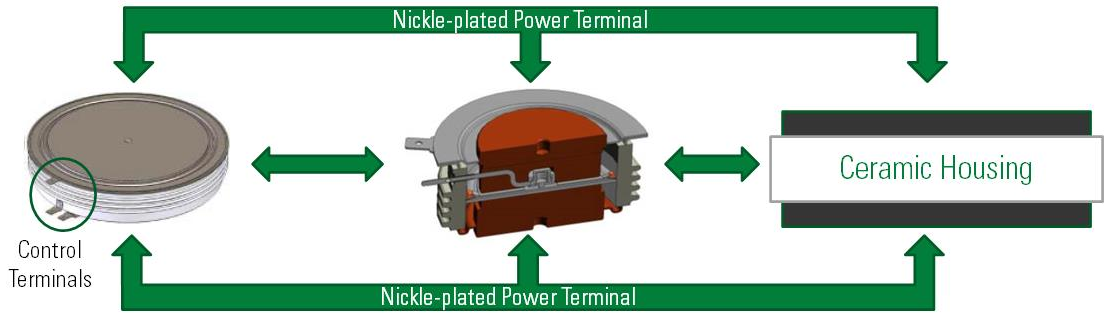

Figure 2. Schematical Overview of Disc Devices, Internal Construction, and Simplified Representation

In contrast to power modules with screw-type terminals, disc devices are contacted purely by pressure which is why they are also referred to as press-packs or capsule types.

2.1. Surface Requirements when Mounting Disc Devices

When using disc devices, the contact area fulfills two functions. It acts as an electrical contact to carry current and at the same time carries the thermal energy to allow proper cooling. As the contact area's partner can be both, heat sink and bus bar at the same time, it is important that these interfaces maintain a stable contact throughout the lifetime of the equipment to ensure reliable operation of the device. Both, the surface geometry, and the surface finish are important factors to be considered. For ease of understanding, heat sink or busbars are considered contact blocks throughout the remaining document. To ensure a low value of thermal resistance, the contact surface of the contact block must be flat, even, and clean. For the mounting area, the surface quality must achieve or exceed the values given in **Figure 3**.

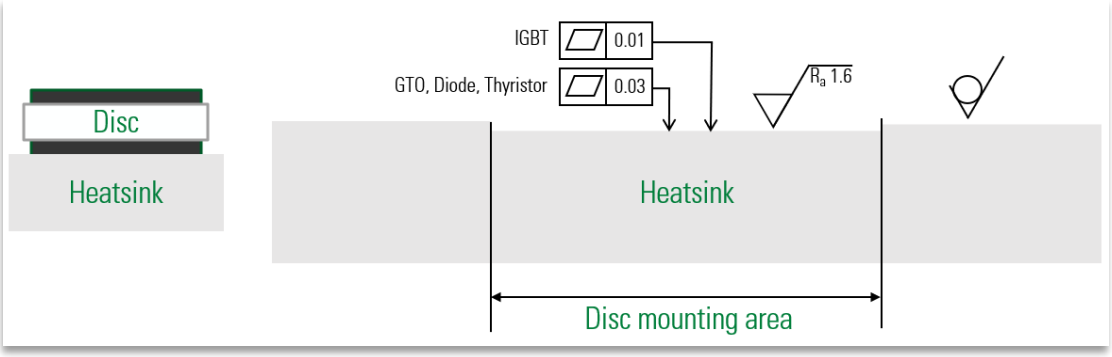

Figure 3. Contact Block Surface Requirements to Mount a Disc Device

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In case the contact block is mounted between two discs, the contact surfaces on both sides must achieve parallelism as sketched in **Figure 4**.

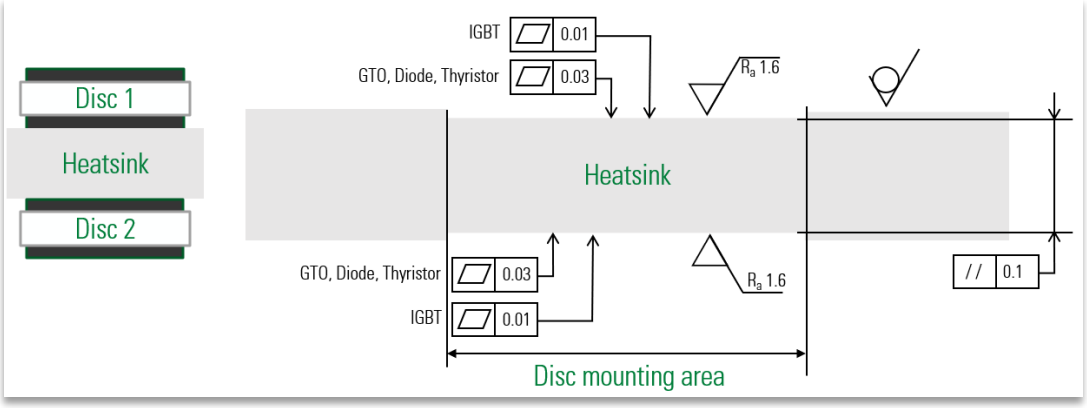


Figure 4. Contact Block Requirements When Discs are Mounted on Both Sides

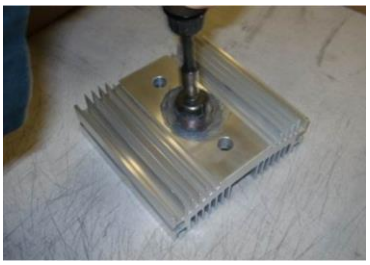
Measuring the flatness of an IGBT's surface in unmounted condition may return values that exceed those specified when being clamped. This is expected because of the component's assembly technology and processes. In no way does this reflect or impact the device flatness once it is clamped to the nominal force.

It is also important to ensure that all components in a stack deform only elastically. A flatness exceeding the maximum specified may result if plastic deformation of the contact surfaces occurs under loading. One example where such effects can potentially be observed is a local collapse of heat sinks. Loss of reliability or lifetime can be a consequence of such an effect.

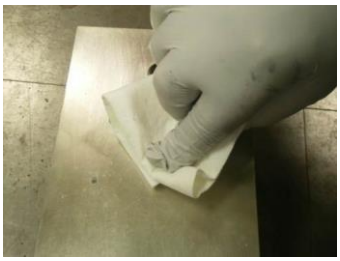
2.2. Surface Treatment

All contact surfaces should be clean and dry prior to assembly. If necessary, non-plated contact surfaces like these from extruded aluminum heat sinks should be lightly abraded to remove oxide films. A proper tool to do so is a rotary wire brush equipped with a suitable contact grease like Jet-Lube SCX13 to form a slurry. Note that the slurry produced by the abrasion should be left on the contact surface until the device is ready to be mounted. This helps to prevent oxidation of the surfaces. Alternatively, polishing the surfaces using 3M Scotch-Brite™ or a similar product can be considered. Right before conflating, the contact surfaces should be cleaned using ethanol or a similar solvent and a lint free cloth. The different steps of this procedure are depicted in **Figure 5**.

(a) Contact grease is applied to the surface sparingly



(b) Abrasion of the heatsink using contact grease and rotating wire brush



(c) Cleaning the surface right before mounting the disc

(d) Mounting surface, lightly abraded

Figure 5. Surface Preparation Sequence

Regarding the power semiconductor or heat sinks with plated surfaces, no further mechanical preparation is required. Cleaning with a suitable cleaning agent prior to mounting is advised to make sure that no particles remain on the surface.

In order to maintain a good electrical connection and avoid corrosion over time, Littelfuse recommends that all non-aluminum contact surfaces be nickel-plated. Chemical plating is preferable to electroplating in high reliability applications. Plating thickness should be 4-6 µm in accordance with that applied to the device or module.

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Prior to mounting, a tiny amount of contact grease is applied to the power terminals of the press-pack homogeneously. In contrast to modules with isolated base plates, this grease must enhance the transfer of thermal energy but may not hinder electric current to flow. Therefore, materials like Jet-Lube SCX13 with metallic particles are used. With some experience, the application can be done with a rubber-roller, as depicted in **Figure 6**.

(a) Applying a very small amount of contact grease with a roller (b) The result is a very thin, homogeneous layer

Figure 6. Applying Contact Grease by Roller and Inspection of the Result

Once the mounting force is applied, only the material necessary to fill microscopic gaps between the contact surfaces remains. Excess material is pressed out and forms a small bead around the semiconductor's perimeter. To get familiar with the process and gather experience, unmounting the disc can be done to inspect the result.

The mounting area should appear almost clean and a small bead with a line width of about 0.1 mm should remain, as seen in **Figure 7**.

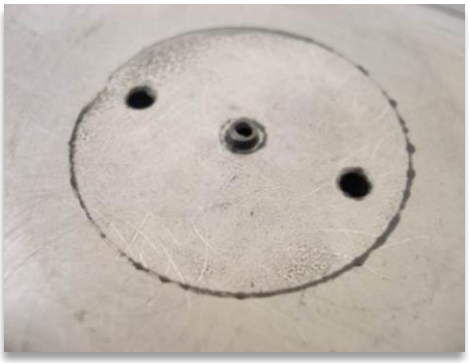

Figure 7. View After Unmounting the Device. A Bead Remains While Mounting Area Appears Almost Clean

Important: This inspection is just to get familiar with the process. Once the device was removed from the heat sink, thorough cleaning of the contact surfaces is mandatory and new contact grease needs to be applied. Putting the device back in place after unmounting is not recommended!

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2.3. Applying the Assembly Force

It is mandatory, yet not trivial, to set up a mechanical fixture that applies the necessary mounting force and achieves a homogeneous distribution at the same time. Littelfuse offers a variety of proven clamp systems to support the construction of high-power semiconductor applications. Size and shape depend on the individual requirements of the application, the size of the component in use, and how many components need to be combined. Common ground for all the designs is the target of applying a proper force and spreading it to the semiconductors in a suitable manner.

The force must be applied perpendicular to the semiconductor's surface. In theory, an even distribution is achieved by applying the force to a single point aligned with the center line of the semiconductor and using suitable mechanical means to spread the force to the available contact area. A schematical overview is seen in **Figure 8**.

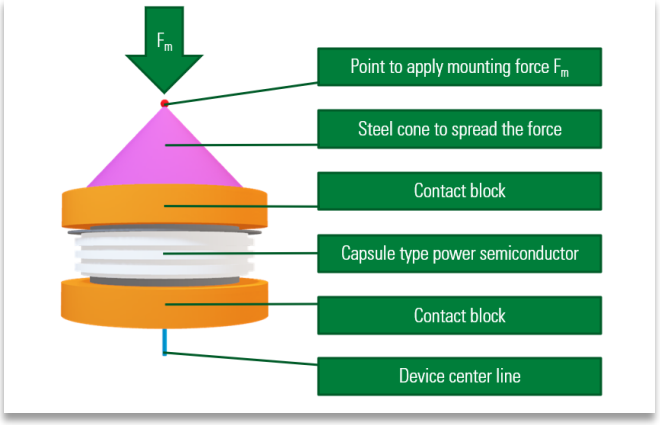

Figure 8. Spreading the Mounting Force to Uniform Distribution

To properly spread the applied force, the cone's diameter must match the semiconductor's diameter and the point angle must not exceed 90°.

2.3.1. Side-by-side Mounting

Depending on the topology to be built, either parallel or anti-parallel connection of power semiconductors may be necessary. Slight variations in the components' dimensions due to tolerances might lead to unnecessary mechanical stress if two devices are clamped using a single bracket. When combining devices with different height dimensions, spacers would be needed to achieve parallel arrangements which would make the design unnecessarily complex. **Figure 9(a)** holds an example where tilting angles due to different dimensions can lead to high mechanical stress to the disc's rims. **Figure 9(b)** displays an illustration with the preferred setup that inherently decouples the mounting forces and is also well-suited to combine devices with different geometries.

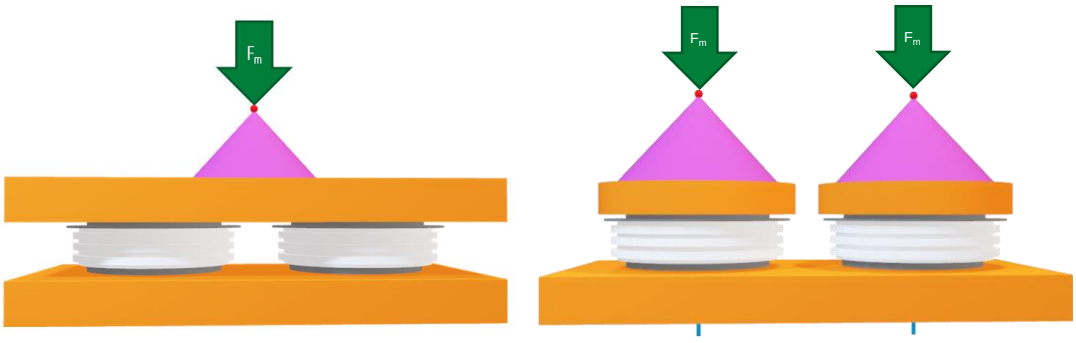

Figure 9. Mounting Two Devices Side-by-side on a Common Carrier

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2.3.2. Stacking Disc Devices

In high-power applications, it is very common to stack devices either to form the desired topology or to achieve higher blocking voltages. As an example, the image in **Figure 10** represents a diode arrangement, capable of blocking 90 kV. Due to specific application requirements, no heat sinks are needed in this design.

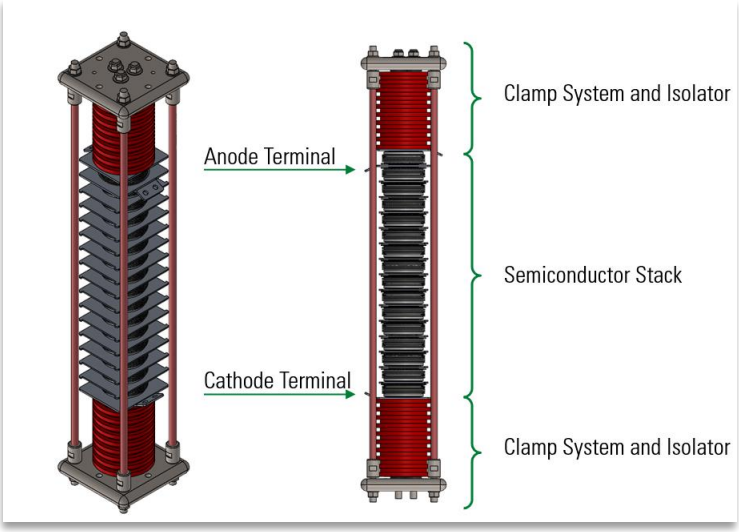

Figure 10. Stacked Diode Arrangement Using Littelfuse Clamping System

Stacks formed from more than just two devices required special attention during construction and assembly. Stacking several identical devices as in the given example is the most basic approach. When combining different devices, their mounting forces must be compatible. This prevents single devices from being overstressed or receiving an unsuitable low pressure. It is also favorable if the diameters of all press-packs involved are in a similar range. During assembly, the mounting direction of the discs is defined by the topology to be built. Attention needs to be paid to mount the discs with the correct orientation.

To facilitate the center alignment, press-packs feature centering holes on both the power terminals. In combination with a corresponding pin, this can be used to precisely align the devices to their central axes. Mechanical holders that align the discs during assembly can also be considered.

As the exploded view in **Figure 11** demonstrates, Littelfuse can supply kits, parts, and complete assemblies to speed up development of stacks.

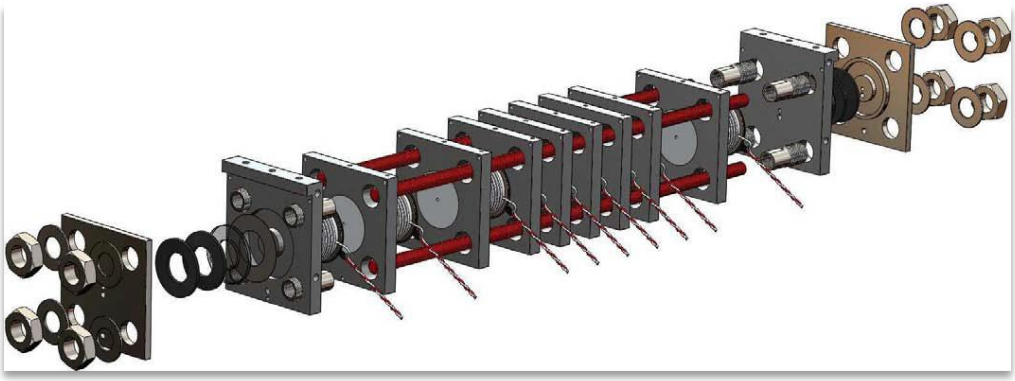

Figure 11. Clamps, Rods, Heatsinks, and other Mechanical Components for Stack-Assemblies

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2.3.3. Design Verification

A homogeneous pressure distribution is a mandatory prerequisite when mounting disc devices as uneven distribution leads to accelerated aging of the components with a risk of premature failure. The pressure distribution is a consequence of properly designing and assembling the stack. As it cannot be measured or monitored in every stack, the mounting procedure and the stack's clamp system need to be defined in a way that ensures a suitable result by design.

A verification of the design needs to be done by monitoring the pressure in a fully assembled system. There are two potential methods of achieving a robust statement regarding pressure distribution.

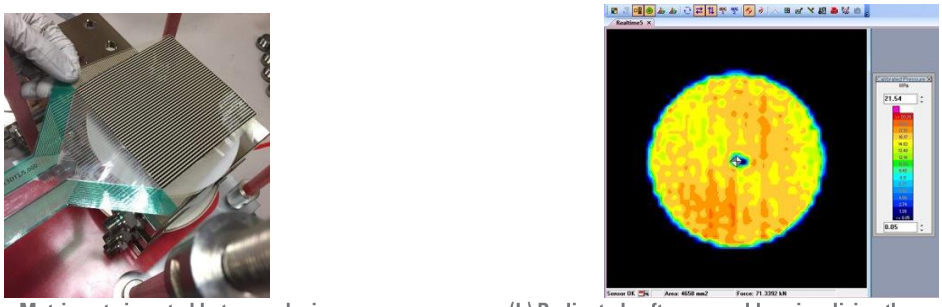
Littelfuse recommends the use of Fuji Prescale film or a similar film product to confirm the pressure uniformity. These films are available in several different pressure ranges and should be inserted between the semiconductor device and the corresponding contact block. Once pressure is applied to an area of the film, the material irreversibly changes color to indicate the local pressure.

The pressure distribution achieved with a given setup can be judged by disassembling the stack and inspecting the film. Uniform color change signals uniform pressure. A suitable pressure distribution and a non-uniform result are summarized in **Figure 12(a)** and **Figure 12(b)** respectively.

(a) Exemplary results showing uniform pressure distribution (b) Poor results, revealing highly non-uniform pressure distribution

Figure 12. Results from Inspecting Pressure Distribution Using Color-Changing Film

The second option is to use pressure sensitive electrical sensor arrays. These consist of a matrix of pressure-sensitive resistors that can be measured by dedicated equipment. The result is displayed as a color-map. In contrast to the irreversible color change of the film, these sensors allow monitoring in real-time and can be reused. A common sensor and a typical result from such a measurement are included in **Figure 13**.



(a) Sensor Matrix gets inserted between devices (b) Dedicated software enables visualizing the captured data

Figure 13. Piezo-electric, Tactile Pressure Sensor, and Captured Results

Both the sensor types need to be removed from the stack as they would prevent proper electric function. As this comes with releasing the pressure in the assembly, re-applying the force after removing the sensor is necessary. The result demonstrated by the measurement can substantiate that the chosen assembly technique reproducibly leads to the correct magnitude of force and to homogeneous pressure distribution.

2.4. Isolation Coordination

High-power applications typically come with high voltages, making isolation coordination an important issue in protecting hardware and people. Clearance and creepage distances for high voltages need to be considered. Correlating information can be derived from the relevant standards, particularly IEC 60664-1 and UL840.

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2.5. Thermal Management Details

The power sections built by disc devices typically reach outstanding efficiency values. Given the amount of energy handled, the absolute value of losses that appear require proper considerations. In general, three types of use-cases can be identified:

- Pulse power applications where energy is handled in a time frame well below a single second. In these cases, the thermal capacity of the material involved may be large enough to absorb the thermal energy without exceeding the technological limits. If so, additional heat sinks turn out to be obsolete.
- Assemblies that need to dissipate a moderate amount of heat which can be done by forced air cooling using extruded aluminum heat sinks.
- Challenging applications with restrictive power-density requirements that can only dissipate the heat with advanced liquid cooling systems.

With press-packs, the cooling systems inevitably makes galvanic contact with electrically life parts. To prevent malfunction or even catastrophic failure, it is important to ensure galvanic connectivity is only present where device terminals share a common voltage node within the intended circuit. Particularly in liquid cooling, cold plates are mounted between the electronic devices. Electrically, each cold plate has a different voltage level while all of them are connected by sharing the same cooling liquid, as sketched in **Figure 14**.

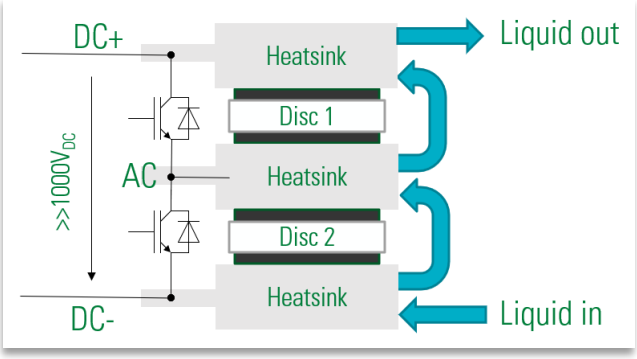

Figure 14. Basic Two-Level Phase Leg with Liquid Cooling

The use of a common cooling liquid requires that neither the cooling liquid itself nor the tubes in use may be electrically conductive. A suitable setup can be achieved using plastic tubes instead of metal parts and a mixture of 80% de-ionized water and 20% glycol ethylene as a cooling liquid. For the same reason, grounding the heat sinks is not an option!

3. Conclusion

Disc–, capsule– or press-pack-devices are key components in high-power electronics in a broad spectrum of applications and use cases. Despite their robust appearance, these components are challenging in terms of handling and mounting. Building and verifying a power section based on disc devices can best be done by applying proven mechanical concepts and components. Mastering the mechanical, thermal, and electrical challenges is a prerequisite to achieving long-lasting, reliable, and efficient designs. As there are plenty of standardized solutions for different applications that potentially can be customized to particular needs, a primary evaluation should consider whether acquiring a ready-made system solution could be the better option.

For additional information please visit www.Littelfuse.com/powersemi

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IXYS UK WESTCODE

Date:- 14th September, 2018

Issue: 1

An application note on wearout failure mechanisms

In general, the overall reliability of power semiconductor devices is represented by the “bathtub” curve shown in figure 1. The wearout phase of a device is linked to the general accumulation of physical damage under the operating load conditions in the application. The main changes in the properties of the device are linked to mechanical wear out due to the differences in the thermal expansion coefficients of the components in the housing. The surface of the die can show significant “scrubbing” due to expansion and contraction of the components. The scrubbing may lead to the formation of intermetallic compounds at these component interfaces as shown in figures 2-4. The build-up can then lead to changes in the on-state, V_T or forward voltage, V_F characteristic and in addition changes in the junction leakage current over long periods of time.

It is difficult to provide actual quantitative values to the X axis as this will depend very much on the conditions in the application. However, for many applications it is prudent to consider a refurbishment program after around thirty years’ service.

Generally, it is not good practice to remove a device from an assembly and then re-mount that device back into the same assembly using the same components. The device is unlikely to be re-located in exactly the same orientation in the clamp assembly, so the contact of the components is likely to be compromised due to the extended time in service.

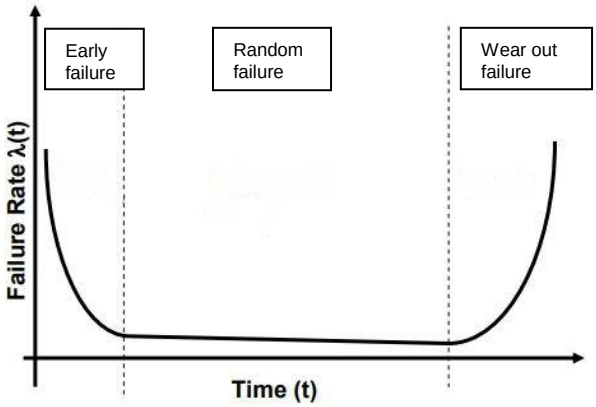

Figure 1: Typical “bathtub” curve

Figure 2: Initial evidence of thermal cycling scrubbing at the edge on the cathode contact area

Figure 3: Initial evidence of thermal cycling scrubbing on the anode molybdenum contact

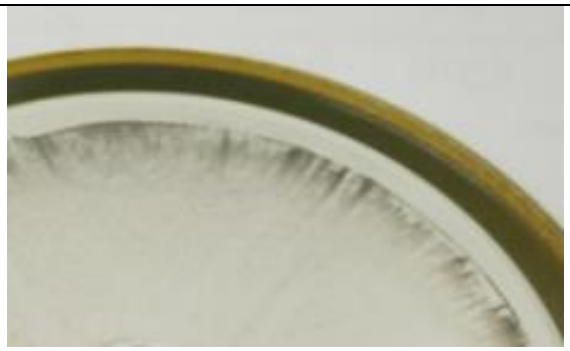

Figure 4: More extensive evidence of thermal cycling scrubbing at the edge on the cathode contact area

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IXYS UK WESTCODE

Date: 1st August 2017

Issue: 3

Application note for the use of a rectifier diode above $T_{j(max)}$ with a short term overload

Introduction

In many applications, semiconductor converters are subject to infrequent short-term overload periods. In order to make efficient use of the semiconductor device it is possible to consider a short term increase in junction temperature above $T_{j(max)}$ but at a reduced voltage.

Rectifier diode operation at an elevated temperature

Silicon rectifier diode characteristics are temperature dependant to some degree. For a modest increase in junction temperature many of these characteristics are of little consequence in line frequency converters.

Above the rated maximum junction temperature, $T_{j(max)}$ the reverse leakage current, I_{RRM} will approximately double for every 10°C rise above $T_{j(max)}$ as shown in figure 1. As the leakage current increases the power dissipation within the diode will increase and the potential for hot spots to form in the silicon could increase significantly. This mechanism could ultimately lead to component failure.

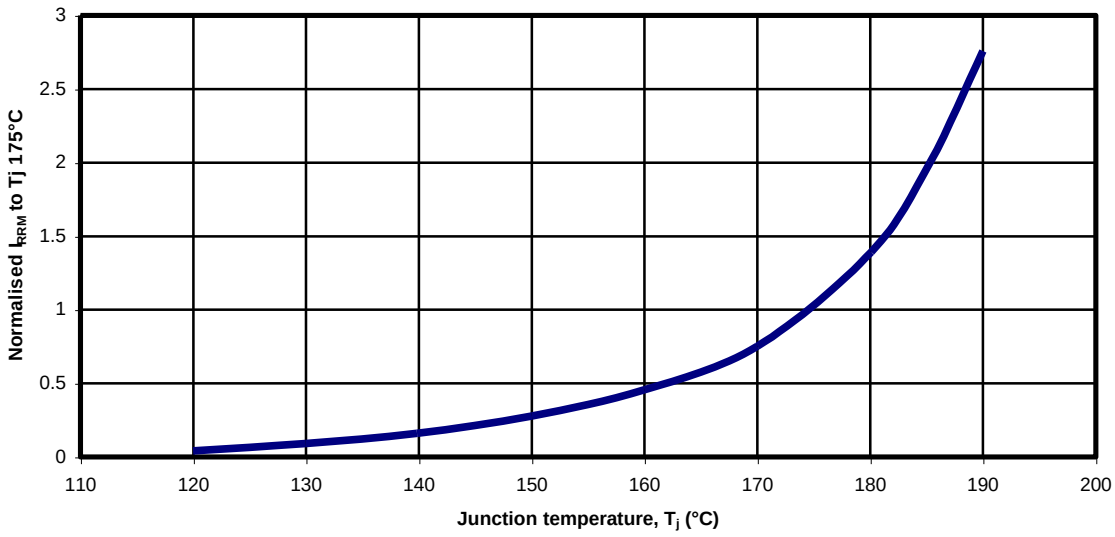

Figure 1: Normalised I_{RRM} vs Tj

In the majority of applications however there is a significant margin between the device rating and the applied working voltage. This is required to allow for transients induced by commutation and network disturbances.

It can be seen in figure 2 that the leakage current typically halves for a 20% drop in the applied voltage.

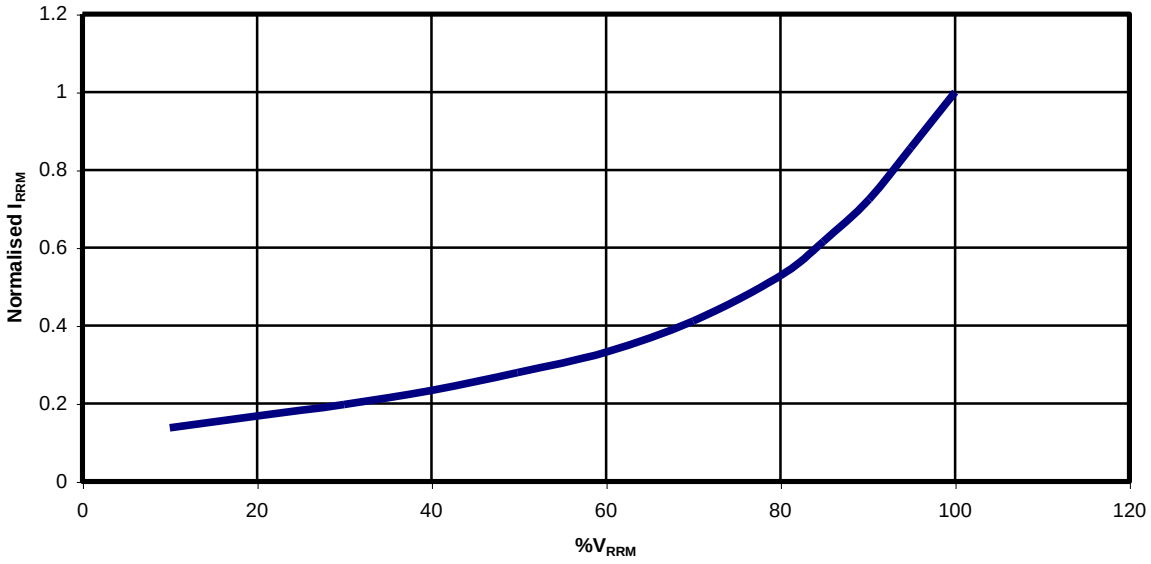

Figure 2: Normalised I_{RRM} vs % applied voltage

It is therefore reasonable to assume that in such applications it may be permissible to operate at an elevated junction temperature for a short period of time.

Designs in which the junction temperature of up to 15°C beyond the maximum rated value of T_j for transient operation with a maximum working peak voltage of 60% of the device rating have been successfully implemented. The transient overload period is limited by the thermal stability of the blocking junction and will vary according to cooling conditions and individual device geometry. Typically overloads up to 60 seconds are acceptable for all IXYS UK Westcode line frequency rectifiers.

It should be noted that during an overload period it may be appropriate to use the transient thermal impedance curve to calculate the increase in junction temperature. To demonstrate a graph of forward current and junction temperature vs time is shown in figure 3. The diode is conducting 5000A DC and the junction temperature is calculated at $T_{j(max)}$ using the steady state thermal resistance value. During this time a series of overload events takes place and the temperature increase is reflected using the transient thermal impedance curve. Information relating to the transient thermal impedances can be found in the data sheets.

For very short overload periods a much higher junction temperature is possible. Under typical limit surge conditions the device junction temperature may exceed 350°C. Please refer to the individual device data sheets for more information relating to surge events.

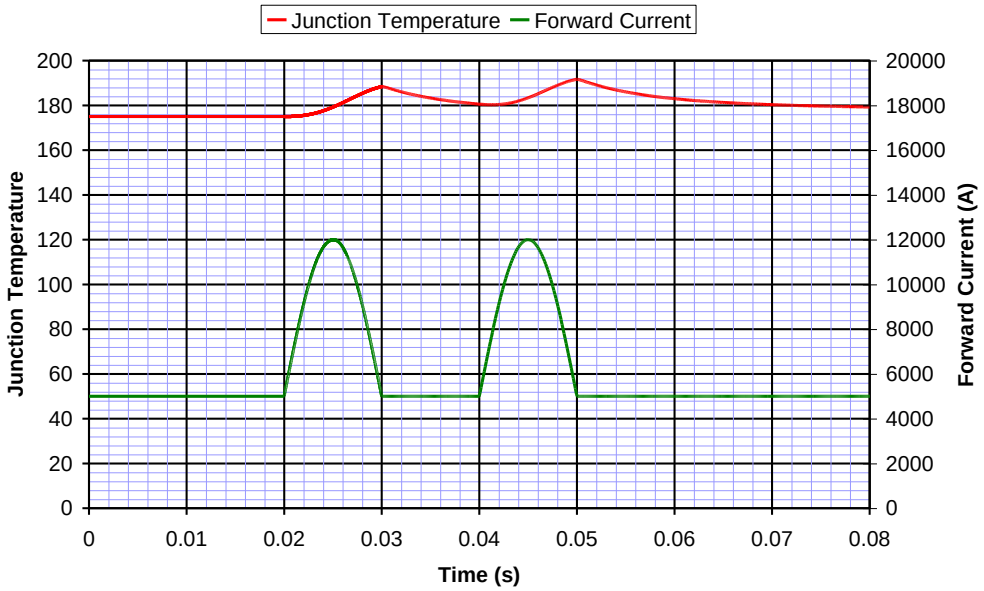

Figure 3: Forward current, junction temperature vs time under overload conditions

Precautions

Other device characteristics will be affected by increasing the T_j beyond that specified in the datasheet, in particular:

1. Increased recovered charge of typically 10% of Q_{rr} per 15°C. This increase must be factored into any snubber design.
2. A shift in the on state characteristics, specifically a small reduction in V_{T0} and a small increase in R_T. This shift could be as much as 5% per 15°C.

Other characteristics such a forward recovery voltage, V_{FR} could be affected but these parameters are less likely to be significant in typical rectifier applications.

One final point to consider is that of thermal cycling load. Operation of a diode with a large temperature deviation (ΔT) is likely to accelerate the mechanical wear out of the internal components and could lead to a reduction in the useful life of the diode. Again it is unlikely that this will present as an issue, but it may warrant investigation.

Summary

The application of rectifier diodes with a junction temperature of 15°C beyond the maximum rated value for transient operation of with an upper limit working peak voltage of 60% of rating has been successfully achieved. The transient overload period is limited by the thermal stability of the blocking junction and will vary according to cooling conditions and individual device geometry. Typically overloads up to 60 seconds are acceptable for all IXYS UK Westcode line frequency rectifiers.

The effects of the increased temperature on the various parameters have been briefly outlined.

It should be noted that the customer must be satisfied as to the suitability of this approach in the specific application.

Disclaimer

The guidance given herein is provided for information only and IXYS UK Westcode in no way implies any warranty for devices operated outside of the maximum ratings as specified in the datasheet.

Any application of devices beyond maximum ratings should be thoroughly qualified and validated on an individual basis.

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IXYS UK WESTCODE

Date: 1st October 2015

Issue: 2

An application note for stocking and handling requirements of press pack devices and pressure contacted modules

Stocking and handling requirements

IXYS UK Westcode recommends that devices and assemblies be stocked in their original packaging if possible. The devices and assemblies should be stored within the temperature range specified in the data sheet. Storage in conditions of very high humidity of greater than 95%RH for long periods should be avoided. The primary pack boxes should not be stacked more than five boxes high.

Press pack devices, assemblies and pressure contacted modules can be stored indefinitely as long as the storage conditions are within the limits specified in the datasheet. Pressure contact devices do not deteriorate with time.

Care should be taken in handing the devices and assemblies; in particular damage to the following should be avoided:

- Scratches and dents to the external anode and cathode contact faces of the device may result in reduced thermal and electrical performance.
- Mechanical damage to the device flanges, which may result in loss of hermetic sealing and a possible reduction in the useful life of the device.
- Cracking or chipping of the alumina ceramic which may result in loss of hermetic sealing or a reduction in tracking performance between the anode and cathode.
- Distortion to the end plates, bus bars and coolers of an assembly, which may result in water leaks, poor thermal performance or the inability to mount the stack to the assembly fixtures.
- Scratches or fingerprints on the assembly components that could damage the surface passivation and result and increase in localised oxidation or corrosion.
- Damage to assemblies resulting from multiple stacking.

It is recommended that latex, vinyl or nitrile gloves be worn when handing devices or assemblies.

Assemblies utilising oil filled capacitors should be orientated to prevent oil leaking from the capacitor.

The recommended manual handling procedures should be adopted when handling a number of devices or an assembly to avoid potential personal injuries. For an assembly, a crane or other suitable handing equipment is recommended.

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IXYS UK WESTCODE

Date: 28th November 2013

Issue: 1

An application note for soldering leads to thyristors, GTO's and IGBT's

Figure 1 *All device types - Set up* Ensure that the temperature controller for the soldering iron is set high enough to melt the solder.	
Figure 2 *Cathode tag and gate pin solder process* Use a pair of pliers to attach the cathode tag to the cathode terminal. Note that this solder process also applies to GTO's.	
Figure 3 *Cathode tag and gate pin solder process* Use a pair of pliers to attach the gate terminal to the gate pin. The pin will click into position when it is correctly seated.	

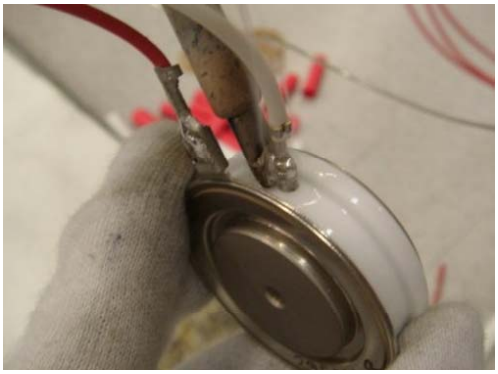
Figure 4 *Cathode tag and gate pin solder process* Wipe the soldering iron tip with a sponge moistened with water and apply a small amount of solder to the tip of the soldering iron. This will assist the wetting process.	
Figure 5 *Cathode tag and gate pin solder process* Place the soldering iron in contact with the cathode tag as shown and allow the solder to wet the joint. Pull the device away from the soldering iron and allow to joint to cool.	
Figure 6 *Cathode tag and gate pin solder process* Place the gate terminal and pin into contact with the soldering iron and apply solder to the joint. Ensure that the solder wets the joint. Pull the device away from the soldering iron and allow to joint to cool.	
Figure 7 *Solder inspection - Cathode tag* Some evidence of flux can be seen on the weld flange area but the solder must not have flow beyond the weld area.	

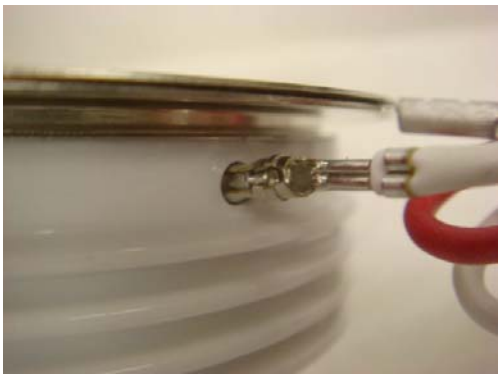
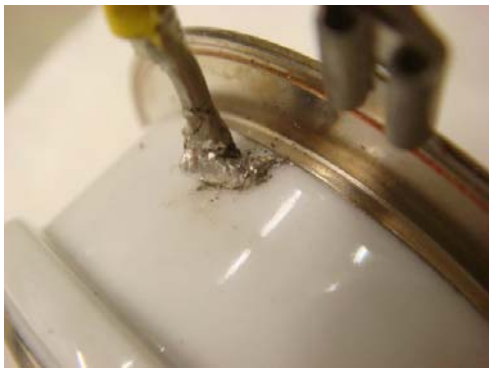
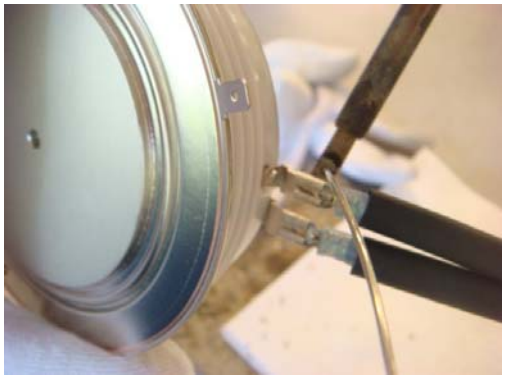
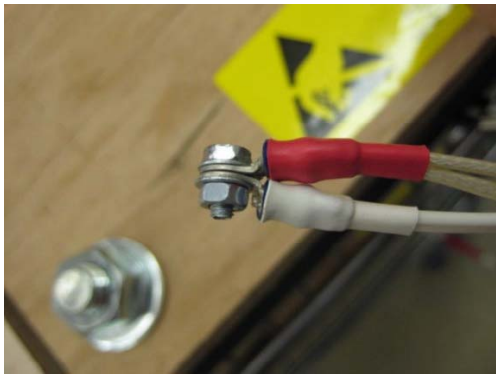
Figure 8 *Solder inspection - Gate pin* Inspect the cathode tag soldered joint. Ensure that the solder has fully wet the joint.	
Figure 9 *Solder inspection - Gate pin* Check that the solder has flowed correctly onto the gate pin. The picture shows EXCESSIVE SOLDER shorting the gate to the cathode. This solder must be removed, cleaned and re-soldered.	
Figure 10 *Shrink sleeving* Place the sleeving (if required) over the soldered leads and push up to the gate and cathode tag terminals.	
Figure 11 *Shrink sleeving* Shrink the sleeving using a hot air gun. Inspect the sleeving to ensure it has shrunk evenly around the terminals and that no exposed copper wire is showing between the end of the terminal and the lead insulation.	

Figure 12 *Cleaning process* Spray a small amount of flux removing solvent onto a tissue and remove the flux from the top face of the cathode return flange. Note that if clear sleeving is used the flux removal should be carried out before the sleeving process is complete.	
Figure 13 *Cleaning process* Gently remove the flux from the underside of the cathode flange.	
Figure 14 *Cleaning process* Apply a small amount of flux removing solvent to a short bristled brush.	
Figure 15 *Cleaning process* Remove the flux underneath the cathode tag using the brush.	

Figure 16 *Cleaning process* Remove the excess flux close to the gate pin using the tweezers.	
Figure 17 *Cleaning process* Clean the anode poleface with a tissue soaked in flux removing solvent.	
Figure 18 *Cleaning process* Clean the cathode poleface with a tissue soaked in flux removing solvent.	
Figure 19 *IGBT solder instructions* Take ESD precautions when soldering IGBT devices.	

Figure 20 *IGBT solder instructions* Tighten the ESD wrist strap onto the appropriate wrist.	
Figure 21 *IGBT solder instructions* Place the heatshrink onto the lead terminations as shown.	
Figure 22 *IGBT solder instructions* Remove the shorting clip from the emitter and gate connectors.	
Figure 23 *IGBT solder instructions* Gently push on the connectors to the termination.	

Figure 24 *IGBT solder instructions* Solder using the same process as shown for thyristors. Follow the thyristor instructions for the heatshrink process.	
Figure 25 Ensure that the gate lead terminals are shorted before removing the ESD protection shown in figures 19 and 20.	

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